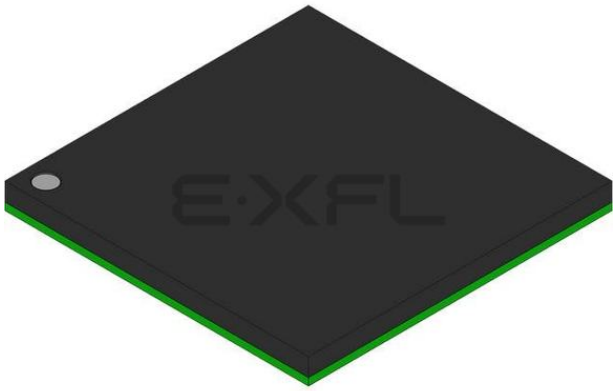

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	61
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5270vm100j

3 Features

For a detailed feature list see the MCF5271 Reference Manual (MCF5271RM).

4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF5271 signals, consult the *MCF5271 Reference Manual* (MCF5271RM).

4.1 Signal Properties

Table 4 lists all of the signals grouped by function. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts and Part Numbers," for package diagrams.

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 2. MCF5270 and MCF5271 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
Reset						
$\overline{\text{RESET}}$	—	—	—	I	83	N13
$\overline{\text{RSTOUT}}$	—	—	—	O	82	P13
Clock						
EXTAL	—	—	—	I	86	M14
XTAL	—	—	—	O	85	N14
CLKOUT	—	—	—	O	89	K14
Mode Selection						
CLKMOD[1:0]	—	—	—	I	20,21	G5,H5
$\overline{\text{RCON}}$	—	—	—	I	79	K10
External Memory Interface and Ports						
A[23:21]	PADDR[7:5]	$\overline{\text{CS}}$[6:4]	—	O	126, 125, 124	B11, C11, D11

Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
A[20:0]	—	—	—	O	123:115, 112:106, 102:98	A12, B12, C12, A13, B13, B14, C13, C14, D12, D13, D14, E11, E12, E13, E14, F12, F13, F14, G11, G12, G13
D[31:16]	—	—	—	O	22:30, 33:39	G1, G2, H1, H2, H3, H4, J1, J2, J3, J4, K1, K2, K3, K4, L1, L2
D[15:8]	PDATAH[7:0]	—	—	O	42:49	M1, N1, M2, N2, P2, L3, M3, N3
D[7:0]	PDATAL[7:0]	—	—	O	50:52, 56:60	P3, M4, N4, P4, L5, M5, N5, P5
$\overline{BS}$[3:0]	PBS[7:4]	$\overline{CAS}$[3:0]	—	O	143:140	B6, C6, D7, C7
$\overline{OE}$	PBUSCTL7	—	—	O	62	N6
$\overline{TA}$	PBUSCTL6	—	—	I	96	H11
$\overline{TEA}$	PBUSCTL5	$\overline{DREQ1}$	—	I	—	J14
R/$\overline{W}$	PBUSCTL4	—	—	O	95	J13
$\overline{TSIZ1}$	PBUSCTL3	DACK1	—	O	—	P6
$\overline{TSIZ0}$	PBUSCTL2	DACK0	—	O	—	P7
$\overline{TS}$	PBUSCTL1	DACK2	—	O	97	H13
$\overline{TIP}$	PBUSCTL0	DREQ0	—	O	—	H12
Chip Selects						
$\overline{CS}$[7:4]	PCS[7:4]	—	—	O	—	B9, A10, C10, A11
$\overline{CS}$[3:2]	PCS[3:2]	SD_CS[1:0]	—	O	132,131	A9, C9
$\overline{CS1}$	PCS1	—	—	O	130	B10
$\overline{CS0}$	—	—	—	O	129	D10
SDRAM Controller						
$\overline{SD\_WE}$	PSDRAM5	—	—	O	92	K13
$\overline{SD\_SCAS}$	PSDRAM4	—	—	O	91	K12
$\overline{SD\_SRAS}$	PSDRAM3	—	—	O	90	K11
SD_CKE	PSDRAM2	—	—	O	—	E8
$\overline{SD\_CS}$[1:0]	PSDRAM[1:0]	—	—	O	—	L12, L13

Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
UARTs						
U2TXD	PUARTH1	—	—	O	—	A8
U2RXD	PUARTH0	—	—	I	—	A7
$\overline{\text{U1CTS}}$	PUARTL7	$\overline{\text{U2CTS}}$	—	I	136	B8
$\overline{\text{U1RTS}}$	PUARTL6	$\overline{\text{U2RTS}}$	—	O	135	C8
U1TXD	PUARTL5	—	—	O	133	D9
U1RXD	PUARTL4	—	—	I	134	D8
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	12	F3
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	15	G3
U0TXD	PUARTL1	—	—	O	14	F1
U0RXD	PUARTL0	—	—	I	13	F2
DMA Timers						
DT3IN	PTIMER7	$\overline{\text{U2CTS}}$	QSPI_CS2	I	—	H14
DT3OUT	PTIMER6	$\overline{\text{U2RTS}}$	QSPI_CS3	O	—	G14
DT2IN	PTIMER5	$\overline{\text{DREQ2}}$	DT2OUT	I	66	M9
DT2OUT	PTIMER4	DACK2	—	O	—	L9
DT1IN	PTIMER3	$\overline{\text{DREQ1}}$	DT1OUT	I	61	L6
DT1OUT	PTIMER2	DACK1	—	O	—	M6
DT0IN	PTIMER1	$\overline{\text{DREQ0}}$	—	I	10	E4
DT0OUT	PTIMER0	DACK0	—	O	11	F4
BDM/JTAG[2]						
DSCLK	—	TRST	—	O	70	N9
PSTCLK	—	TCLK	—	O	68	P9
$\overline{\text{BKPT}}$	—	TMS	—	O	71	P10
DSI	—	TDI	—	I	73	M10
DSO	—	TDO	—	O	72	N10
JTAG_EN	—	—	—	I	78	K9
DDATA[3:0]	—	—	—	O	—	M12, N12, P12, L11
PST[3:0]	—	—	—	O	77:74	M11, N11, P11, L10

will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop V_{DD} to 0 V.
2. Drop OV_{DD}/V_{DDPLL} supplies.

5.3 Decoupling

- Place the decoupling caps as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 µF and 0.01 µF at each supply input

5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See Section 7, “Electrical Characteristics.”

5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

5.7 Interface Recommendations

5.7.1 SDRAM Controller

5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

Table 3. Synchronous DRAM Signal Connections

Signal	Description
$\overline{\text{SD\_SRAS}}$	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SD\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals.
$\overline{\text{SD\_SCAS}}$	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM.
$\overline{\text{DRAMW}}$	DRAM read/write. Asserted for write operations and negated for read operations.
$\overline{\text{SD\_CS}}$[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF5271. One $\overline{\text{SD\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
$\overline{\text{BS}}$[3:0]	Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5271 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF5271 Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[3:0]
Transmit error	ETXER
Collision	ECOL
Carrier sense	ECRS
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[3:0]

6.1 Pinout—196 MAPBGA

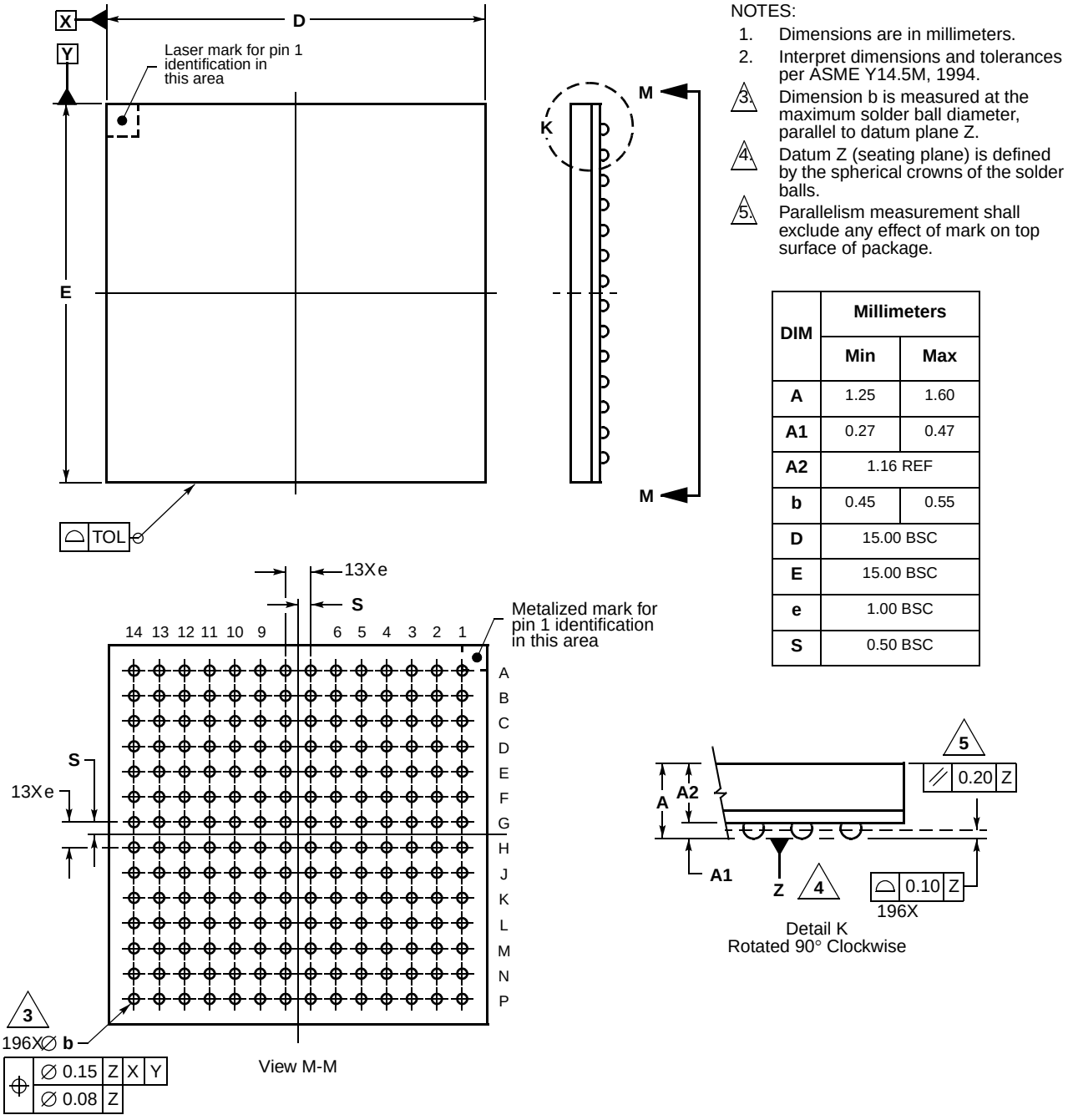
The following figure shows a pinout of the MCF5270/71CVMxxx package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	ETXCLK	ETXD3	ETXD2	QSPI_DOUT	QSPI_CS0	U2RXD	U2TXD	$\overline{CS3}$	$\overline{CS6}$	$\overline{CS4}$	A20	A17	VSS	A
B	ERXD0	ERXER	ETXER	ETXD0	QSPI_DIN	$\overline{BS3}$	QSPI_CS1	U1CTS	$\overline{CS7}$	$\overline{CS1}$	A23	A19	A16	A15	B
C	ERXD2	ERXD1	ETXEN	ETXD1	QSCK	$\overline{BS2}$	$\overline{BS0}$	RTS1	$\overline{CS2}$	$\overline{CS5}$	A22	A18	A14	A13	C
D	ERXCLK	ERXDV	ERXD3	EMDC	EMDIO	Core VDD_4	$\overline{BS1}$	U1RXD1	U1TXD	$\overline{CS0}$	A21	A12	A11	A10	D
E	ECRS	ECOL	NC	TIN0	VDD	VSS	VDD	SD_CKE	VSS	VDD	A9	A8	A7	A6	E
F	U0TXD	U0RXD	U0CTS	DTOUT0	TEST	VSS	VDD	VSS	VDD	VSS	Core VDD_3	A5	A4	A3	F
G	D31	D30	U0RTS	Core VDD_1	CLK MOD1	VDD	VSS	VDD	VSS	NC	A2	A1	A0	DTOUT3	G
H	D29	D28	D27	D26	CLK MOD0	VSS	VDD	VDD	VDD	NC	$\overline{TA}$	$\overline{TIP}$	$\overline{TS}$	DTIN3	H
J	D25	D24	D23	D22	VSS	VDD	VSS	VDD	VSS	VDD	I2C_SCL	I2C_SDA	R/$\overline{W}$	$\overline{TEA}$	J
K	D21	D20	D19	D18	VDD	VDD	VSS	VDD	JTAG_EN	$\overline{RCON}$	$\overline{SD\_RAS}$	$\overline{SD\_CAS}$	$\overline{SD\_WE}$	CLKOUT	K
L	D17	D16	D10	Core VDD_2	D3	DTIN1	$\overline{IRQ5}$	$\overline{IRQ1}$	DTOUT2	PST0	DDATA0	$\overline{SD\_CS1}$	$\overline{SD\_CS0}$	VSSPLL	L
M	D15	D13	D9	D6	D2	DTOUT1	$\overline{IRQ6}$	$\overline{IRQ2}$	DTIN2	TDI/DSI	PST3	DDATA3	VDDPLL	EXTAL	M
N	D14	D12	D8	D5	D1	$\overline{OE}$	$\overline{IRQ7}$	$\overline{IRQ3}$	$\overline{TRST}$/DSCLK	TDO/DSO	PST2	DDATA2	$\overline{RESET}$	XTAL	N
P	VSS	D11	D7	D4	D0	TSIZ1	TSIZ0	$\overline{IRQ4}$	TCLK/PSTCLK	$\overline{TMS}$/$\overline{BKPT}$	PST1	DDATA1	$\overline{RSTOUT}$	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 3. MCF5270/71CVMxxx Pinout (196 MAPBGA)

6.2 Package Dimensions—196 MAPBGA

Figure 4 shows MCF5270/71CVMxxx package dimensions.



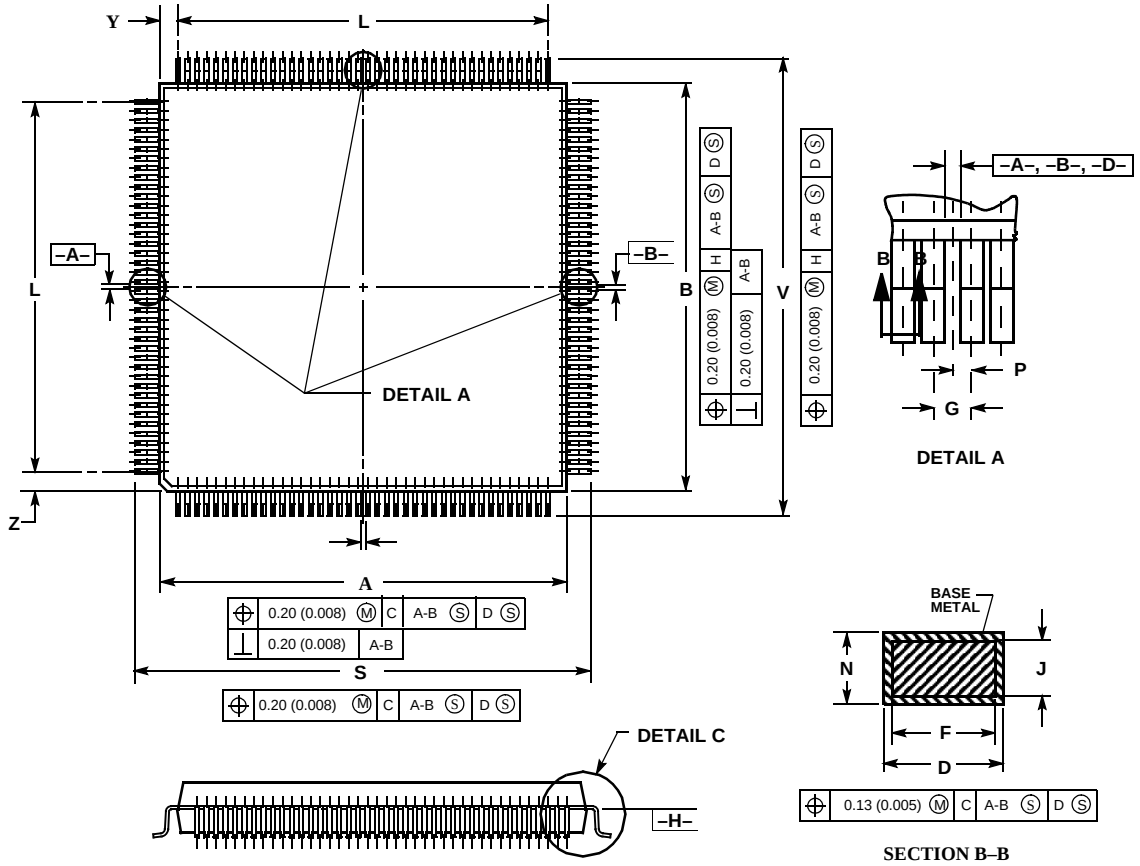
NOTES:
1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

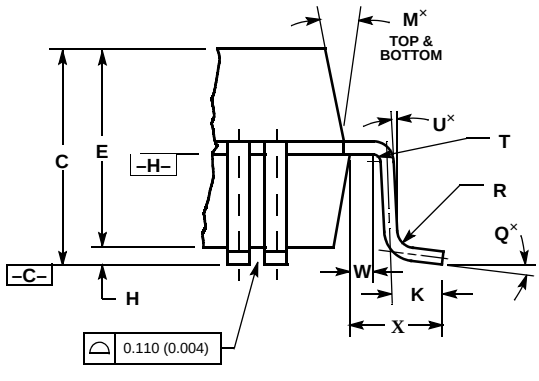
DIM	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 4. 196 MAPBGA Package Dimensions (Case No. 1128A-01)

6.4 Package Dimensions—160 QFP

Figure 6 shows MCF5270/71CAB80 package dimensions.





DETAIL C

NOTES

1. DIMENSIONING AND TOLERINCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLAN -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B-, AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	1.106
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 BSC		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 REF	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.4	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

Case 864A-03

Figure 6. 160 QFP Package Dimensions

6.5 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Lead-Free?	Temperature
MCF5270AB100	MCF5270 RISC Microprocessor	160 QFP	100MHz	Yes	0° to +70° C
MCF5270CAB100	MCF5270 RISC Microprocessor	160 QFP	100MHz	Yes	-40° to +85° C
MCF5270VM100	MCF5270 RISC Microprocessor	196 MAPBGA	100MHz	Yes	0° to +70° C
MCF5270CVM150	MCF5270 RISC Microprocessor	196 MAPBGA	150MHz	Yes	-40° to +85° C
MCF5271CAB100	MCF5271 RISC Microprocessor	160 QFP	100MHz	Yes	-40° to +85° C
MCF5271CVM100	MCF5271 RISC Microprocessor	196 MAPBGA	100MHz	Yes	-40° to +85° C
MCF5271CVM150	MCF5271 RISC Microprocessor	196 MAPBGA	150MHz	Yes	-40° to +85° C

7 Electrical Characteristics

This chapter contains electrical specification tables and reference timing diagrams for the MCF5271 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5271.

NOTE

The parameters specified in this processor document supersede any values found in the module specifications.

7.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
Pad Supply Voltage	OV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3,4,5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

7.5 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 11. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
freq	System bus frequency	$f_{sys/2}$	50	75	MHz
B0	CLKOUT period	t_{cyc}	—	1/75	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	9	—	ns
B1b	$\overline{\text{BKPT}}$ valid to CLKOUT high[3]	t_{BKVCH}	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{\text{BKPT}}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:0]) valid to CLKOUT high	t_{DIVCH}	4	—	ns
B5	CLKOUT high to data input (D[31:0]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications are tested using full drive strength pad configurations in a 50ohm transmission line environment..
2 $\overline{\text{TEA}}$ and $\overline{\text{TA}}$ pins are being referred to as control inputs.
3 Refer to figure A-19.

Timings listed in Table 11 are shown in Figure 7.

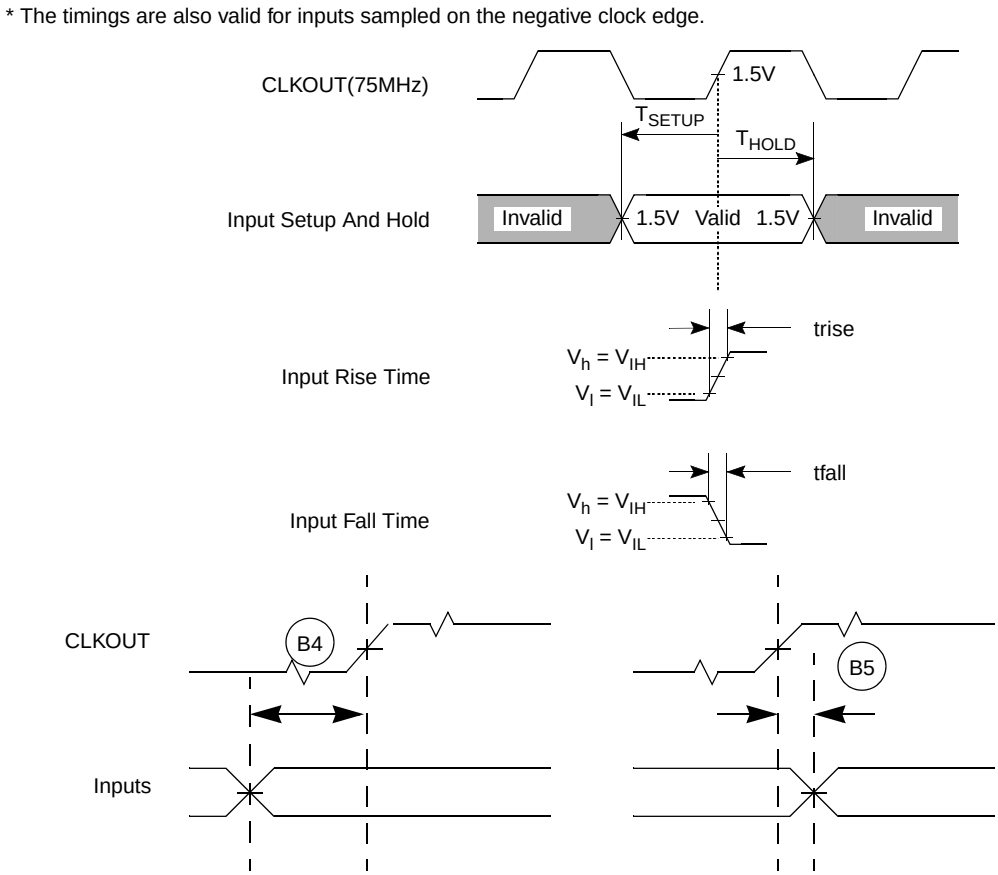


Figure 7. General Input Timing Requirements

7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

Table 12. External Bus Output Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit
Control Outputs					
B6a	CLKOUT high to chip selects valid [1]	t_{CHCV}	—	$0.5t_{CYC}$ +5	ns
B6b	CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2]	t_{CHBV}	—	$0.5t_{CYC}$ +5	ns
B6c	CLKOUT high to output enable ($\overline{OE}$) valid[3]	t_{CHOV}	—	$0.5t_{CYC}$ +5	ns
B7	CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$+1.5	—	ns
B7a	CLKOUT high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$+1.5	—	ns

Table 12. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) valid	t_{CHAV}	—	9	ns
B9	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid	t_{CHAI}	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:0]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:0]) invalid	t_{CHDOI}	1.5	—	ns
B13	CLKOUT high to data output (D[31:0]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}$ transitions after the falling edge of CLKOUT.
2 $\overline{BS}$ transitions after the falling edge of CLKOUT.
3 $\overline{OE}$ transitions after the falling edge of CLKOUT.

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 12.

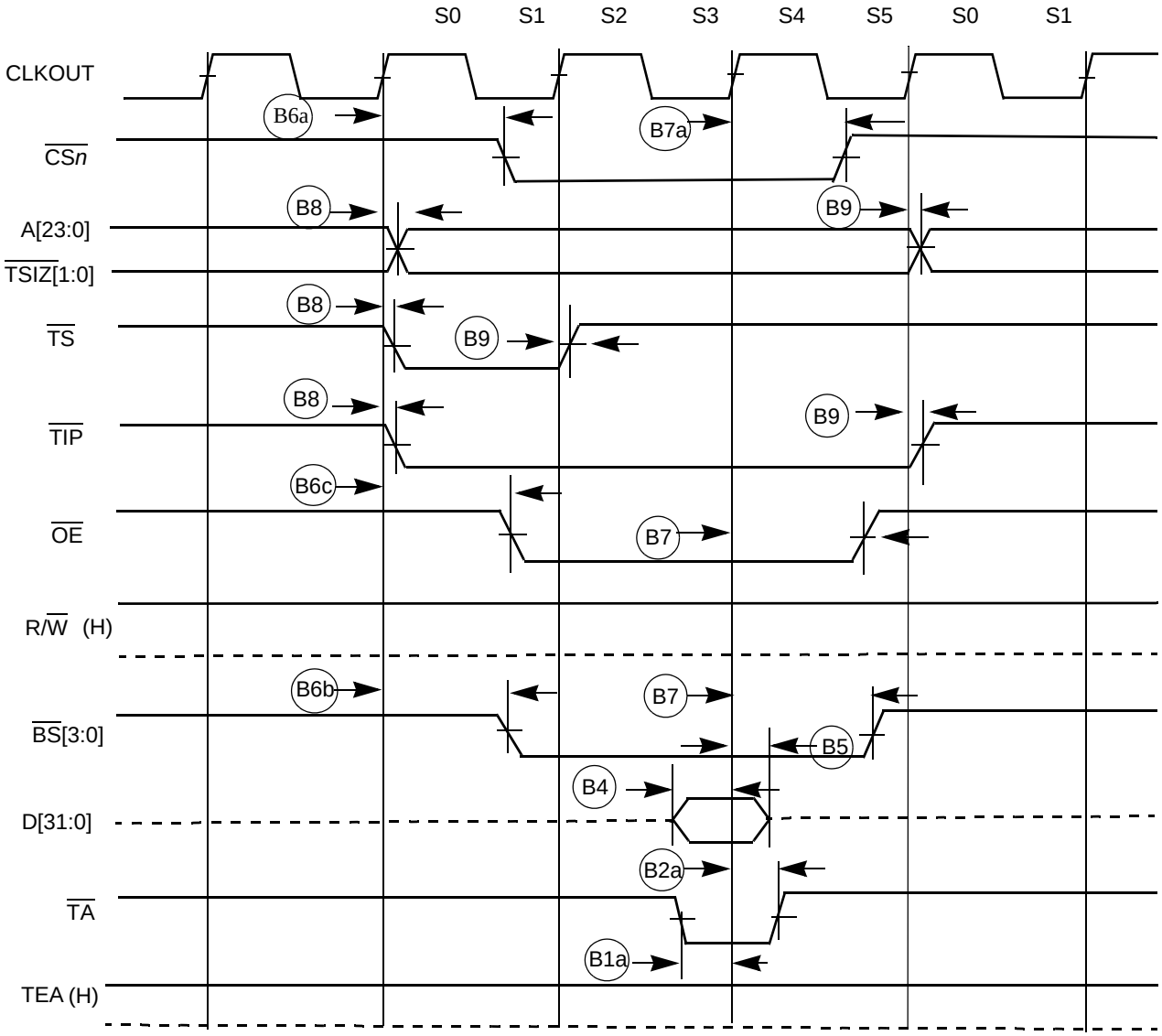
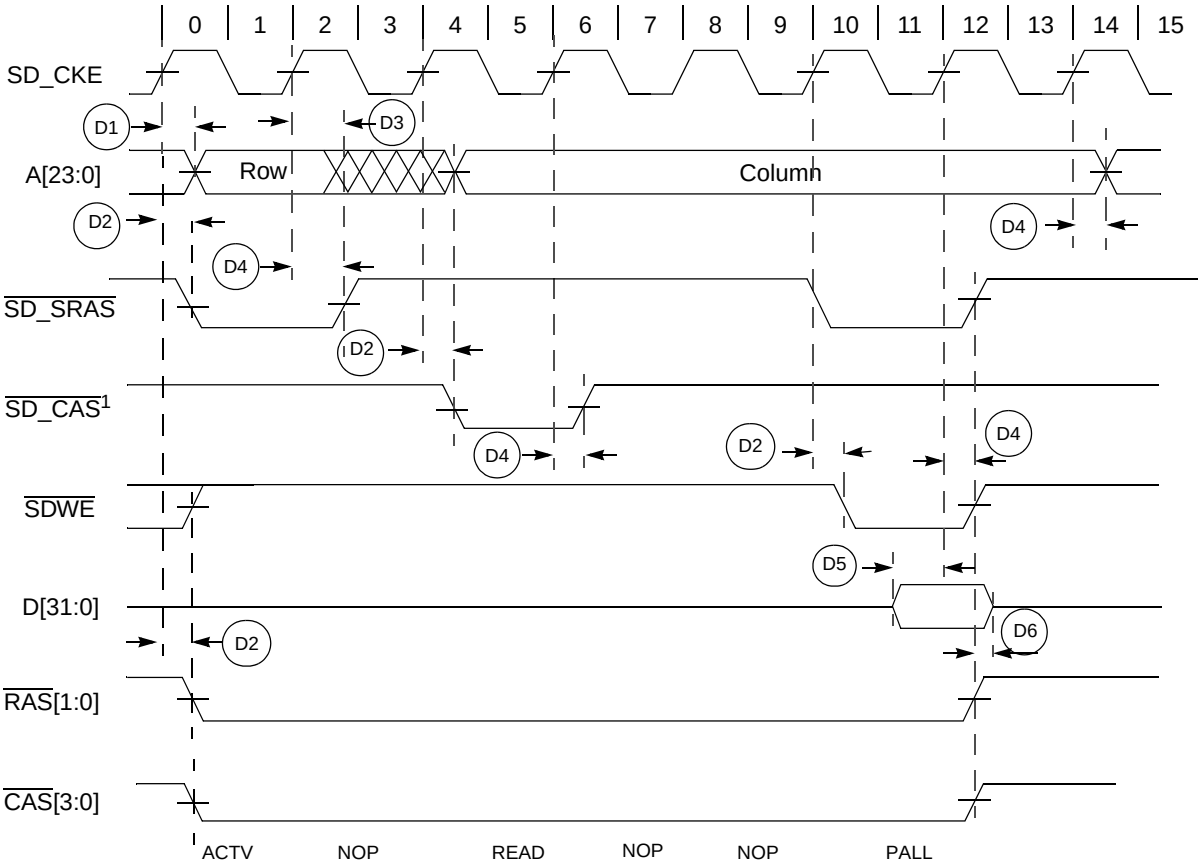


Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$

Figure 11 shows an SDRAM read cycle.



1 DACR[CASL] = 2

Figure 11. SDRAM Read Cycle

Table 13. SDRAM Timing

NUM	Characteristic	Symbol	Min	Max	Unit
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	—	9	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}	—	9	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.5	—	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.5	—	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	4	—	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.5	—	ns
D7[1]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	—	9	ns
D8[1]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.5	—	ns

1 D7 and D8 are for write cycles only.

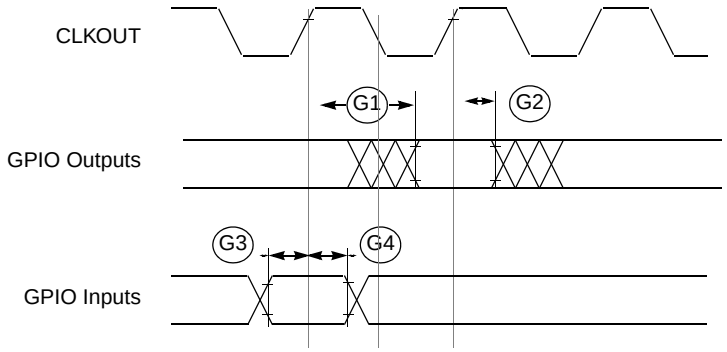


Figure 13. GPIO Timing

7.8 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

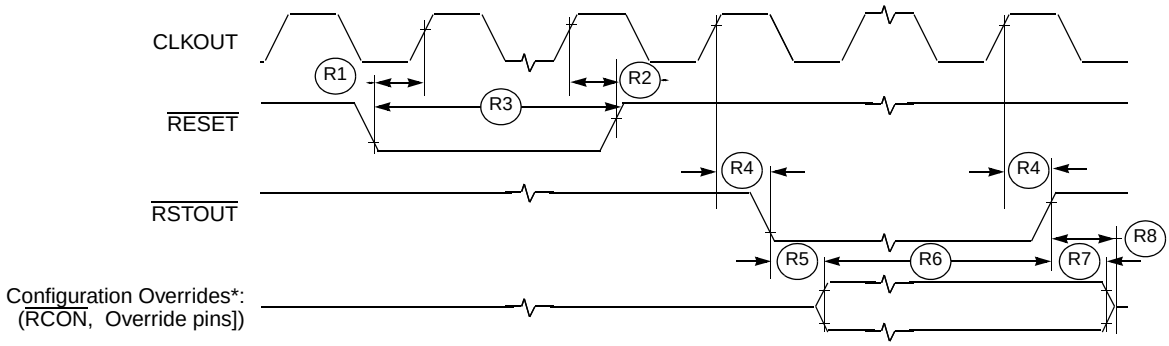


Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing

Refer to the chip configuration module (CCM) chapter in the device's reference manual for more information.

7.9 I²C Input/Output Timing Specifications

Table 16 lists specifications for the I²C input timing parameters shown in Figure 15.

Table 16. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 17 lists specifications for the I²C output timing parameters shown in Figure 15.

Table 17. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

1 Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 17. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 17 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 15 shows timing for the values in Table 16 and Table 17.

7.11 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	0–66 MHz		Unit
		Min	Max	
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

7.12 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[1:0] to QSPI_CLK	1	510	tcyc
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 23 correspond to Figure 20.

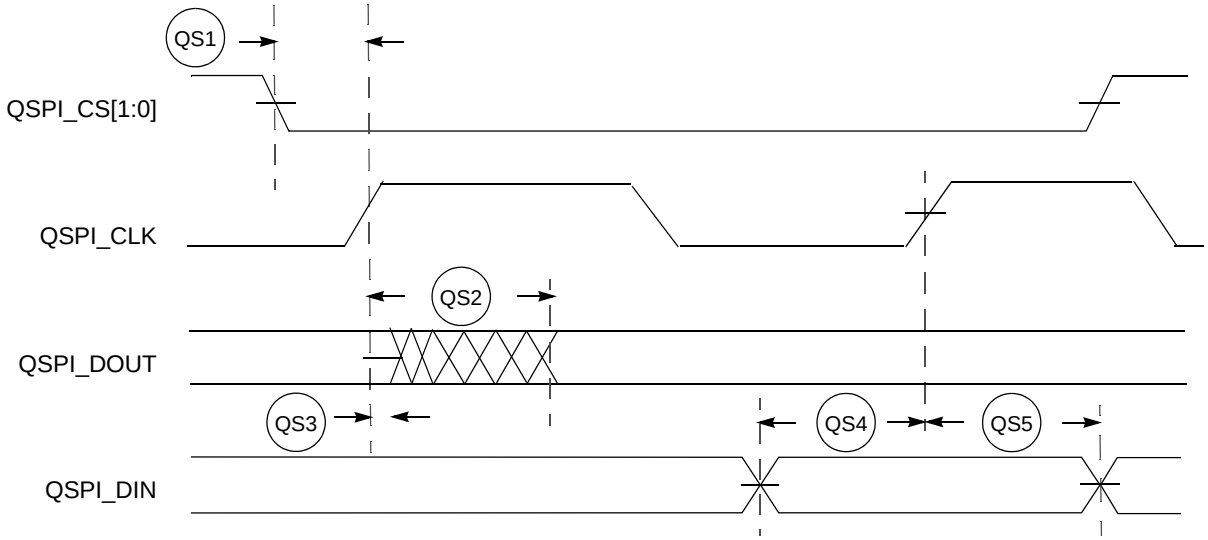


Figure 20. QSPI Timing

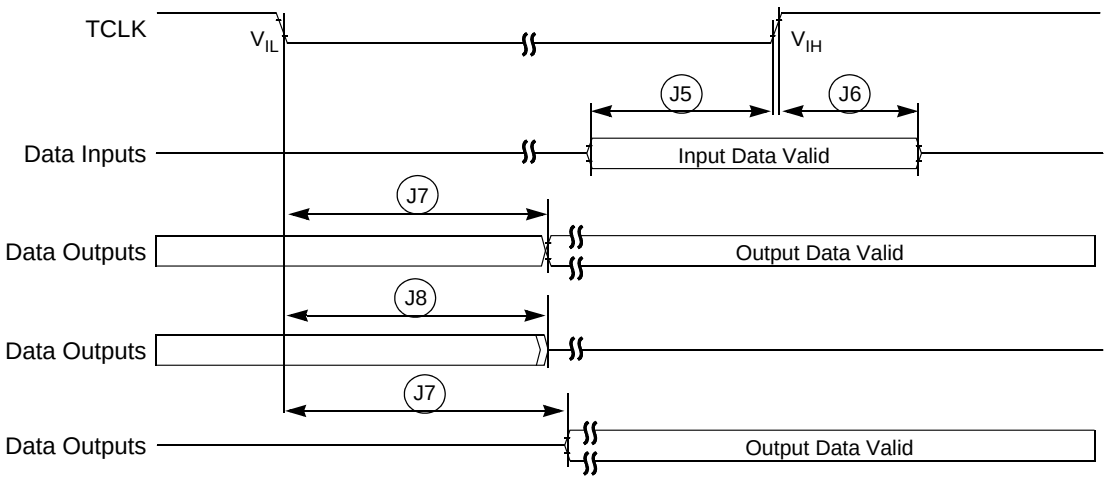


Figure 22. Boundary Scan (JTAG) Timing

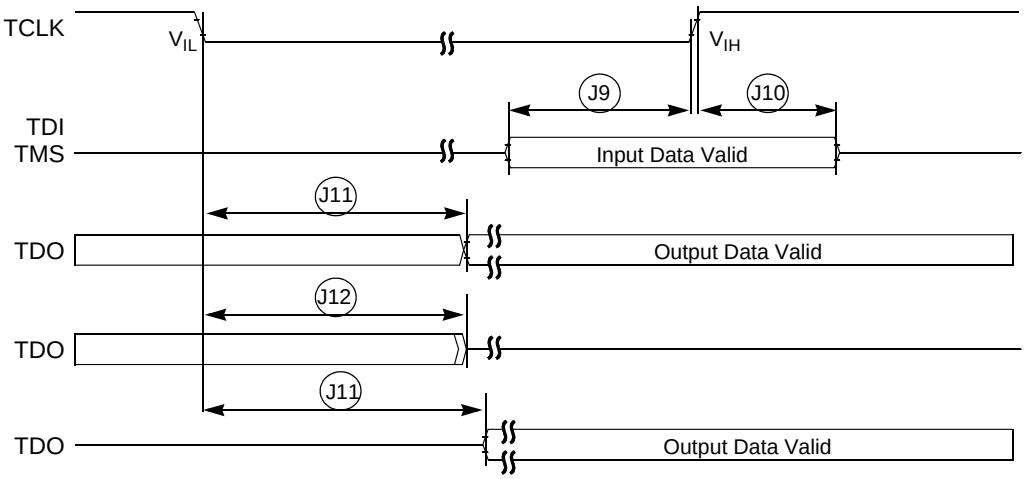


Figure 23. Test Access Port Timing

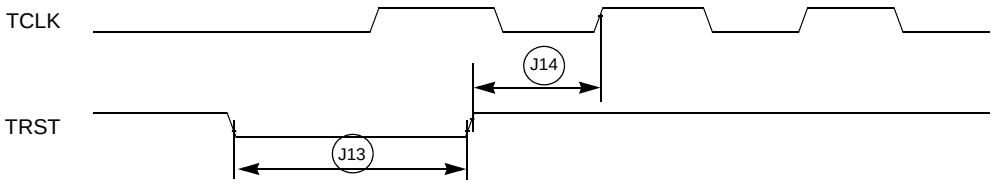


Figure 24. $\overline{\text{TRST}}$ Timing

Table 26. MCF5271EC Revision History (continued)

Rev. No.	Substantive Change(s)
1.3	• Device is now available in 150 MHz versions. Updated specs where necessary to reflect this improvement. • Added 2 new part numbers to Table 6: MCF5270CVM150 and MCF5271CVM150. • Removed features list. This information can be found in the MCF5271RM. • Removed SDRAM address multiplexing section. This information can be found in the MCF5271RM.
1.4	• Added Section 5.2.1, “Supply Voltage Sequencing and Separation Cautions.” • Updated 196MAPBGA package dimensions, Figure 4.
2	• Table 2: Changed SD_CKE pin location from 139 to “—” for the 160QFP device. • Table 2: Changed QSPI_CS1 pin location from “—” to 139 for the 160QFP device. • Table 2: Changed DT3IN pin’s alternate 2 function from “—” to QSPI_CS2. • Table 2: Changed DT3OUT pin’s alternate 2 function from “—” to QSPI_CS3. • Figure 5: Changed pin 139 label from “SD_CKE/QSPI_CS1” to “QSPI_CS1/SD_CKE”. • Removed second sentence from Section 7.10.1, “MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK),” and Section 7.10.2, “MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK),” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 7.10.2, “MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK),” as this feature is not supported on this device.
3	• Section 5.2.1, “Supply Voltage Sequencing and Separation Cautions” changed $PLLV_{DD}$ to V_{DDPLL} to match rest of document. • Section 5.2.1, “Supply Voltage Sequencing and Separation Cautions” Changed V_{DDPLL} voltage level from 1.5V to 3.3V throughout section. • Section 5.2.1.1, “Power Up Sequence” first bullet, changed “Use 1 µs” to “Use 1 ms”. • Corrected position of spec D5 in Figure 11. • Figure 3: Corrected M4 ball location from DATA5 to DATA6, changed DATA*n* labels to D*n* for consistency • Table 14: Added $\overline{\text{DACK}}n$ and $\overline{\text{DREQ}}n$ to footnote. • Table 9, added PLL supply voltage row
4	• Added part number MCF5270CAB100 in Table 6

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