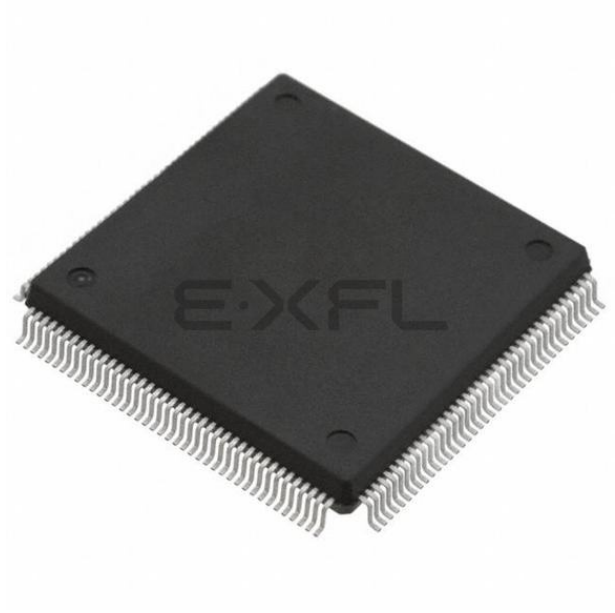

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Coldfire V2 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | EBI/EMI, Ethernet, I²C, SPI, UART/USART |
| Peripherals | DMA, WDT |
| Number of I/O | 39 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.4V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 160-BQFP |
| Supplier Device Package | 160-QFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5271cab100 |

# 1 MCF5271 Family Configurations

**Table 1. MCF5271 Family Configurations**

| Module | MCF5270 | MCF5271 |
|---|---|---|
| ColdFire V2 Core with EMAC and Hardware Divide | x | x |
| System Clock | 150 MHz | |
| Performance (Dhrystone/2.1 MIPS) | 144 | |
| Instruction/Data Cache | 8 Kbytes | |
| Static RAM (SRAM) | 64 Kbytes | |
| Interrupt Controllers (INTC) | 2 | 2 |
| Edge Port Module (EPORT) | x | x |
| External Interface Module (EIM) | x | x |
| 4-channel Direct-Memory Access (DMA) | x | x |
| SDRAM Controller | x | x |
| Fast Ethernet Controller (FEC) | x | x |
| Hardware Encryption | — | x |
| Watchdog Timer (WDT) | x | x |
| Four Periodic Interrupt Timers (PIT) | x | x |
| 32-bit DMA Timers | 4 | 4 |
| QSPI | x | x |
| UART(s) | 3 | 3 |
| $I^2C$ | x | x |
| General Purpose I/O Module (GPIO) | x | x |
| JTAG - IEEE 1149.1 Test Access Port | x | x |
| Package | 160 QFP, 196 MAPBGA | 160 QFP, 196 MAPBGA |

# 2 Block Diagram

The superset device in the MCF5271 family comes in a 196 mold array plastic ball grid array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5271.

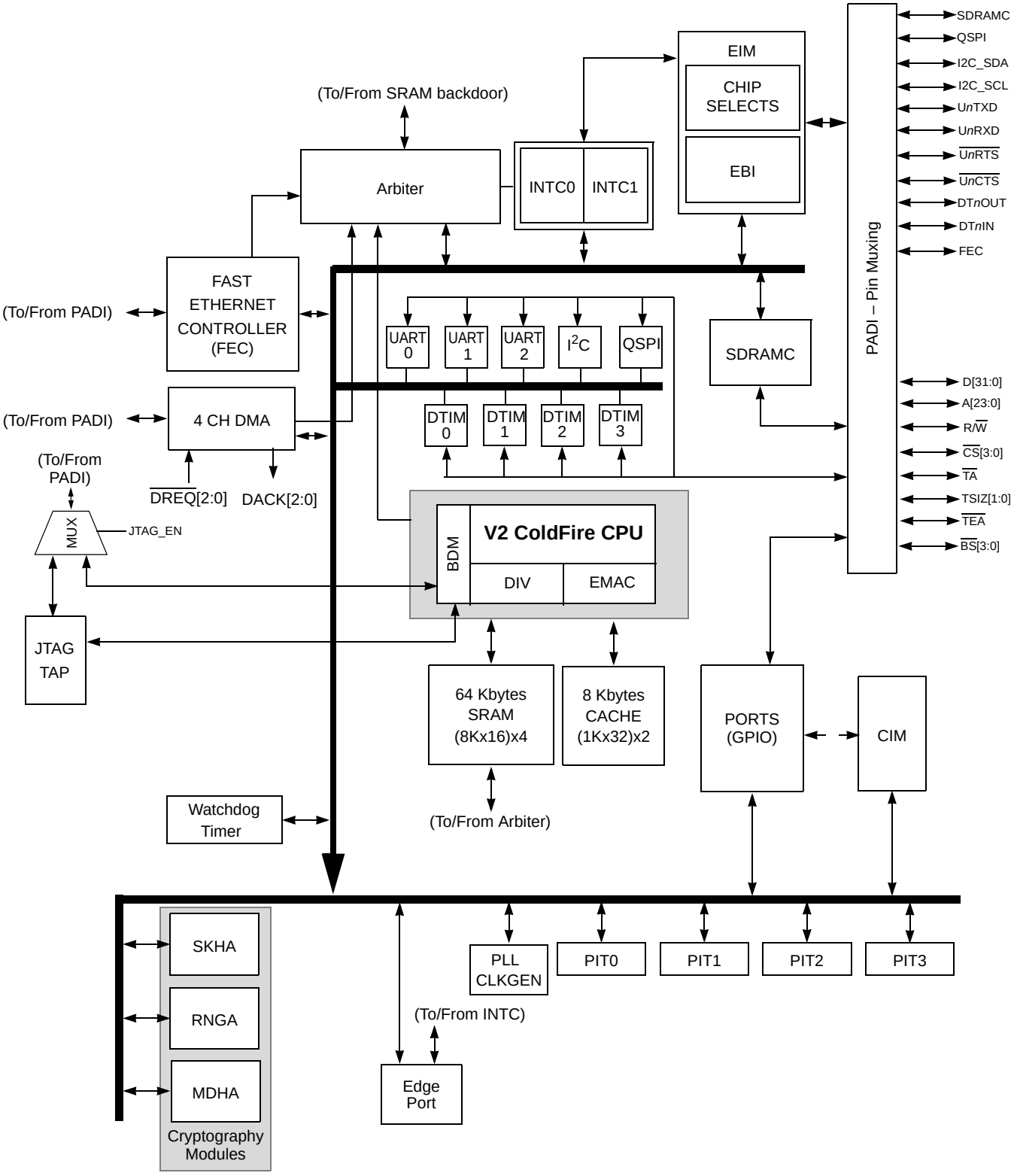


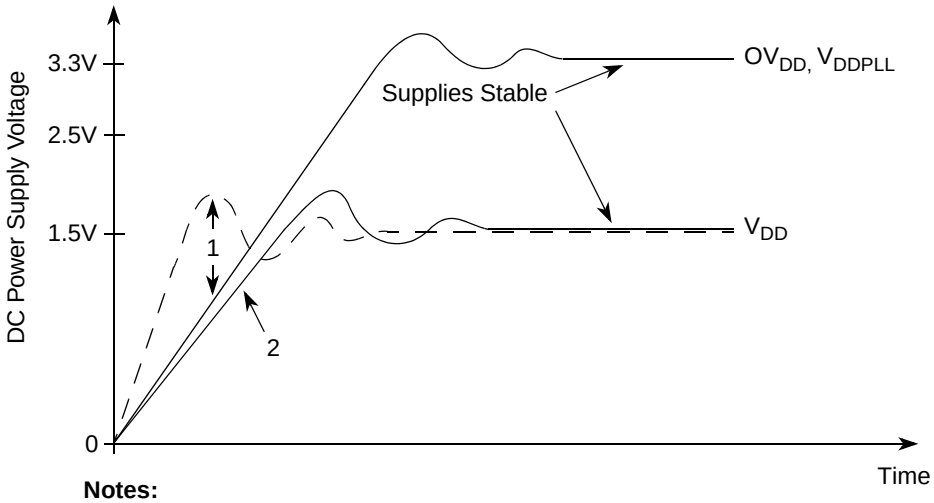

**Figure 1. MCF5271 Block Diagram**

**Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | MCF5270 MCF5271 160 QFP | MCF5270 MCF5271 196 MAPBGA |
|---|---|---|---|---|---|---|
| A[20:0] | — | — | — | O | 123:115, 112:106, 102:98 | A12, B12, C12, A13, B13, B14, C13, C14, D12, D13, D14, E11, E12, E13, E14, F12, F13, F14, G11, G12, G13 |
| D[31:16] | — | — | — | O | 22:30, 33:39 | G1, G2, H1, H2, H3, H4, J1, J2, J3, J4, K1, K2, K3, K4, L1, L2 |
| D[15:8] | PDATAH[7:0] | — | — | O | 42:49 | M1, N1, M2, N2, P2, L3, M3, N3 |
| D[7:0] | PDATAL[7:0] | — | — | O | 50:52, 56:60 | P3, M4, N4, P4, L5, M5, N5, P5 |
| $\overline{BS}$[3:0] | PBS[7:4] | $\overline{CAS}$[3:0] | — | O | 143:140 | B6, C6, D7, C7 |
| $\overline{OE}$ | PBUSCTL7 | — | — | O | 62 | N6 |
| $\overline{TA}$ | PBUSCTL6 | — | — | I | 96 | H11 |
| $\overline{TEA}$ | PBUSCTL5 | $\overline{DREQ1}$ | — | I | — | J14 |
| R/$\overline{W}$ | PBUSCTL4 | — | — | O | 95 | J13 |
| $\overline{TSIZ1}$ | PBUSCTL3 | DACK1 | — | O | — | P6 |
| $\overline{TSIZ0}$ | PBUSCTL2 | DACK0 | — | O | — | P7 |
| $\overline{TS}$ | PBUSCTL1 | DACK2 | — | O | 97 | H13 |
| $\overline{TIP}$ | PBUSCTL0 | DREQ0 | — | O | — | H12 |
| **Chip Selects** | | | | | | |
| $\overline{CS}$[7:4] | PCS[7:4] | — | — | O | — | B9, A10, C10, A11 |
| $\overline{CS}$[3:2] | PCS[3:2] | SD_CS[1:0] | — | O | 132,131 | A9, C9 |
| $\overline{CS1}$ | PCS1 | — | — | O | 130 | B10 |
| $\overline{CS0}$ | — | — | — | O | 129 | D10 |
| **SDRAM Controller** | | | | | | |
| $\overline{SD\_WE}$ | PSDRAM5 | — | — | O | 92 | K13 |
| $\overline{SD\_SCAS}$ | PSDRAM4 | — | — | O | 91 | K12 |
| $\overline{SD\_SRAS}$ | PSDRAM3 | — | — | O | 90 | K11 |
| SD_CKE | PSDRAM2 | — | — | O | — | E8 |
| $\overline{SD\_CS}$[1:0] | PSDRAM[1:0] | — | — | O | — | L12, L13 |

### 5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O $V_{DD}$ ($OV_{DD}$), PLL $V_{DD}$ ($V_{DDPLL}$), and Core $V_{DD}$ ($V_{DD}$). $OV_{DD}$ is specified relative to $V_{DD}$.




**Notes:**
1. VDD should not exceed OVDD or VDDPLL by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/VDDPLL up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, VDD, or VDDPLL) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

**Figure 2. Supply Voltage Sequencing and Separation Cautions**

#### 5.2.1.1 Power Up Sequence

If $OV_{DD}$ is powered up with $V_{DD}$ at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the $OV_{DD}$ to be in a high impedance state. There is no limit on how long after $OV_{DD}$ powers up before $V_{DD}$ must power up. $V_{DD}$ should not lead the $OV_{DD}$ or $V_{DDPLL}$ by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 μs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 ms or slower rise time for all supplies.
2. $V_{DD}$ and $OV_{DD}$/$V_{DDPLL}$ should track up to 0.9 V, then separate for the completion of ramps with $OV_{DD}$ going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

#### 5.2.1.2 Power Down Sequence

If $V_{DD}$ is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after $V_{DD}$ powers down before $OV_{DD}$/$V_{DDPLL}$ must power down. $V_{DD}$ should not lag $OV_{DD}$ or $V_{DDPLL}$ going low by more than 0.4 V during power down or there

**Table 3. Synchronous DRAM Signal Connections**

| Signal | Description |
|---|---|
| $\overline{\text{SD\_SRAS}}$ | Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SD\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals. |
| $\overline{\text{SD\_SCAS}}$ | Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM. |
| $\overline{\text{DRAMW}}$ | DRAM read/write. Asserted for write operations and negated for read operations. |
| $\overline{\text{SD\_CS}}$[1:0] | Row address strobe. Select each memory block of SDRAMs connected to the MCF5271. One $\overline{\text{SD\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals. |
| SD_CKE | Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality. |
| $\overline{\text{BS}}$[3:0] | Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs. |
| CLKOUT | Bus clock output. Connects to the CLK input of SDRAMs. |

#### 5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5271 Reference Manual* for details on address multiplexing.

### 5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

**Table 4. MII Mode**

| Signal Description | MCF5271 Pin |
|---|---|
| Transmit clock | ETXCLK |
| Transmit enable | ETXEN |
| Transmit data | ETXD[3:0] |
| Transmit error | ETXER |
| Collision | ECOL |
| Carrier sense | ECRS |
| Receive clock | ERXCLK |
| Receive enable | ERXDV |
| Receive data | ERXD[3:0] |

**Table 4. MII Mode (continued)**

| Signal Description | MCF5271 Pin |
|---|---|
| Receive error | ERXER |
| Management channel clock | EMDC |
| Management channel serial data | EMDIO |

The serial mode interface operates in what is generally referred to as AMD mode. The MCF5271 configuration for seven-wire serial mode connections to the external transceiver are shown in Table 5.

**Table 5. Seven-Wire Mode Configuration**

| Signal Description | MCF5271 Pin |
|---|---|
| Transmit clock | ETXCLK |
| Transmit enable | ETXEN |
| Transmit data | ETXD[0] |
| Collision | ECOL |
| Receive clock | ERXCLK |
| Receive enable | ERXDV |
| Receive data | ERXD[0] |
| Unused, configure as PB14 | ERXER |
| Unused input, tie to ground | ECRS |
| Unused, configure as PB[13:11] | ERXD[3:1] |
| Unused output, ignore | ETXER |
| Unused, configure as PB[10:8] | ETXD[3:1] |
| Unused, configure as PB15 | EMDC |
| Input after reset, connect to ground | EMDIO |

Refer to the M5271EVB evaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5271 site by navigating to: http://www.freescale.com/coldfire.

### 5.7.3 BDM

Use the BDM interface as shown in the M5271EVB evaluation board user's manual. The schematics for this board are accessible at the Freescale website at: http://www.freescale.com/coldfire.

# 6 Mechanicals/Pinouts and Part Numbers

This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF5271 devices. See Table 4 for a list the signal names and pin locations for each device.

## 6.5 Ordering Information

**Table 6. Orderable Part Numbers**

| Freescale Part Number | Description | Package | Speed | Lead-Free? | Temperature |
|---|---|---|---|---|---|
| MCF5270AB100 | MCF5270 RISC Microprocessor | 160 QFP | 100MHz | Yes | 0° to +70° C |
| MCF5270CAB100 | MCF5270 RISC Microprocessor | 160 QFP | 100MHz | Yes | -40° to +85° C |
| MCF5270VM100 | MCF5270 RISC Microprocessor | 196 MAPBGA | 100MHz | Yes | 0° to +70° C |
| MCF5270CVM150 | MCF5270 RISC Microprocessor | 196 MAPBGA | 150MHz | Yes | -40° to +85° C |
| MCF5271CAB100 | MCF5271 RISC Microprocessor | 160 QFP | 100MHz | Yes | -40° to +85° C |
| MCF5271CVM100 | MCF5271 RISC Microprocessor | 196 MAPBGA | 100MHz | Yes | -40° to +85° C |
| MCF5271CVM150 | MCF5271 RISC Microprocessor | 196 MAPBGA | 150MHz | Yes | -40° to +85° C |

# 7 Electrical Characteristics

This chapter contains electrical specification tables and reference timing diagrams for the MCF5271 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5271.

**NOTE**

The parameters specified in this processor document supersede any values found in the module specifications.

## 7.1 Maximum Ratings

**Table 7. Absolute Maximum Ratings[1, 2]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | – 0.5 to +2.0 | V |
| Pad Supply Voltage | $OV_{DD}$ | – 0.3 to +4.0 | V |
| PLL Supply Voltage | $V_{DDPLL}$ | – 0.3 to +4.0 | V |
| Digital Input Voltage [3] | $V_{IN}$ | – 0.3 to + 4.0 | V |
| Instantaneous Maximum Current Single pin limit (applies to all pins) [3,4,5] | $I_D$ | 25 | mA |
| Operating Temperature Range (Packaged) | $T_A$ ($T_L$ - $T_H$) | – 40 to 85 | °C |
| Storage Temperature Range | $T_{stg}$ | – 65 to 150 | °C |

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $OV_{DD}$).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to $V_{SS}$ and $OV_{DD}$.

5 Power supply must maintain regulation within operating $OV_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > OV_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $OV_{DD}$ and could result in external power supply going out of regulation. Insure external $OV_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power (ex; no clock).Power supply must maintain regulation within operating $OV_{DD}$ range during instantaneous and operating maximum current conditions.

## 7.2 Thermal Characteristics

The below table lists thermal resistance values.

**Table 8. Thermal Characteristics**

| Characteristic | | Symbol | 196 MAPBGA | 160QFP | Unit |
|---|---|---|---|---|---|
| Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JMA}$ | 32[1,2] | 40[1,2] | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 29[1,2] | 36[1,2] | °C/W |
| Junction to board | | $\theta_{JB}$ | 20[3] | 25[3] | °C/W |
| Junction to case | | $\theta_{JC}$ | 10[4] | 10[4] | °C/W |
| Junction to top of package | | $\Psi_{jt}$ | 2[1,5] | 2[1,5] | °C/W |
| Maximum operating junction temperature | | $T_j$ | 104 | 105 | °C |

1 $\theta_{JMA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Motorola recommends the use of $\theta_{JmA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature ($T_J$) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

$T_A$= Ambient Temperature, °C

$\Theta_{JMA}$= Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

## 7.3 DC Electrical Specifications

**Table 9. DC Electrical Specifications[1]**

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | 1.4 | — | 1.6 | V |
| Pad Supply Voltage | $OV_{DD}$ | 3.0 | — | 3.6 | V |
| PLL Supply Voltage | $V_{DDPLL}$ | 3.0 | — | 3.6 | V |
| Input High Voltage | $V_{IH}$ | $0.7 \times OV_{DD}$ | — | 3.65 | V |
| Input Low Voltage | $V_{IL}$ | $V_{SS} - 0.3$ | — | $0.35 \times OV_{DD}$ | V |
| Input Hysteresis | $V_{HYS}$ | $0.06 \times OV_{DD}$ | — | — | mV |
| Input Leakage Current<br>$V_{in} = V_{DD}$ or $V_{SS}$, Input-only pins | $I_{in}$ | –1.0 | — | 1.0 | µA |
| High Impedance (Off-State) Leakage Current<br>$V_{in} = V_{DD}$ or $V_{SS}$, All input/output and output pins | $I_{OZ}$ | –1.0 | — | 1.0 | µA |
| Output High Voltage (All input/output and all output pins)<br>$I_{OH}$ = –5.0 mA | $V_{OH}$ | $OV_{DD}$ - 0.5 | — | — | V |
| Output Low Voltage (All input/output and all output pins)<br>$I_{OL}$ = 5.0mA | $V_{OL}$ | — | — | 0.5 | V |
| Weak Internal Pull Up Device Current, tested at $V_{IL}$ Max.[2] | $I_{APU}$ | –10 | — | – 130 | µA |
| Input Capacitance [3]<br>All input-only pins<br>All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | — | <br>7<br>7 | pF |

**Table 9. DC Electrical Specifications[1] (continued)**

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Load Capacitance[4]<br>Low drive strength<br>High drive strength | $C_L$ | | —<br>— | 25<br>50 | pF<br>pF |
| Core Operating Supply Current [5]<br>Master Mode | $I_{DD}$ | — | 135 | 150 | mA |
| Pad Operating Supply Current<br>Master Mode<br>Low Power Modes | $OI_{DD}$ | —<br>— | 100<br>TBD | —<br>— | mA<br>µA |
| DC Injection Current [3, 6, 7, 8]<br>$V_{NEGCLAMP}$ =$V_{SS}$– 0.3 V, $V_{POSCLAMP}$ = $V_{DD}$ + 0.3<br>Single Pin Limit<br>Total processor Limit, Includes sum of all stressed pins | $I_{IC}$ | <br><br>–1.0<br>–10 | | <br><br>1.0<br>10 | <br><br>mA<br>mA |

1 Refer to Table 10 for additional PLL specifications.
2 Refer to the MCF5271 signals section for pins having weak internal pull-up devices.
3 This parameter is characterized before qualification rather than 100% tested.
4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination. See High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson for design guidelines.
5 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.
6 All functional non-supply pins are internally clamped to $V_{SS}$ and their respective $V_{DD}$.
7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
8 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Insure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

## 7.4 Oscillator and PLLMRFM Electrical Characteristics

**Table 10. HiP7 PLLMRFM Electrical Specifications[1]**

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|---|---|---|---|---|---|
| 1 | PLL Reference Frequency Range<br>Crystal reference<br>External reference<br>1:1 mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$) | <br>$f_{ref\_crystal}$<br>$f_{ref\_ext}$<br>$f_{ref\_1:1}$ | <br>8<br>8<br>24 | <br>25<br>25<br>75 | MHz |
| 2 | Core frequency<br>CLKOUT Frequency [2]<br>External reference<br>On-Chip PLL Frequency | $f_{sys}$<br><br>$f_{sys/2}$ | <br>0<br>$f_{ref} \div 32$ | 150<br>75<br>75 | MHz<br>MHz<br>MHz |
| 3 | Loss of Reference Frequency [3, 5] | $f_{LOR}$ | 100 | 1000 | kHz |
| 4 | Self Clocked Mode Frequency [4, 5] | $f_{SCM}$ | 10.25 | 15.25 | MHz |
| 5 | Crystal Start-up Time [5, 6] | $t_{cst}$ | — | 10 | ms |

**Table 10. HiP7 PLLMRFM Electrical Specifications[1] (continued)**

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|---|---|---|---|---|---|
| 6 | XTAL Load Capacitance[5] | | 5 | 30 | pF |
| 7 | PLL Lock Time [5, 7,13] | $t_{lpll}$ | — | 750 | µs |
| 8 | Power-up To Lock Time [5, 6,8]<br>With Crystal Reference (includes 5 time)<br>Without Crystal Reference[9] | $t_{lplk}$ | <br>—<br>— | <br>11<br>750 | <br>ms<br>µs |
| 9 | 1:1 Mode Clock Skew (between CLKOUT and EXTAL) [10] | $t_{skew}$ | –1 | 1 | ns |
| 10 | Duty Cycle of reference [5] | $t_{dc}$ | 40 | 60 | % |
| 11 | Frequency un-LOCK Range | $f_{UL}$ | –3.8 | 4.1 | % $f_{sys/2}$ |
| 12 | Frequency LOCK Range | $f_{LCK}$ | –1.7 | 2.0 | % $f_{sys/2}$ |
| 13 | CLKOUT Period Jitter, [5, 6, 8,11, 12]<br>Measured at $f_{sys/2}$ Max<br>Peak-to-peak Jitter (Clock edge to clock edge)<br>Long Term Jitter (Averaged over 2 ms interval) | $C_{jitter}$ | <br>—<br>— | <br>5.0<br>.01 | % $f_{sys/2}$ |
| 14 | Frequency Modulation Range Limit[13,14] ($f_{sys/2}$ Max must not be exceeded) | $C_{mod}$ | 0.8 | 2.2 | %$f_{sys/2}$ |
| 15 | ICO Frequency. $f_{ico} = f_{ref} \times 2 \times (MFD+2)$ [15] | $f_{ico}$ | 48 | 150 | MHz |

1 All values given are initial design targets and subject to change.
2 All internal registers retain data at 0 Hz.
3 “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.
4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below $f_{LOR}$ with default MFD/RFD settings.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 Proper PC board layout procedures must be followed to achieve specifications.
7 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
8 Assuming a reference is available at power up, lock time is measured from the time $V_{DD}$ and $V_{DDSYN}$ are valid to $\overline{\text{RSTOUT}}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
9 $t_{lpll} = (64 * 4 * 5 + 5\ \tau)\ T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6}\ 2(MFD + 2)$.
10 PLL is operating in 1:1 PLL mode.
11 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DDSYN}$ and $V_{SSSYN}$ and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.
12 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.
13 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100KHz.
14 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.
15 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

Timings listed in Table 11 are shown in Figure 7.

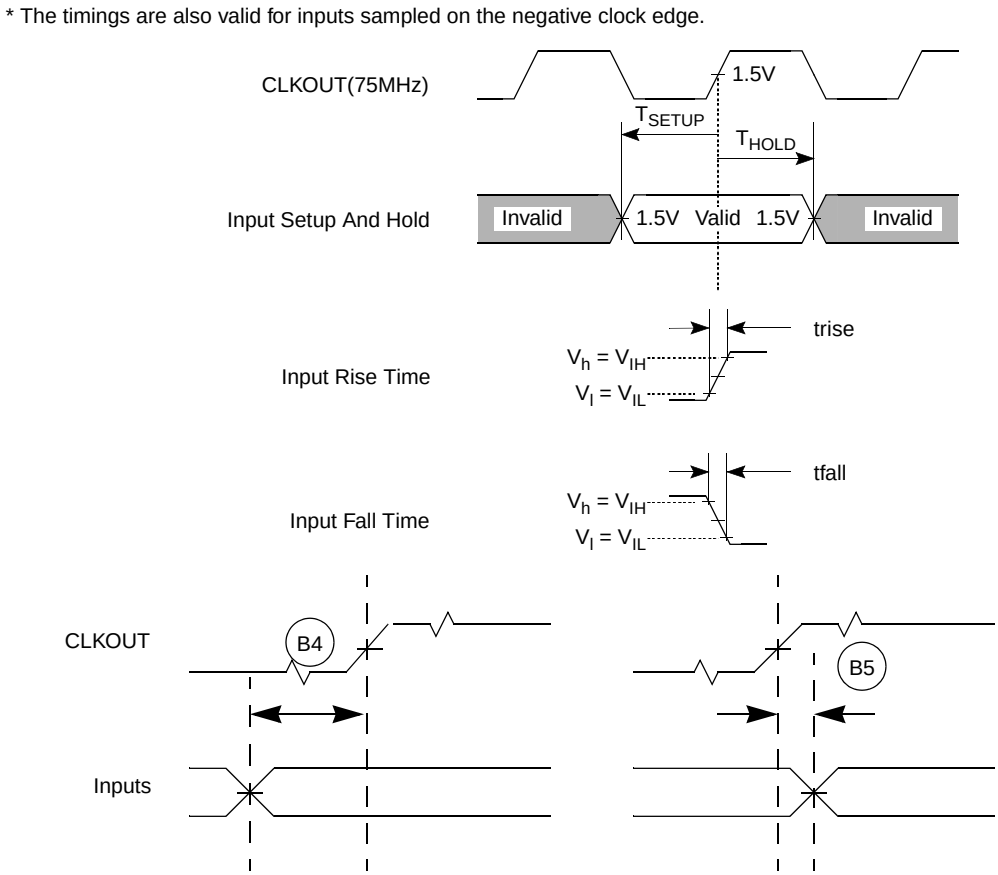



**Figure 7. General Input Timing Requirements**

## 7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

**Table 12. External Bus Output Timing Specifications**

| Name | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **Control Outputs** | | | | | |
| B6a | CLKOUT high to chip selects valid [1] | $t_{CHCV}$ | — | $0.5t_{CYC}$ +5 | ns |
| B6b | CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2] | $t_{CHBV}$ | — | $0.5t_{CYC}$ +5 | ns |
| B6c | CLKOUT high to output enable ($\overline{OE}$) valid[3] | $t_{CHOV}$ | — | $0.5t_{CYC}$ +5 | ns |
| B7 | CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid | $t_{CHCOI}$ | $0.5t_{CYC}$+1.5 | — | ns |
| B7a | CLKOUT high to chip selects invalid | $t_{CHCI}$ | $0.5t_{CYC}$+1.5 | — | ns |

Read/write bus timings listed in Table 12 are shown in Figure 8, Figure 9, and Figure 10.

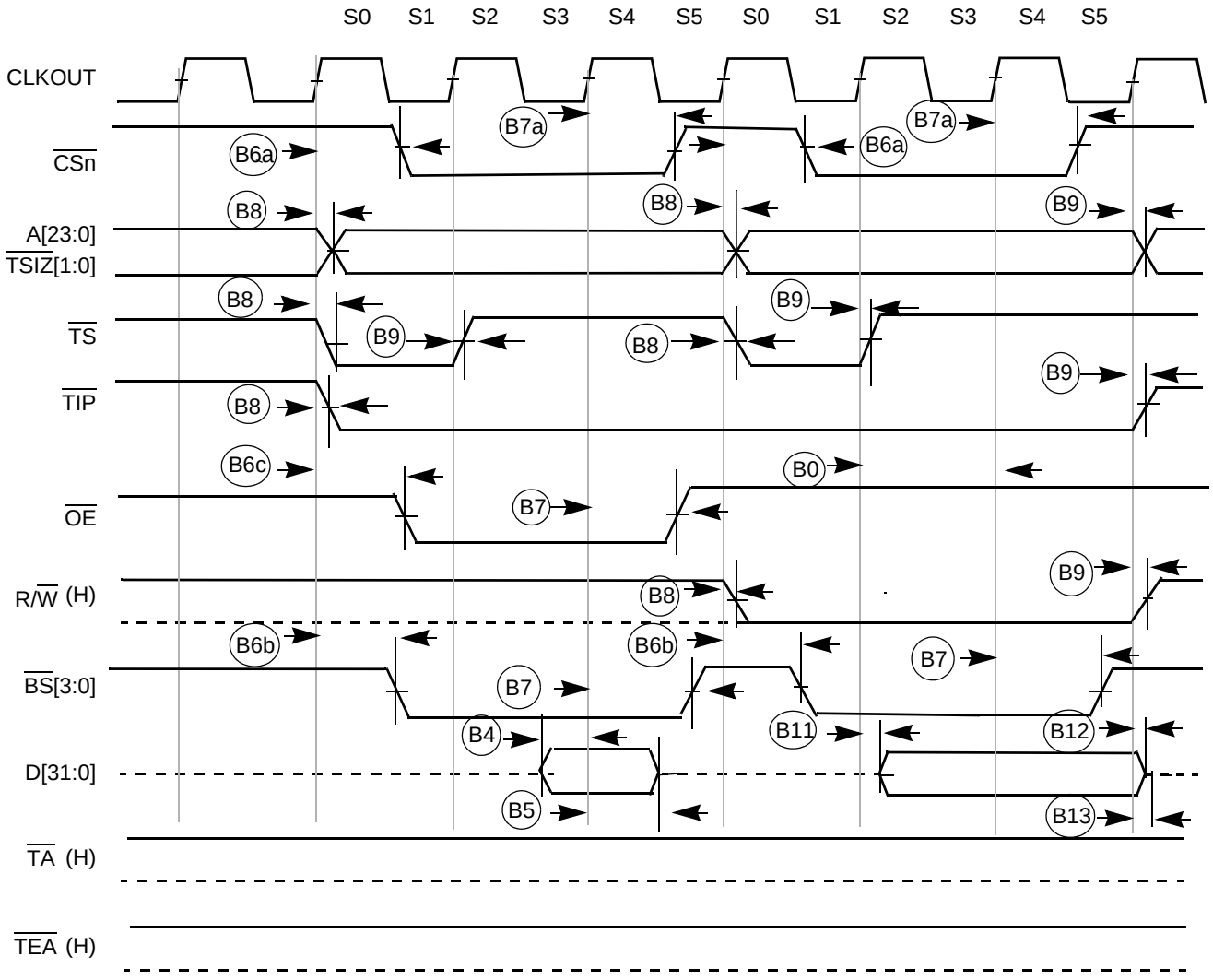



**Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing**

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 12.

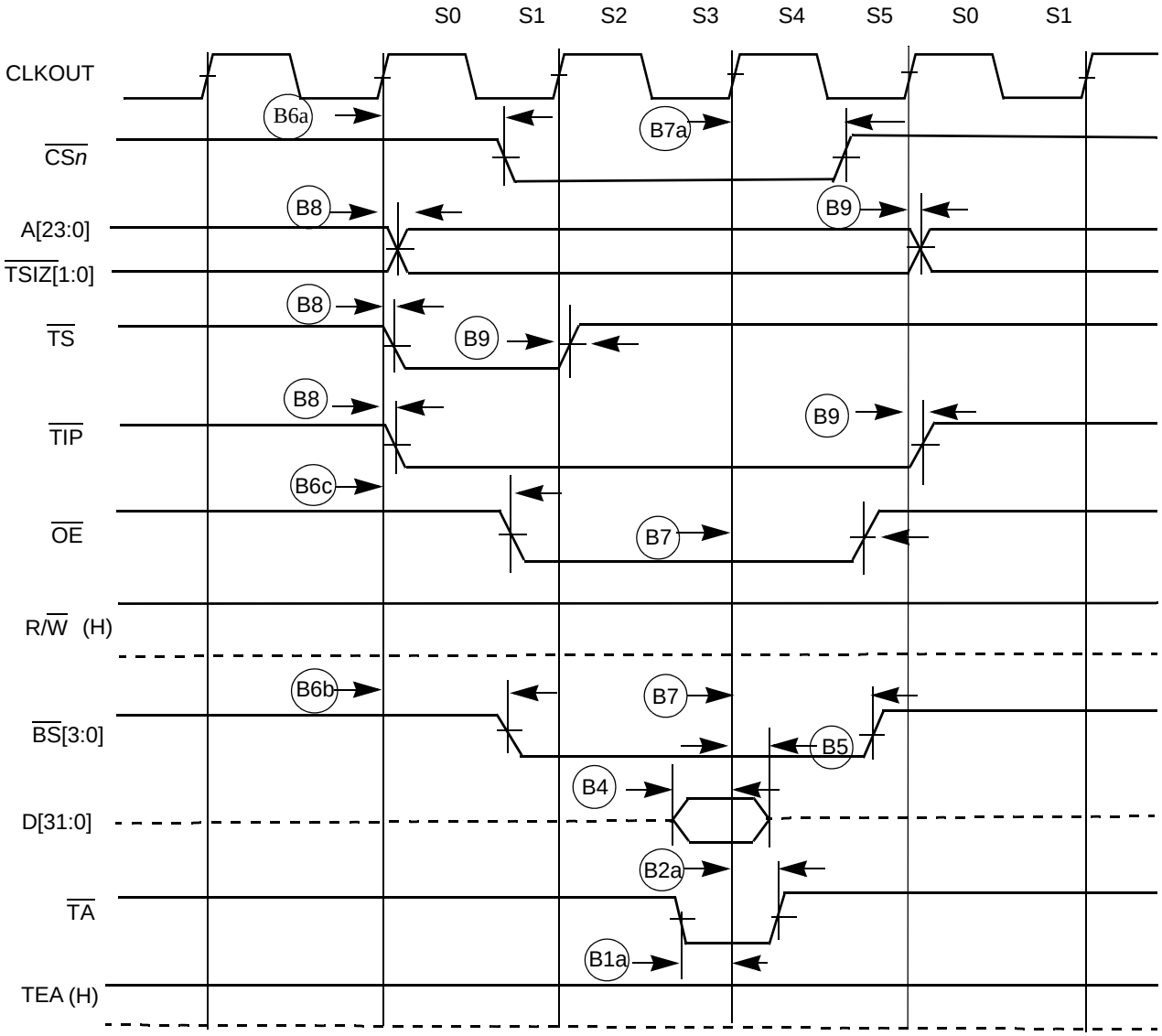



**Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$**

Figure 10 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 12.

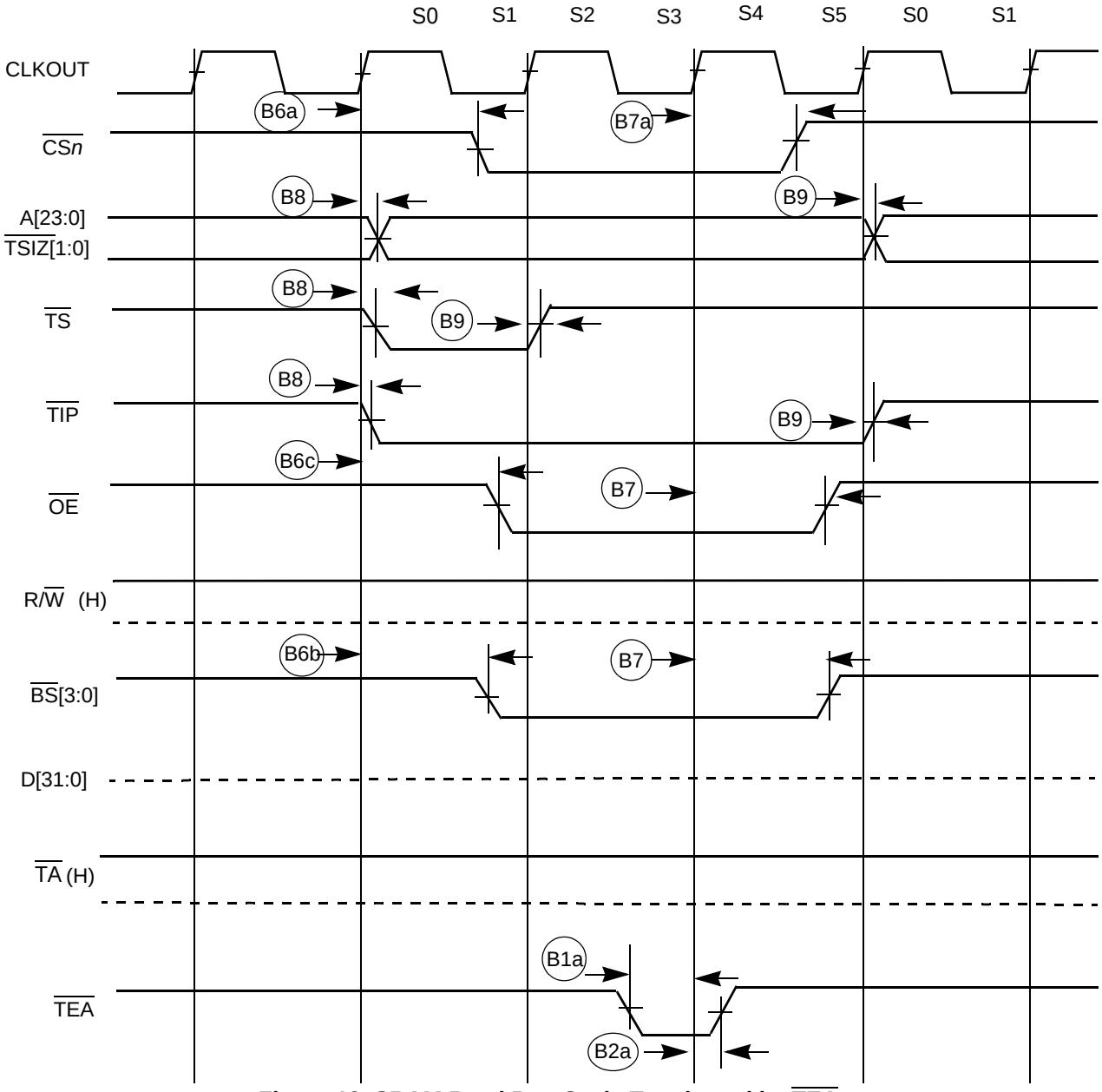



**Figure 10. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$**

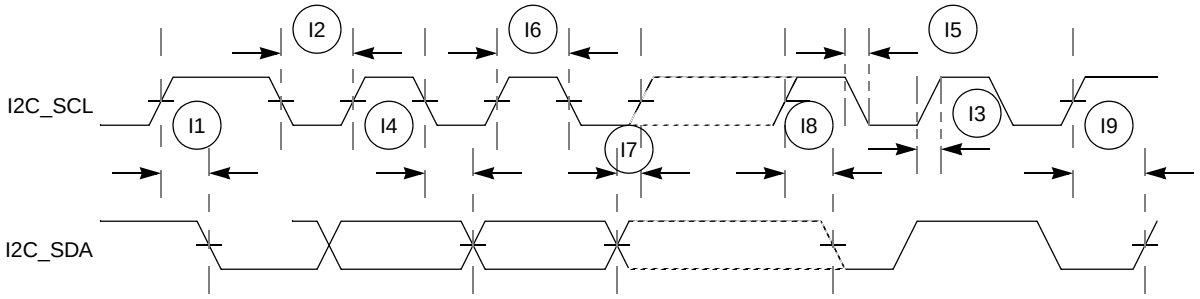



**Figure 15. I²C Input/Output Timings**

## 7.10 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

### 7.10.1 MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)

The receiver functions correctly up to a ERXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ERXCLK frequency.

Table 18 lists MII receive channel timings.

**Table 18. MII Receive Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M1 | ERXD[3:0], ERXDV, ERXER to ERXCLK setup | 5 | — | ns |
| M2 | ERXCLK to ERXD[3:0], ERXDV, ERXER hold | 5 | — | ns |
| M3 | ERXCLK pulse width high | 35% | 65% | ERXCLK period |
| M4 | ERXCLK pulse width low | 35% | 65% | ERXCLK period |

Figure 16 shows MII receive signal timings listed in Table 18.

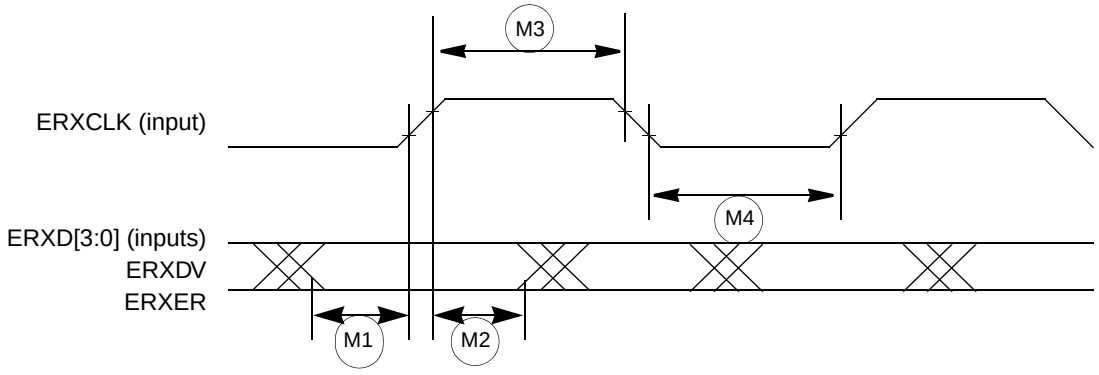



**Figure 16. MII Receive Signal Timing Diagram**

## 7.13 JTAG and Boundary Scan Timing

**Table 24. JTAG and Boundary Scan Timing**

| Num | Characteristics[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| J1 | TCLK Frequency of Operation | $f_{JCYC}$ | DC | 1/4 | $f_{sys/2}$ |
| J2 | TCLK Cycle Period | $t_{JCYC}$ | 4 | — | $t_{CYC}$ |
| J3 | TCLK Clock Pulse Width | $t_{JCW}$ | 26 | — | ns |
| J4 | TCLK Rise and Fall Times | $t_{JCRF}$ | 0 | 3 | ns |
| J5 | Boundary Scan Input Data Setup Time to TCLK Rise | $t_{BSDST}$ | 4 | — | ns |
| J6 | Boundary Scan Input Data Hold Time after TCLK Rise | $t_{BSDHT}$ | 26 | — | ns |
| J7 | TCLK Low to Boundary Scan Output Data Valid | $t_{BSDV}$ | 0 | 33 | ns |
| J8 | TCLK Low to Boundary Scan Output High Z | $t_{BSDZ}$ | 0 | 33 | ns |
| J9 | TMS, TDI Input Data Setup Time to TCLK Rise | $t_{TAPBST}$ | 4 | — | ns |
| J10 | TMS, TDI Input Data Hold Time after TCLK Rise | $t_{TAPBHT}$ | 10 | — | ns |
| J11 | TCLK Low to TDO Data Valid | $t_{TDODV}$ | 0 | 26 | ns |
| J12 | TCLK Low to TDO High Z | $t_{TDODZ}$ | 0 | 8 | ns |
| J13 | $\overline{TRST}$ Assert Time | $t_{TRSTAT}$ | 100 | — | ns |
| J14 | $\overline{TRST}$ Setup Time (Negation) to TCLK High | $t_{TRSTST}$ | 10 | — | ns |

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

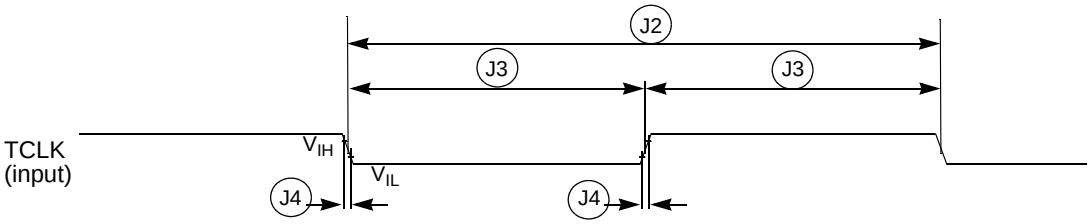



**Figure 21. Test Clock Input Timing**

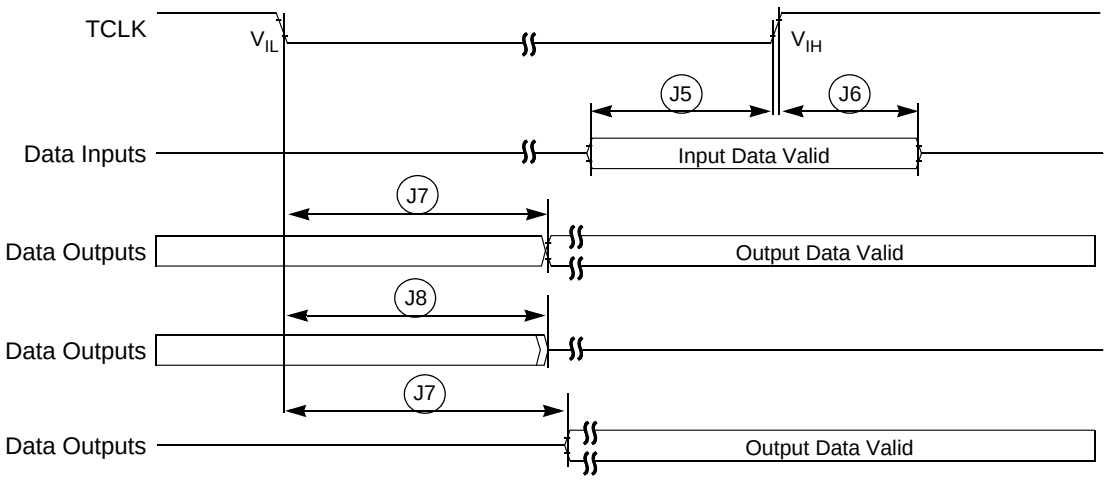



**Figure 22. Boundary Scan (JTAG) Timing**

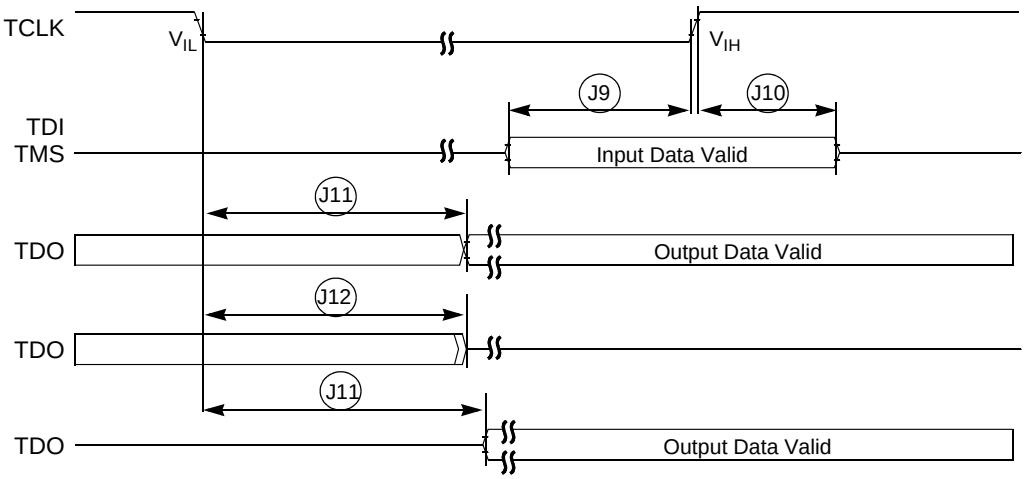



**Figure 23. Test Access Port Timing**

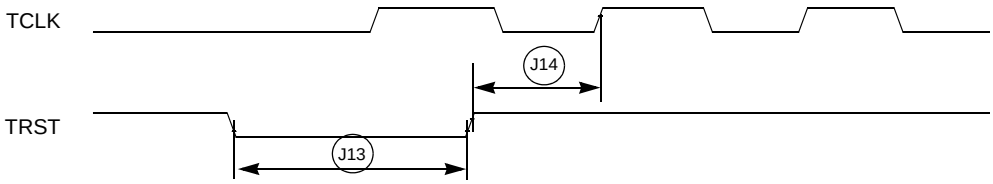



**Figure 24. $\overline{\text{TRST}}$ Timing**

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