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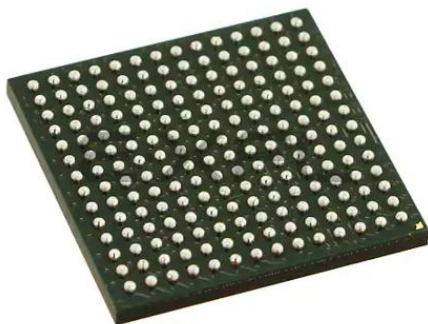
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	97
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5271cvm150j

1 MCF5271 Family Configurations

Table 1. MCF5271 Family Configurations

Module	MCF5270	MCF5271
ColdFire V2 Core with EMAC and Hardware Divide	x	x
System Clock	150 MHz	
Performance (Dhrystone/2.1 MIPS)	144	
Instruction/Data Cache	8 Kbytes	
Static RAM (SRAM)	64 Kbytes	
Interrupt Controllers (INTC)	2	2
Edge Port Module (EPORT)	x	x
External Interface Module (EIM)	x	x
4-channel Direct-Memory Access (DMA)	x	x
SDRAM Controller	x	x
Fast Ethernet Controller (FEC)	x	x
Hardware Encryption	—	x
Watchdog Timer (WDT)	x	x
Four Periodic Interrupt Timers (PIT)	x	x
32-bit DMA Timers	4	4
QSPI	x	x
UART(s)	3	3
I^2C	x	x
General Purpose I/O Module (GPIO)	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x
Package	160 QFP, 196 MAPBGA	160 QFP, 196 MAPBGA

2 Block Diagram

The superset device in the MCF5271 family comes in a 196 mold array plastic ball grid array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5271.

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3 Features

For a detailed feature list see the MCF5271 Reference Manual (MCF5271RM).

4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF5271 signals, consult the *MCF5271 Reference Manual* (MCF5271RM).

4.1 Signal Properties

Table 4 lists all of the signals grouped by function. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts and Part Numbers," for package diagrams.

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 2. MCF5270 and MCF5271 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
Reset						
$\overline{\text{RESET}}$	—	—	—	I	83	N13
$\overline{\text{RSTOUT}}$	—	—	—	O	82	P13
Clock						
EXTAL	—	—	—	I	86	M14
XTAL	—	—	—	O	85	N14
CLKOUT	—	—	—	O	89	K14
Mode Selection						
CLKMOD[1:0]	—	—	—	I	20,21	G5,H5
$\overline{\text{RCON}}$	—	—	—	I	79	K10
External Memory Interface and Ports						
A[23:21]	PADDR[7:5]	$\overline{\text{CS}}$[6:4]	—	O	126, 125, 124	B11, C11, D11

Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
A[20:0]	—	—	—	O	123:115, 112:106, 102:98	A12, B12, C12, A13, B13, B14, C13, C14, D12, D13, D14, E11, E12, E13, E14, F12, F13, F14, G11, G12, G13
D[31:16]	—	—	—	O	22:30, 33:39	G1, G2, H1, H2, H3, H4, J1, J2, J3, J4, K1, K2, K3, K4, L1, L2
D[15:8]	PDATAH[7:0]	—	—	O	42:49	M1, N1, M2, N2, P2, L3, M3, N3
D[7:0]	PDATAL[7:0]	—	—	O	50:52, 56:60	P3, M4, N4, P4, L5, M5, N5, P5
$\overline{BS}$[3:0]	PBS[7:4]	$\overline{CAS}$[3:0]	—	O	143:140	B6, C6, D7, C7
$\overline{OE}$	PBUSCTL7	—	—	O	62	N6
$\overline{TA}$	PBUSCTL6	—	—	I	96	H11
$\overline{TEA}$	PBUSCTL5	$\overline{DREQ1}$	—	I	—	J14
R/$\overline{W}$	PBUSCTL4	—	—	O	95	J13
$\overline{TSIZ1}$	PBUSCTL3	DACK1	—	O	—	P6
$\overline{TSIZ0}$	PBUSCTL2	DACK0	—	O	—	P7
$\overline{TS}$	PBUSCTL1	DACK2	—	O	97	H13
$\overline{TIP}$	PBUSCTL0	DREQ0	—	O	—	H12
Chip Selects						
$\overline{CS}$[7:4]	PCS[7:4]	—	—	O	—	B9, A10, C10, A11
$\overline{CS}$[3:2]	PCS[3:2]	SD_CS[1:0]	—	O	132,131	A9, C9
$\overline{CS1}$	PCS1	—	—	O	130	B10
$\overline{CS0}$	—	—	—	O	129	D10
SDRAM Controller						
$\overline{SD\_WE}$	PSDRAM5	—	—	O	92	K13
$\overline{SD\_SCAS}$	PSDRAM4	—	—	O	91	K12
$\overline{SD\_SRAS}$	PSDRAM3	—	—	O	90	K11
SD_CKE	PSDRAM2	—	—	O	—	E8
$\overline{SD\_CS}$[1:0]	PSDRAM[1:0]	—	—	O	—	L12, L13

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Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
External Interrupts Port						
$\overline{\text{IRQ}}$[7:3]	PIRQ[7:3]	—	—	I	IRQ7=63 IRQ4=64	N7, M7, L7, P8, N8
$\overline{\text{IRQ2}}$	PIRQ2	$\overline{\text{DREQ2}}$	—	I	—	M8
$\overline{\text{IRQ1}}$	PIRQ1	—	—	I	65	L8
FEC						
EMDC	PFECI2C3	I2C_SCL	U2TXD	O	151	D4
EMDIO	PFECI2C2	I2C_SDA	U2RXD	I/O	150	D5
ECOL	—	—	—	I	9	E2
ECRS	—	—	—	I	8	E1
ERXCLK	—	—	—	I	7	D1
ERXDV	—	—	—	I	6	D2
ERXD[3:0]	—	—	—	I	5:2	D3, C1, C2, B1
ERXER	—	—	—	O	159	B2
ETXCLK	—	—	—	I	158	A2
ETXEN	—	—	—	I	157	C3
ETXER	—	—	—	O	156	B3
ETXD[3:0]	—	—	—	O	155:152	A3, A4, C4, B4
I^{2}C						
I2C_SDA	PFECI2C1	—	—	I/O	—	J12
I2C_SCL	PFECI2C0	—	—	I/O	—	J11
DMA						
DACK[2:0] and $\overline{\text{DREQ}}$[2:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and DT2OUT for DACK2, TSIZ1and DT1OUT for DACK1, TSIZ0 and DT0OUT for DACK0, $\overline{\text{IRQ2}}$ and DT2IN for $\overline{\text{DREQ2}}$, $\overline{\text{TEA}}$ and $\overline{\text{DT1IN}}$ for $\overline{\text{DREQ1}}$, and $\overline{\text{TIP}}$ and DT0IN for $\overline{\text{DREQ0}}$.					—	—
QSPI						
QSPI_CS1	PQSPI4	SD_CKE	—	O	139	B7
QSPI_CS0	PQSPI3	—	—	O	146	A6
QSPI_CLK	PQSPI2	I2C_SCL	—	O	147	C5
QSPI_DIN	PQSPI1	I2C_SDA	—	I	148	B5
QSPI_DOUT	PQSPI0	—	—	O	149	A5

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Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
Test						
TEST	—	—	—	I	19	F5
PLL_TEST	—	—	—	I	—	
Power Supplies						
VDDPLL	—	—	—	I	87	M13
VSSPLL	—	—	—	I	84	L14
OVDD	—	—	—	I	1, 18, 32, 41, 55, 69, 81, 94, 105, 114, 128, 138, 145	E5, E7, E10, F7, F9, G6, G8, H7, H8, H9, J6, J8, J10, K5, K6, K8
VSS	—	—	—	I	17, 31, 40, 54, 67, 80, 88, 93, 104, 113, 127, 137, 144, 160	A1, A14, E6, E9, F6, F8, F10, G7, G9, H6, J5, J7, J9, K7, P1, P14
VDD	—	—	—	I	16, 53, 103	D6, F11, G4, L4

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5271.

- See application note AN1259, *System Design and Layout Techniques for Noise Reduction in Processor-Based Systems*.

- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33 μF, 0.1 μF, and 0.01 μF across each power supply

Table 3. Synchronous DRAM Signal Connections

Signal	Description
$\overline{\text{SD\_SRAS}}$	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SD\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals.
$\overline{\text{SD\_SCAS}}$	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM.
$\overline{\text{DRAMW}}$	DRAM read/write. Asserted for write operations and negated for read operations.
$\overline{\text{SD\_CS}}$[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF5271. One $\overline{\text{SD\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
$\overline{\text{BS}}$[3:0]	Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5271 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF5271 Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[3:0]
Transmit error	ETXER
Collision	ECOL
Carrier sense	ECRS
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[3:0]

Table 4. MII Mode (continued)

Signal Description	MCF5271 Pin
Receive error	ERXER
Management channel clock	EMDC
Management channel serial data	EMDIO

The serial mode interface operates in what is generally referred to as AMD mode. The MCF5271 configuration for seven-wire serial mode connections to the external transceiver are shown in Table 5.

Table 5. Seven-Wire Mode Configuration

Signal Description	MCF5271 Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[0]
Collision	ECOL
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[0]
Unused, configure as PB14	ERXER
Unused input, tie to ground	ECRS
Unused, configure as PB[13:11]	ERXD[3:1]
Unused output, ignore	ETXER
Unused, configure as PB[10:8]	ETXD[3:1]
Unused, configure as PB15	EMDC
Input after reset, connect to ground	EMDIO

Refer to the M5271EVB evaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5271 site by navigating to: http://www.freescale.com/coldfire.

5.7.3 BDM

Use the BDM interface as shown in the M5271EVB evaluation board user's manual. The schematics for this board are accessible at the Freescale website at: http://www.freescale.com/coldfire.

6 Mechanicals/Pinouts and Part Numbers

This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF5271 devices. See Table 4 for a list the signal names and pin locations for each device.

6.1   Pinout—196 MAPBGA

The following figure shows a pinout of the MCF5270/71CVMxxx package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	ETXCLK	ETXD3	ETXD2	QSPI_DOUT	QSPI_CS0	U2RXD	U2TXD	$\overline{CS3}$	$\overline{CS6}$	$\overline{CS4}$	A20	A17	VSS	**A**
B	ERXD0	ERXER	ETXER	ETXD0	QSPI_DIN	$\overline{BS3}$	QSPI_CS1	U1CTS	$\overline{CS7}$	$\overline{CS1}$	A23	A19	A16	A15	**B**
C	ERXD2	ERXD1	ETXEN	ETXD1	QSCK	$\overline{BS2}$	$\overline{BS0}$	RTS1	$\overline{CS2}$	$\overline{CS5}$	A22	A18	A14	A13	**C**
D	ERXCLK	ERXDV	ERXD3	EMDC	EMDIO	Core VDD_4	$\overline{BS1}$	U1RXD1	U1TXD	$\overline{CS0}$	A21	A12	A11	A10	**D**
E	ECRS	ECOL	NC	TIN0	VDD	VSS	VDD	SD_CKE	VSS	VDD	A9	A8	A7	A6	**E**
F	U0TXD	U0RXD	U0CTS	DTOUT0	TEST	VSS	VDD	VSS	VDD	VSS	Core VDD_3	A5	A4	A3	**F**
G	D31	D30	U0RTS	Core VDD_1	CLK MOD1	VDD	VSS	VDD	VSS	NC	A2	A1	A0	DTOUT3	**G**
H	D29	D28	D27	D26	CLK MOD0	VSS	VDD	VDD	VDD	NC	$\overline{TA}$	$\overline{TIP}$	$\overline{TS}$	DTIN3	**H**
J	D25	D24	D23	D22	VSS	VDD	VSS	VDD	VSS	VDD	I2C_SCL	I2C_SDA	R/$\overline{W}$	$\overline{TEA}$	**J**
K	D21	D20	D19	D18	VDD	VDD	VSS	VDD	JTAG_EN	$\overline{RCON}$	SD_RAS	SD_CAS	SD_WE	CLKOUT	**K**
L	D17	D16	D10	Core VDD_2	D3	DTIN1	$\overline{IRQ5}$	$\overline{IRQ1}$	DTOUT2	PST0	DDATA0	SD_CS1	SD_CS0	VSSPLL	**L**
M	D15	D13	D9	D6	D2	DTOUT1	$\overline{IRQ6}$	$\overline{IRQ2}$	DTIN2	TDI/DSI	PST3	DDATA3	VDDPLL	EXTAL	**M**
N	D14	D12	D8	D5	D1	$\overline{OE}$	$\overline{IRQ7}$	$\overline{IRQ3}$	$\overline{TRST}$/ DSCLK	TDO/DSO	PST2	DDATA2	$\overline{RESET}$	XTAL	**N**
P	VSS	D11	D7	D4	D0	TSIZ1	TSIZ0	$\overline{IRQ4}$	TCLK/ PSTCLK	TMS/ $\overline{BKPT}$	PST1	DDATA1	$\overline{RSTOUT}$	VSS	**P**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 3. MCF5270/71CVMxxx Pinout (196 MAPBGA)

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or OV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and OV_{DD}.

5 Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > OV_{DD}$) is greater than I_{DD}, the injection current may flow out of OV_{DD} and could result in external power supply going out of regulation. Insure external OV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power (ex; no clock).Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions.

7.2   Thermal Characteristics

The below table lists thermal resistance values.

Table 8. Thermal Characteristics

Characteristic		Symbol	196 MAPBGA	160QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	32[1,2]	40[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	29[1,2]	36[1,2]	°C/W
Junction to board		θ_{JB}	20[3]	25[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	104	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Motorola recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A= Ambient Temperature, °C

Θ_{JMA}= Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D= P_{INT} + $P_{I/O}$

P_{INT}= $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273 °C) + \Theta_{JMA} \times P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.3   DC Electrical Specifications

Table 9. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Typical	Max	Unit
Core Supply Voltage	V_{DD}	1.4	—	1.6	V
Pad Supply Voltage	OV_{DD}	3.0	—	3.6	V
PLL Supply Voltage	V_{DDPLL}	3.0	—	3.6	V
Input High Voltage	V_{IH}	$0.7 \times OV_{DD}$	—	3.65	V
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$0.35 \times OV_{DD}$	V
Input Hysteresis	V_{HYS}	$0.06 \times OV_{DD}$	—	—	mV
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	−1.0	—	1.0	µA
High Impedance (Off-State) Leakage Current V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	−1.0	—	1.0	µA
Output High Voltage (All input/output and all output pins) I_{OH} = −5.0 mA	V_{OH}	OV_{DD} - 0.5	—	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	—	0.5	V
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[2]	I_{APU}	−10	—	− 130	µA

Input Capacitance [3]
   All input-only pins
   All input/output (three-state) pins
	C_{in}	
		—
		—
			—	
				7
				7
					pF

Table 10. HiP7 PLLMRFM Electrical Specifications[1] (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
6	XTAL Load Capacitance[5]		5	30	pF
7	PLL Lock Time [5, 7, 13]	t_{lpll}	—	750	μs
8	Power-up To Lock Time [5, 6, 8] With Crystal Reference (includes 5 time) Without Crystal Reference[9]	t_{lplk}	— —	11 750	ms μs
9	1:1 Mode Clock Skew (between CLKOUT and EXTAL) [10]	t_{skew}	−1	1	ns
10	Duty Cycle of reference [5]	t_{dc}	40	60	%
11	Frequency un-LOCK Range	f_{UL}	−3.8	4.1	% $f_{sys/2}$
12	Frequency LOCK Range	f_{LCK}	−1.7	2.0	% $f_{sys/2}$

13	CLKOUT Period Jitter, [5, 6, 8, 11, 12]
	Measured at $f_{sys/2}$ Max
	   Peak-to-peak Jitter (Clock edge to clock edge)
	   Long Term Jitter (Averaged over 2 ms interval)
		C_{jitter}	—
			—
				5.0
				.01
					% $f_{sys/2}$

14	Frequency Modulation Range Limit[13,14] ($f_{sys/2}$ Max must not be exceeded)	C_{mod}	0.8	2.2	% $f_{sys/2}$
15	ICO Frequency. $f_{ico} = f_{ref} \times 2 \times$ (MFD+2) [15]	f_{ico}	48	150	MHz

1. All values given are initial design targets and subject to change.
2. All internal registers retain data at 0 Hz.
3. "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.
4. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.
5. This parameter is guaranteed by characterization before qualification rather than 100% tested.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
8. Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{RSTOUT}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
9. $t_{lpll} = (64 * 4 * 5 + 5 \ \tau) \ T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57 \times 10^{-6} \ 2(\text{MFD} + 2)$.
10. PLL is operating in 1:1 PLL mode.
11. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.
12. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.
13. Modulation percentage applies over an interval of 10μs, or equivalently the modulation rate is 100KHz.
14. Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.
15. $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

7.5 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 11. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
freq	System bus frequency	$f_{sys/2}$	50	75	MHz
B0	CLKOUT period	t_{cyc}	—	1/75	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	9	—	ns
B1b	$\overline{BKPT}$ valid to CLKOUT high[3]	t_{BKVCH}	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{BKPT}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:0]) valid to CLKOUT high	t_{DIVCH}	4	—	ns
B5	CLKOUT high to data input (D[31:0]) invalid	t_{CHDII}	0	—	ns

[1] Timing specifications are tested using full drive strength pad configurations in a 50ohm transmission line environment..

[2] $\overline{TEA}$ and $\overline{TA}$ pins are being referred to as control inputs.

[3] Refer to figure A-19.

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Table 12. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{\text{TS}}$, $\overline{\text{TSIZ}}$[1:0], $\overline{\text{TIP}}$, R/$\overline{\text{W}}$) valid	t_{CHAV}	—	9	ns
B9	CLKOUT high to address (A[23:0]) and control ($\overline{\text{TS}}$, $\overline{\text{TSIZ}}$[1:0], $\overline{\text{TIP}}$, R/$\overline{\text{W}}$) invalid	t_{CHAI}	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:0]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:0]) invalid	t_{CHDOI}	1.5	—	ns
B13	CLKOUT high to data output (D[31:0]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{\text{CS}}$ transitions after the falling edge of CLKOUT.
2 $\overline{\text{BS}}$ transitions after the falling edge of CLKOUT.
3 $\overline{\text{OE}}$ transitions after the falling edge of CLKOUT.

Figure 9 shows a bus cycle terminated by $\overline{\text{TA}}$ showing timings listed in Table 12.
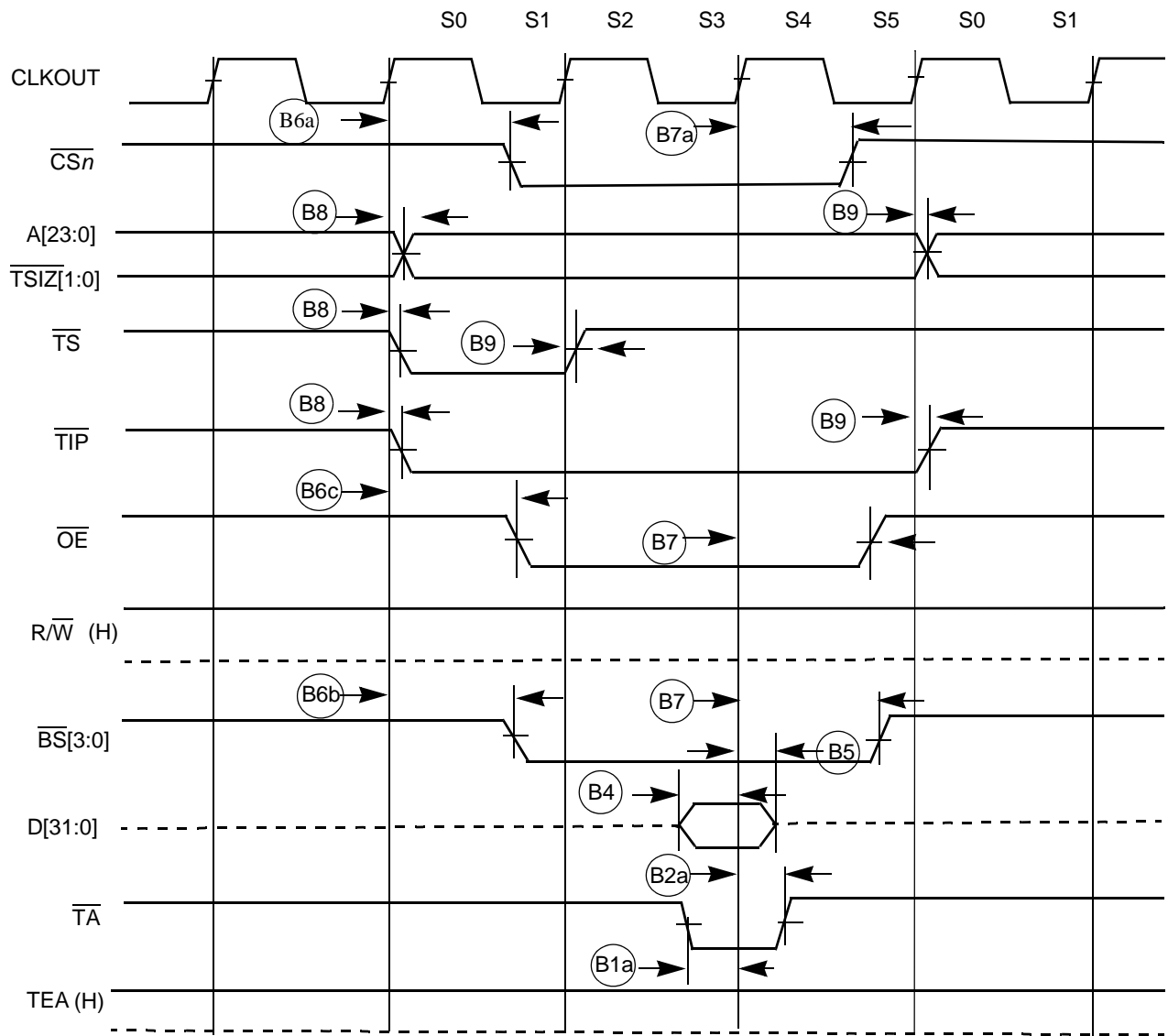

Figure 9. SRAM Read Bus Cycle Terminated by $\overline{\text{TA}}$

Figure 10 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 12.
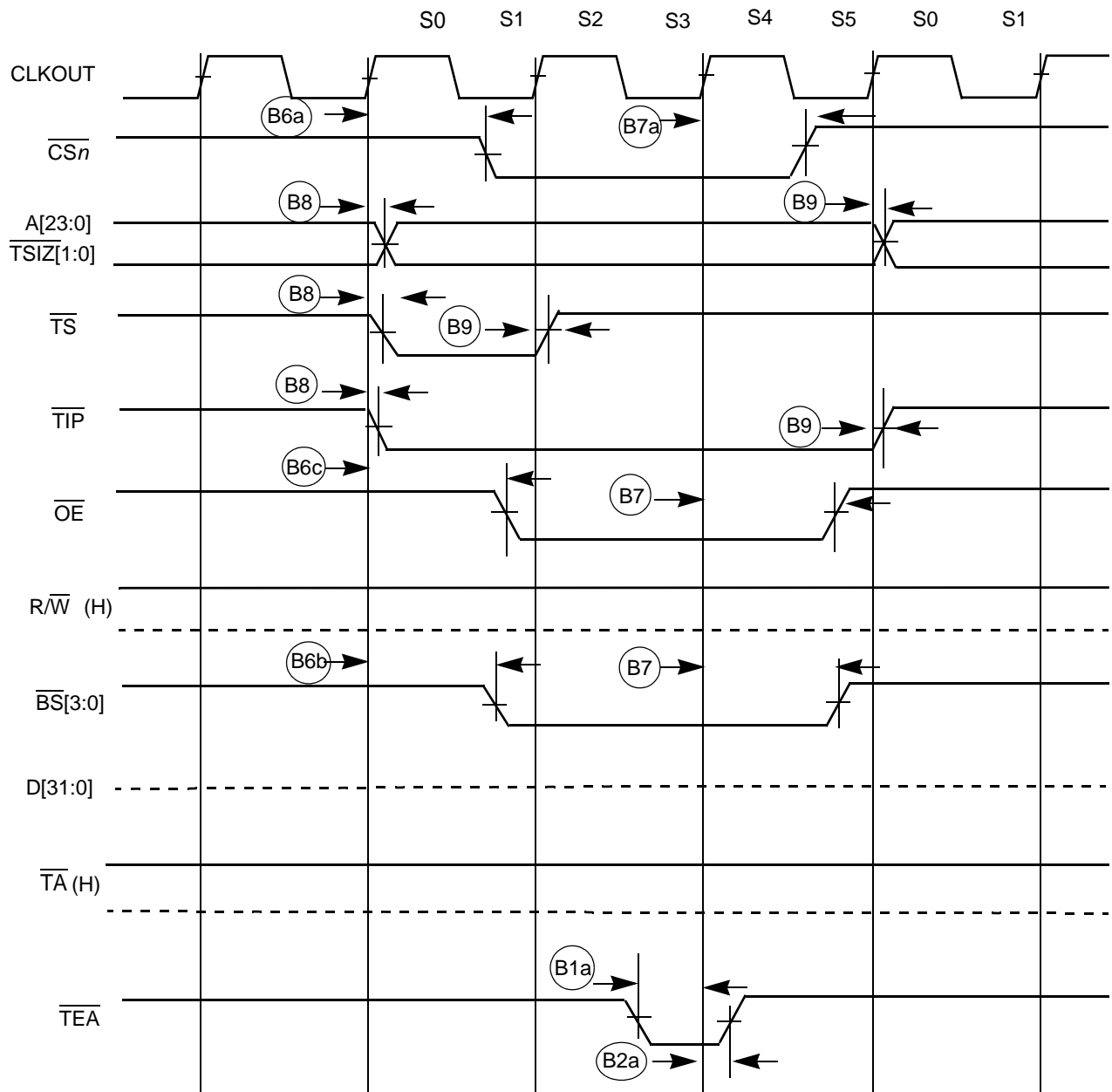

Figure 10. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$
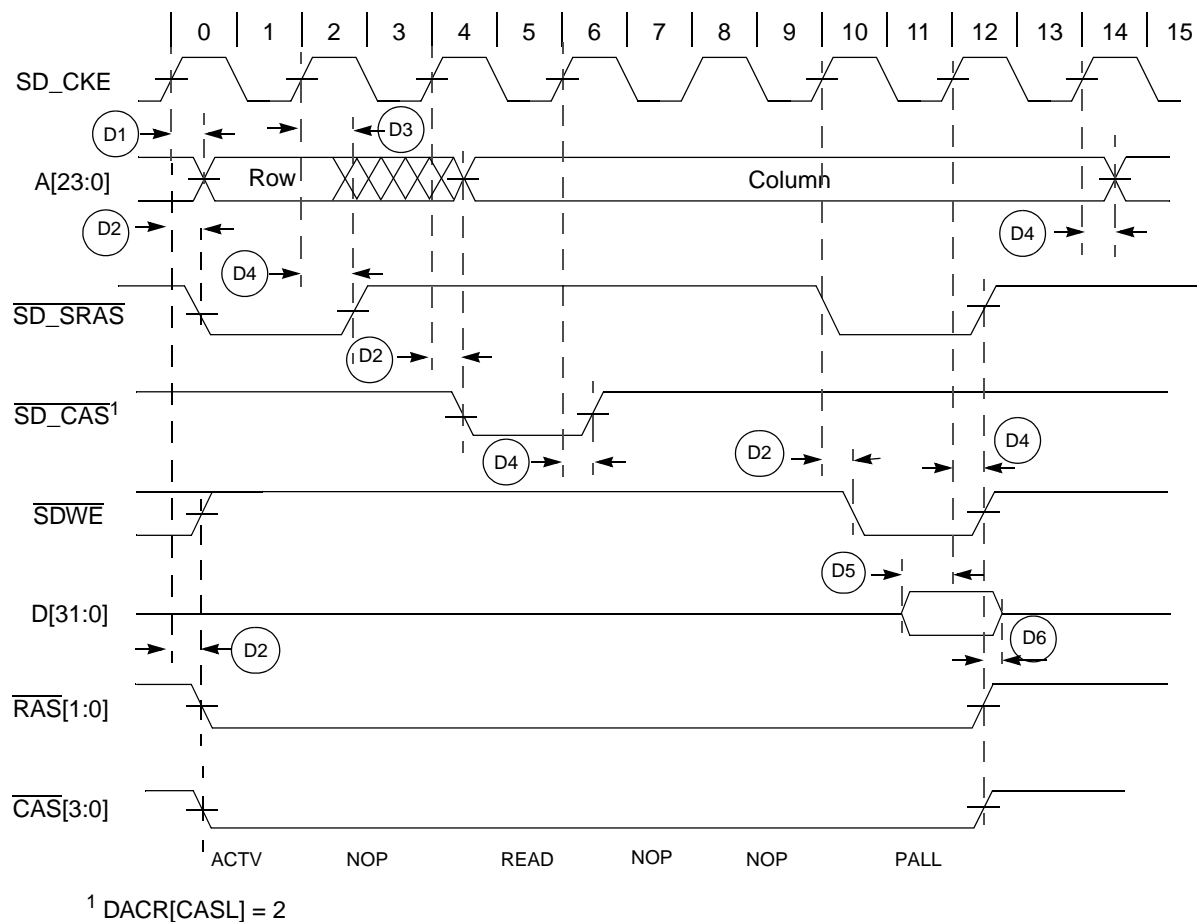
Figure 11 shows an SDRAM read cycle.

Figure 11. SDRAM Read Cycle

Table 13. SDRAM Timing

NUM	Characteristic	Symbol	Min	Max	Unit
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	—	9	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}	—	9	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.5	—	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.5	—	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	4	—	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.5	—	ns
D7[1]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	—	9	ns
D8[1]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.5	—	ns

[1] D7 and D8 are for write cycles only.

7.10.4 MII Serial Management Channel Timing (EMDIO and EMDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	EMDC falling edge to EMDIO output invalid (minimum propagation delay)	0	—	ns
M11	EMDC falling edge to EMDIO output valid (max prop delay)	—	25	ns
M12	EMDIO (input) to EMDC rising edge setup	10	—	ns
M13	EMDIO (input) to EMDC rising edge hold	0	—	ns
M14	EMDC pulse width high	40%	60%	MDC period
M15	EMDC pulse width low	40%	60%	MDC period

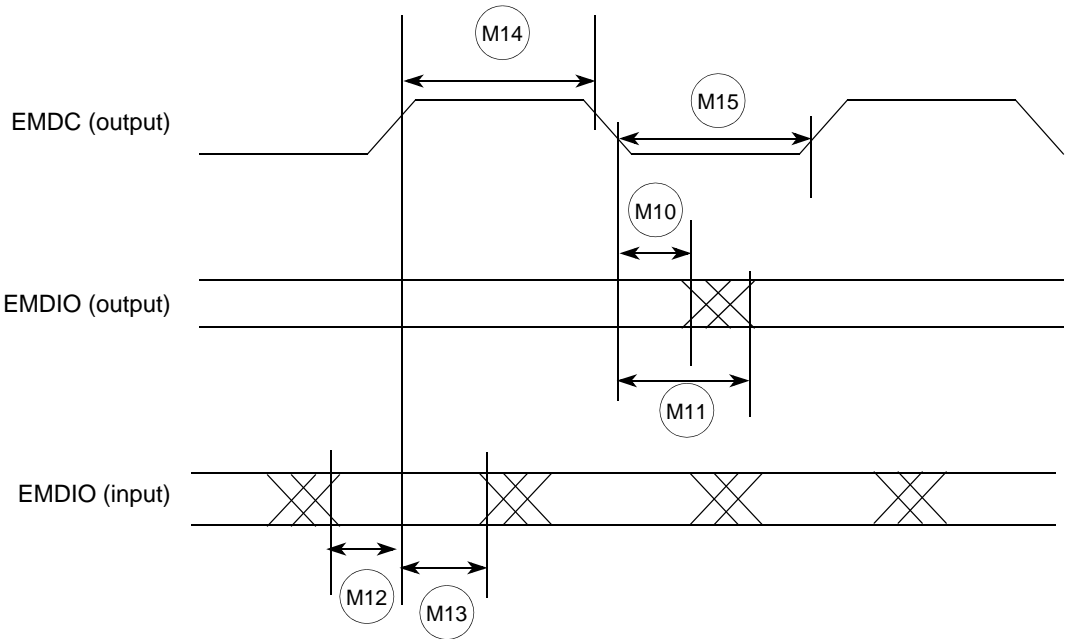Figure 19 shows MII serial management channel timings listed in Table 21.

Figure 19. MII Serial Management Channel Timing Diagram

7.13 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

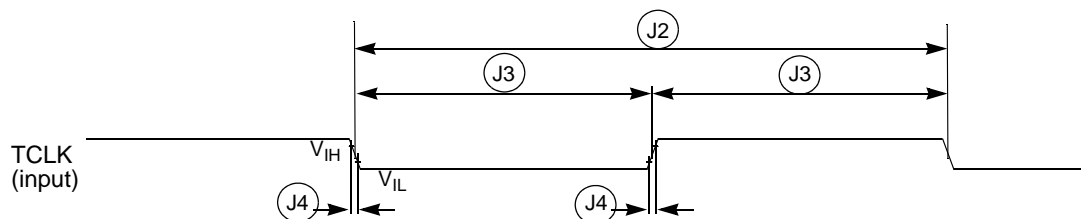[1] JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.
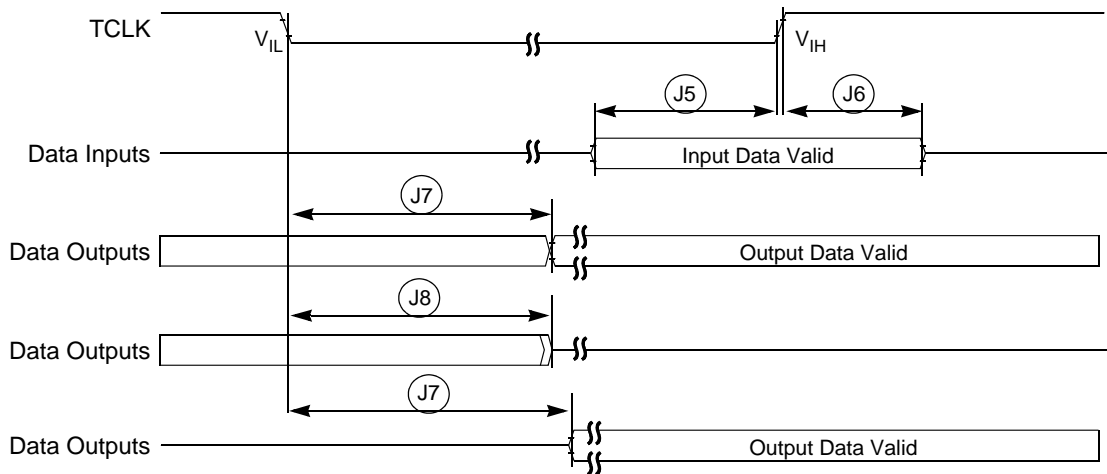

Figure 21. Test Clock Input Timing
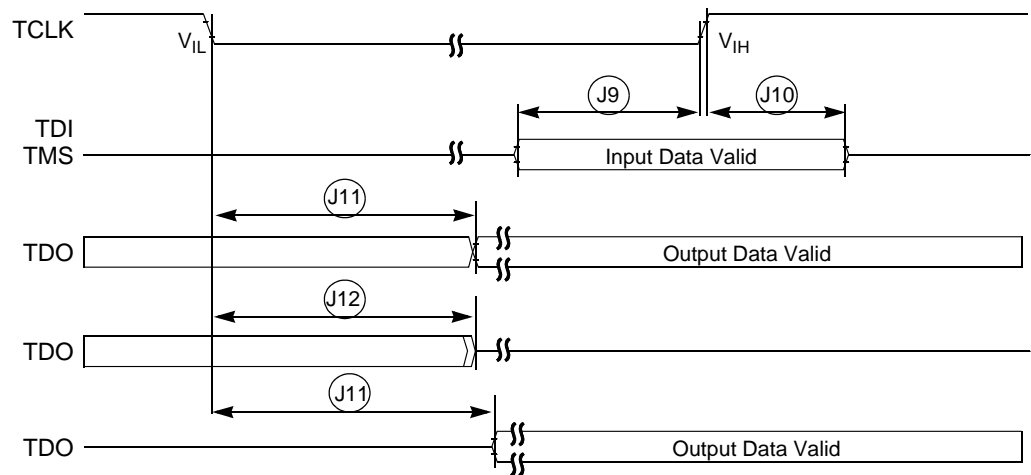
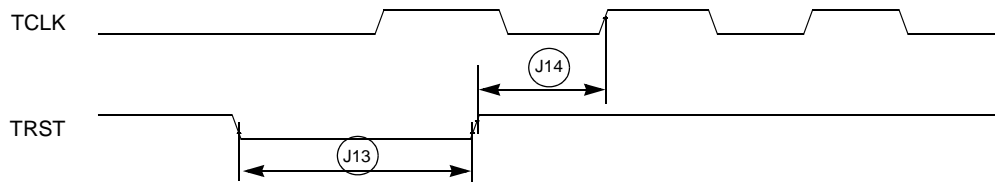**Figure 22. Boundary Scan (JTAG) Timing**

Figure 23. Test Access Port Timing

Figure 24. TRST Timing