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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM7® |
| Core Size | 16/32-Bit |
| Speed | 72MHz |
| Connectivity | CANbus, Ethernet, I²C, Microwire, SPI, SSI, SSP, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 70 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 34K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x10b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2364fbd100-551 |

- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Boundary scan for simplified board testing is available in LPC2364FET100 and LPC2368FET100 (TFBGA package).
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.

## 3. Applications

- Industrial control
- Medical systems
- Protocol converter
- Communications

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC2364FBD100 | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |
| LPC2364HBD100 | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |
| LPC2364FET100 | TFBGA100 | plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm | SOT926-1 |
| LPC2365FBD100 | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |
| LPC2366FBD100 | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |
| LPC2367FBD100 | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |
| LPC2368FBD100 | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |
| LPC2368FET100 | TFBGA100 | plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm | SOT926-1 |

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Flash (kB) | SRAM (kB) | | | | | Ethernet | USB device + 4 kB FIFO | SD/MMC | GP DMA | Channels | | | Temp range |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Local bus | Ethernet buffers | GP/USB | RTC | Total | | | | | CAN | ADC | DAC | |
| LPC2364FBD100 | 128 | 8 | 16 | 8 | 2 | 34 | RMII | yes | no | yes | 2 | 6 | 1 | –40 °C to +85 °C |
| LPC2364HBD100 | 128 | 8 | 16 | 8 | 2 | 34 | RMII | yes | no | yes | 2 | 6 | 1 | –40 °C to +125 °C |
| LPC2364FET100 | 128 | 8 | 16 | 8 | 2 | 34 | RMII | yes | no | yes | 2 | 6 | 1 | –40 °C to +85 °C |
| LPC2365FBD100 | 256 | 32 | 16 | 8 | 2 | 58 | RMII | no | no | yes | - | 6 | 1 | –40 °C to +85 °C |
| LPC2366FBD100 | 256 | 32 | 16 | 8 | 2 | 58 | RMII | yes | no | yes | 2 | 6 | 1 | –40 °C to +85 °C |
| LPC2367FBD100 | 512 | 32 | 16 | 8 | 2 | 58 | RMII | no | yes | yes | - | 6 | 1 | –40 °C to +85 °C |
| LPC2368FBD100 | 512 | 32 | 16 | 8 | 2 | 58 | RMII | yes | yes | yes | 2 | 6 | 1 | –40 °C to +85 °C |
| LPC2368FET100 | 512 | 32 | 16 | 8 | 2 | 58 | RMII | yes | yes | yes | 2 | 6 | 1 | –40 °C to +85 °C |

**Table 3. Pin allocation table**

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|
| **Row A** | | | | | | | |
| 1 | TDO | 2 | P0[3]/RXD0 | 3 | $V_{DD(3V3)}$ | 4 | P1[4]/ENET_TX_EN |
| 5 | P1[10]/ENET_RXD1 | 6 | P1[16]/ENET_MDC | 7 | $V_{DD(DCDC)(3V3)}$ | 8 | P0[4]/I2SRX_CLK/ RD2/CAP2[0] |
| 9 | P0[7]/I2STX_CLK/ SCK1/MAT2[1] | 10 | P0[9]/I2STX_SDA/ MOSI1/MAT2[3] | 11 | - | 12 | - |
| **Row B** | | | | | | | |
| 1 | TMS | 2 | RTCK | 3 | $V_{SS}$ | 4 | P1[1]/ENET_TXD1 |
| 5 | P1[9]/ENET_RXD0 | 6 | P1[17]/ ENET_MDIO | 7 | $V_{SS}$ | 8 | P0[6]/I2SRX_SDA/ SSEL1/MAT2[0] |
| 9 | P2[0]/PWM1[1]/ TXD1/TRACECLK | 10 | P2[1]/PWM1[2]/ RXD1/PIPESTAT0 | 11 | - | 12 | - |
| **Row C** | | | | | | | |
| 1 | TCK | 2 | $\overline{\text{TRST}}$ | 3 | TDI | 4 | P0[2]/TXD0 |
| 5 | P1[8]/ENET_CRS | 6 | P1[15]/ ENET_REF_CLK | 7 | P4[28]/MAT2[0]/ TXD3 | 8 | P0[8]/I2STX_WS/ MISO1/MAT2[2] |
| 9 | $V_{SS}$ | 10 | $V_{DD(3V3)}$ | 11 | - | 12 | - |
| **Row D** | | | | | | | |
| 1 | P0[24]/AD0[1]/ I2SRX_WS/CAP3[1] | 2 | P0[25]/AD0[2]/ I2SRX_SDA/TXD3 | 3 | P0[26]/AD0[3]/ AOUT/RXD3 | 4 | DBGEN |
| 5 | P1[0]/ENET_TXD0 | 6 | P1[14]/ENET_RX_ER | 7 | P0[5]/I2SRX_WS/ TD2/CAP2[1] | 8 | P2[2]/PWM1[3]/ CTS1/PIPESTAT1 |
| 9 | P2[4]/PWM1[5]/ DSR1/TRACESYNC | 10 | P2[5]/PWM1[6]/ DTR1/TRACEPKT0 | 11 | - | 12 | - |
| **Row E** | | | | | | | |
| 1 | $V_{SSA}$ | 2 | $V_{DDA}$ | 3 | VREF | 4 | $V_{DD(DCDC)(3V3)}$ |
| 5 | P0[23]/AD0[0]/ I2SRX_CLK/CAP3[0] | 6 | P4[29]/MAT2[1]/ RXD3 | 7 | P2[3]/PWM1[4]/ DCD1/PIPESTAT2 | 8 | P2[6]/PCAP1[0]/RI1/ TRACEPKT1 |
| 9 | P2[7]/RD2/ RTS1/TRACEPKT2 | 10 | P2[8]/TD2/ TXD2/TRACEPKT3 | 11 | - | 12 | - |
| **Row F** | | | | | | | |
| 1 | $V_{SS}$ | 2 | RTCX1 | 3 | $\overline{\text{RESET}}$ | 4 | P1[31]/SCK1/ AD0[5] |
| 5 | P1[21]/PWM1[3]/ SSEL0 | 6 | P0[18]/DCD1/ MOSI0/MOSI | 7 | P2[9]/USB_CONNECT/ RXD2/EXTIN0 | 8 | P0[16]/RXD1/ SSEL0/SSEL |
| 9 | P0[17]/CTS1/ MISO0/MISO | 10 | P0[15]/TXD1/ SCK0/SCK | 11 | - | 12 | - |
| **Row G** | | | | | | | |
| 1 | RTCX2 | 2 | VBAT | 3 | XTAL2 | 4 | P0[30]/USB_D− |
| 5 | P1[25]/MAT1[1] | 6 | P1[29]/PCAP1[1]/ MAT0[1] | 7 | $V_{SS}$ | 8 | P0[21]/RI1/ MCIPWR/RD1 |
| 9 | P0[20]/DTR1/ MCICMD/SCL1 | 10 | P0[19]/DSR1/ MCICLK/SDA1 | 11 | - | 12 | - |
| **Row H** | | | | | | | |

**Table 3. Pin allocation table** *…continued*

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|
| 1 | P1[30]/$V_{BUS}$/ AD0[4] | 2 | XTAL1 | 3 | P3[25]/MAT0[0]/ PWM1[2] | 4 | P1[18]/USB_UP_LED/ PWM1[1]/CAP1[0] |
| 5 | P1[24]/PWM1[5]/ MOSI0 | 6 | $V_{DD(DCDC)(3V3)}$ | 7 | P0[10]/TXD2/ SDA2/MAT3[0] | 8 | P2[11]/$\overline{\text{EINT1}}$/ MCIDAT1/I2STX_CLK |
| 9 | $V_{DD(3V3)}$ | 10 | P0[22]/RTS1/ MCIDAT0/TD1 | 11 | - | 12 | - |

## 6.2 Pin description

**Table 4. Pin description**

| Symbol | Pin | Ball | Type | Description |
|---|---|---|---|---|
| P0[0] to P0[31] | | | I/O | **Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 0 pins depends upon the pin function selected via the pin connect block. Pins 12, 13, 14, and 31 of this port are not available. |
| P0[0]/RD1/TXD3/ SDA1 | 46[1] | K8[1] | I/O | **P0[0] —** General purpose digital input/output pin. |
| | | | I | **RD1 —** CAN1 receiver input. (LPC2364/66/68 only) |
| | | | O | **TXD3 —** Transmitter output for UART3. |
| | | | I/O | **SDA1 —** $I^2C1$ data input/output (this is not an open-drain pin). |
| P0[1]/TD1/RXD3/ SCL1 | 47[1] | J8[1] | I/O | **P0[1] —** General purpose digital input/output pin. |
| | | | O | **TD1 —** CAN1 transmitter output. (LPC2364/66/68 only) |
| | | | I | **RXD3 —** Receiver input for UART3. |
| | | | I/O | **SCL1 —** $I^2C1$ clock input/output (this is not an open-drain pin). |
| P0[2]/TXD0 | 98[1] | C4[1] | I/O | **P0[2] —** General purpose digital input/output pin. |
| | | | O | **TXD0 —** Transmitter output for UART0. |
| P0[3]/RXD0 | 99[1] | A2[1] | I/O | **P0[3] —** General purpose digital input/output pin. |
| | | | I | **RXD0 —** Receiver input for UART0. |
| P0[4]/ I2SRX_CLK/ RD2/CAP2[0] | 81[1] | A8[1] | I/O | **P0[4] —** General purpose digital input/output pin. |
| | | | I/O | **I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| | | | I | **RD2 —** CAN2 receiver input. (LPC2364/66/68 only) |
| | | | I | **CAP2[0] —** Capture input for Timer 2, channel 0. |
| P0[5]/ I2SRX_WS/ TD2/CAP2[1] | 80[1] | D7[1] | I/O | **P0[5] —** General purpose digital input/output pin. |
| | | | I/O | **I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | O | **TD2 —** CAN2 transmitter output. (LPC2364/66/68 only) |
| | | | I | **CAP2[1] —** Capture input for Timer 2, channel 1. |
| P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0] | 79[1] | B8[1] | I/O | **P0[6] —** General purpose digital input/output pin. |
| | | | I/O | **I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *$I^2S$-bus specification*. |
| | | | I/O | **SSEL1 —** Slave Select for SSP1. |
| | | | O | **MAT2[0] —** Match output for Timer 2, channel 0. |
| P0[7]/ I2STX_CLK/ SCK1/MAT2[1] | 78[1] | A9[1] | I/O | **P0[7] —** General purpose digital input/output pin. |
| | | | I/O | **I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| | | | I/O | **SCK1 —** Serial Clock for SSP1. |
| | | | O | **MAT2[1] —** Match output for Timer 2, channel 1. |
| P0[8]/ I2STX_WS/ MISO1/MAT2[2] | 77[1] | C8[1] | I/O | **P0[8] —** General purpose digital input/output pin. |
| | | | I/O | **I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | I/O | **MISO1 —** Master In Slave Out for SSP1. |
| | | | O | **MAT2[2] —** Match output for Timer 2, channel 2. |

**Table 4. Pin description** *…continued*

| Symbol | Pin | Ball | Type | Description |
|---|---|---|---|---|
| P2[12]/EINT2/ MCIDAT2/ I2STX_WS | 51[6] | K10[6] | I/O | **P2[12] —** General purpose digital input/output pin. |
| | | | I | **EINT2 —** External interrupt 2 input. |
| | | | O | **MCIDAT2 —** Data line for SD/MMC interface. (LPC2367/68 only) |
| | | | I/O | **I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. |
| P2[13]/EINT3/ MCIDAT3/ I2STX_SDA | 50[6] | J9[6] | I/O | **P2[13] —** General purpose digital input/output pin. |
| | | | I | **EINT3 —** External interrupt 3 input. |
| | | | O | **MCIDAT3 —** Data line for SD/MMC interface. (LPC2367/68 only) |
| | | | I/O | **I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. |
| P3[0] to P3[31] | | | I/O | **Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 3 pins depends upon the pin function selected via the pin connect block. Pins 0 through 24, and 27 through 31 of this port are not available. |
| P3[25]/MAT0[0]/ PWM1[2] | 27[1] | H3[1] | I/O | **P3[25] —** General purpose digital input/output pin. |
| | | | O | **MAT0[0] —** Match output for Timer 0, channel 0. |
| | | | O | **PWM1[2] —** Pulse Width Modulator 1, output 2. |
| P3[26]/MAT0[1]/ PWM1[3] | 26[1] | K1[1] | I/O | **P3[26] —** General purpose digital input/output pin. |
| | | | O | **MAT0[1] —** Match output for Timer 0, channel 1. |
| | | | O | **PWM1[3] —** Pulse Width Modulator 1, output 3. |
| P4[0] to P4[31] | | | I/O | **Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 4 pins depends upon the pin function selected via the pin connect block. Pins 0 through 27, 30, and 31 of this port are not available. |
| P4[28]/MAT2[0]/ TXD3 | 82[1] | C7[1] | I/O | **P4[28] —** General purpose digital input/output pin. |
| | | | O | **MAT2[0] —** Match output for Timer 2, channel 0. |
| | | | O | **TXD3 —** Transmitter output for UART3. |
| P4[29]/MAT2[1]/ RXD3 | 85[1] | E6[1] | I/O | **P4[29] —** General purpose digital input/output pin. |
| | | | O | **MAT2[1] —** Match output for Timer 2, channel 1. |
| | | | I | **RXD3 —** Receiver input for UART3. |
| DBGEN | - | D4[1][8] | I | **DBGEN —** JTAG interface control signal. Also used for boundary scanning.<br>**Note:** This pin is available in LPC2364FET100 and LPC2368FET100 devices only (TFBGA package). |
| TDO | 1[1][7] | A1[1][7] | O | **TDO —** Test Data out for JTAG interface. |
| TDI | 2[1][8] | C3[1][8] | I | **TDI —** Test Data in for JTAG interface. |
| TMS | 3[1][8] | B1[1][8] | I | **TMS —** Test Mode Select for JTAG interface. |
| TRST | 4[1][8] | C2[1][8] | I | **TRST —** Test Reset for JTAG interface. |
| TCK | 5[1][7] | C1[1][7] | I | **TCK —** Test Clock for JTAG interface. This clock must be slower than 1/6 of the CPU clock (CCLK) for the JTAG interface to operate |
| RTCK | 100[1][8] | B2[1][8] | I/O | **RTCK —** JTAG interface control signal.<br>**Note:** LOW on this pin while RESET is LOW enables ETM pins (P2[9:0]) to operate as trace port after reset. |

**Table 4. Pin description** *…continued*

| Symbol | Pin | Ball | Type | Description |
|---|---|---|---|---|
| $\overline{\text{RSTOUT}}$ | 14 | - | O | **$\overline{\text{RSTOUT}}$ —** This is a 3.3 V pin. LOW on this pin indicates LPC2364/65/66/67/68 being in Reset state.<br>**Note:** This pin is available in LPC2364FBD100, LPC2365FBD100, LPC2366FBD100, LPC2367FBD100, and LPC2368FBD100 devices only (LQFP100 package). |
| $\overline{\text{RESET}}$ | 17[9] | F3[9] | I | **External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant. |
| XTAL1 | 22[10][11] | H2[10][11] | I | Input to the oscillator circuit and internal clock generator circuits. |
| XTAL2 | 23[10][11] | G3[10][11] | O | Output from the oscillator amplifier. |
| RTCX1 | 16[10][12] | F2[10][12] | I | Input to the RTC oscillator circuit. |
| RTCX2 | 18[10] | G1[10] | O | Output from the RTC oscillator circuit. |
| $V_{SS}$ | 15, 31, 41, 55, 72, 97, 83[13] | B3, B7, C9, F1, G7, J6, K3 [13] | I | **ground:** 0 V reference. |
| $V_{SSA}$ | 11[14] | E1[14] | I | **analog ground:** 0 V reference. This should nominally be the same voltage as $V_{SS}$, but should be isolated to minimize noise and error. |
| $V_{DD(3V3)}$ | 28, 54, 71, 96[15] | A3, C10, H9, K2[15] | I | **3.3 V supply voltage:** This is the power supply voltage for the I/O ports. |
| $V_{DD(DCDC)(3V3)}$ | 13, 42, 84[16] | A7, E4, H6[16] | I | **3.3 V DC-to-DC converter supply voltage:** This is the supply voltage for the on-chip DC-to-DC converter only. |
| $V_{DDA}$ | 10[17] | E2[17] | I | **analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. |
| VREF | 12[17] | E3[17] | I | **ADC reference:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC. |
| VBAT | 19[17] | G2[17] | I | **RTC pin power supply:** 3.3 V on this pin supplies the power to the RTC peripheral. |

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a DAC input, digital section of the pad is disabled.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[4] Open-drain 5 V tolerant digital I/O pad, compatible with $I^2C$-bus 400 kHz specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the $I^2C$-bus is floating and does not disturb the $I^2C$ lines. Open-drain configuration applies to all functions on this pin.

[5] Pad provides digital I/O and USB functions (LPC2364/66/68 only). It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[6] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[7] This pin has no built-in pull-up and no built-in pull-down resistor.

[8] This pin has a built-in pull-up resistor.

[9] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[10] Pad provides special analog functionality.

[11] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

FIQs have the highest priority. If more than one request is assigned to FIQ, the VIC ORs the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs, which include all interrupt requests that are not classified as FIQs, have a programmable interrupt priority. When more than one interrupt is assigned the same priority and occur simultaneously, the one connected to the lowest numbered VIC channel will be serviced first.

The VIC ORs the requests from all of the vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping to the address supplied by that register.

### 7.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the VIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both. Such interrupt request coming from Port 0 and/or Port 2 will be combined with the $\overline{\text{EINT3}}$ interrupt requests.

## 7.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

## 7.7 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected LPC2364/65/66/67/68 peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master.

### 7.7.1 Features

- Two DMA channels. Each channel can support a unidirectional transfer.
- The GPDMA can transfer data between the 8 kB SRAM and peripherals such as the SD/MMC, two SSP, and $I^2S$ interfaces.

## 7.13 10-bit DAC

The DAC allows the LPC2364/65/66/67/68 to generate a variable analog output. The maximum output value of the DAC is $V_{i(VREF)}$.

### 7.13.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive

## 7.14 UARTs

The LPC2364/65/66/67/68 each contain four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

### 7.14.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- UART3 includes an IrDA mode to support infrared communication.

## 7.15 SPI serial I/O controller

The LPC2364/65/66/67/68 each contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

### 7.15.1 Features

- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

## 7.20 General purpose 32-bit timers/external event counters

The LPC2364/65/66/67/68 include four 32-bit Timer/Counters. The Timer/Counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The Timer/Counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

### 7.20.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit prescaler.
- Counter or Timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

## 7.21 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2364/65/66/67/68. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the RTC clock, the Internal RC oscillator (IRC), or the APB peripheral clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring, for increased reliability.

## 7.23 RTC and battery RAM

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power in Power-down and Deep power-down modes. On the LPC2364/65/66/67/68, the RTC can be clocked by a separate 32.768 kHz oscillator, or by a programmable prescale divider based on the APB clock. Also, the RTC is powered by its own power supply pin, VBAT, which can be connected to a battery or to the same 3.3 V supply used by the rest of the device.

The VBAT pin supplies power only to the RTC and the battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery.

### 7.23.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values.
- 2 kB data SRAM powered by VBAT.
- RTC and battery RAM power supply is isolated from the rest of the chip.

## 7.24 Clocking and power control

### 7.24.1 Crystal oscillators

The LPC2364/65/66/67/68 includes three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2364/65/66/67/68 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD(3V3)}$ | supply voltage (3.3 V) | core and external rail | | 3.0 | 3.6 | V |
| $V_{DD(DCDC)(3V3)}$ | DC-to-DC converter supply voltage (3.3 V) | | | 3.0 | 3.6 | V |
| $V_{DDA}$ | analog 3.3 V pad supply voltage | | | −0.5 | +4.6 | V |
| $V_{i(VBAT)}$ | input voltage on pin VBAT | for the RTC | | −0.5 | +4.6 | V |
| $V_{i(VREF)}$ | input voltage on pin VREF | | | −0.5 | +4.6 | V |
| $V_{IA}$ | analog input voltage | on ADC related pins | | −0.5 | +5.1 | V |
| $V_I$ | input voltage | 5 V tolerant I/O pins; only valid when the $V_{DD(3V3)}$ supply voltage is present | [2] | −0.5 | +6.0 | V |
| | | other I/O pins | [2][3] | −0.5 | $V_{DD(3V3)}$ + 0.5 | V |
| $I_{DD}$ | supply current | per supply pin | [4] | - | 100 | mA |
| $I_{SS}$ | ground current | per ground pin | [4] | - | 100 | mA |
| $T_{stg}$ | storage temperature | non-operating | [5] | −65 | +150 | °C |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | | - | 1.5 | W |
| $V_{ESD}$ | electrostatic discharge voltage | human body model; all pins | [6] | −2500 | +2500 | V |

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The peak current is limited to 25 times the corresponding maximum current.

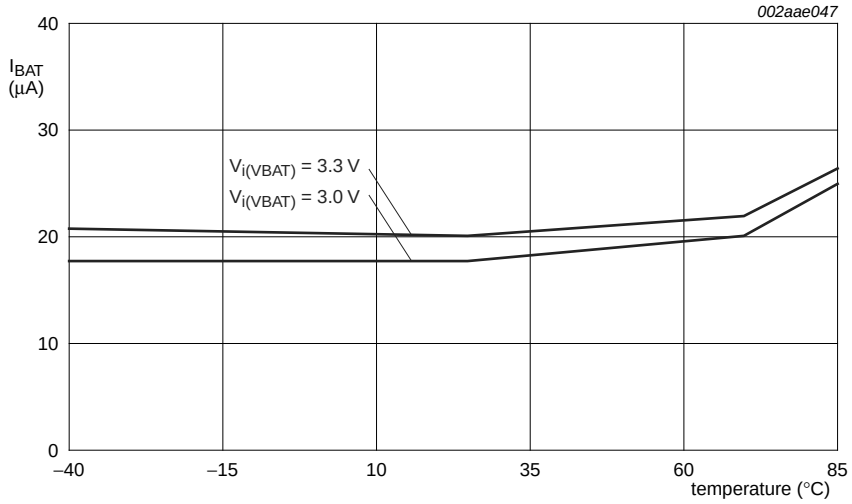
[5] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

**Table 8. Static characteristics** *…continued*

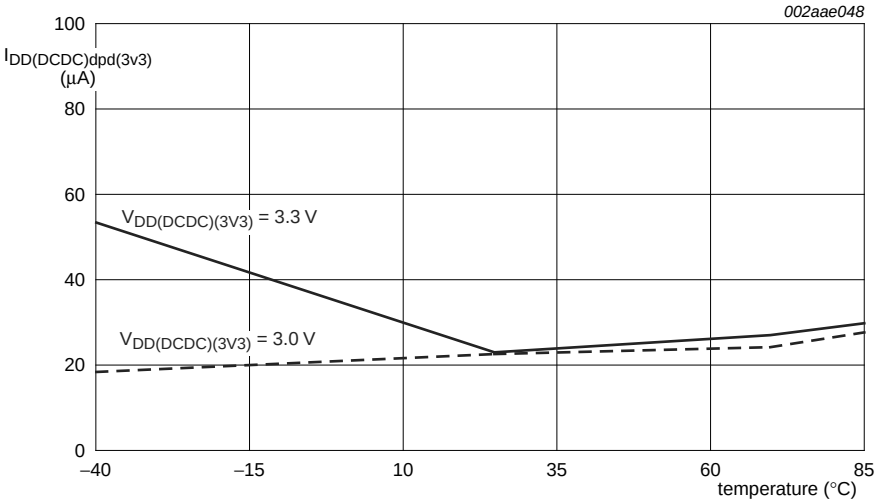
*$T_{amb}$ = −40 °C to +85 °C for standard devices, −40 °C to +125 °C for LPC2364HBD only, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{latch}$ | I/O latch-up current | $-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C | | - | - | 100 | mA |
| $V_I$ | input voltage | pin configured to provide a digital function | [5][6] [7][8] | 0 | - | 5.5 | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD(3V3)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | 0.8 | V |
| $V_{hys}$ | hysteresis voltage | | | 0.4 | - | - | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −4 mA | [9] | $V_{DD(3V3)} - 0.4$ | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = −4 mA | [9] | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{OH} = V_{DD(3V3)} - 0.4$ V | [9] | −4 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | [9] | 4 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | $V_{OH}$ = 0 V | [10] | - | - | −45 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | $V_{OL} = V_{DDA}$ | [10] | - | - | 50 | mA |
| $I_{pd}$ | pull-down current | $V_I$ = 5 V | [11] | 10 | 50 | 150 | μA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V; −40 °C to +85 °C | | −15 | −50 | −85 | μA |
| | | $V_I$ = 0 V; > 85 °C | [12] | −15 | −50 | −100 | μA |
| | | $V_{DD(3V3)} < V_I < 5$ V | [11] | 0 | 0 | 0 | μA |
| **$I^2C$-bus pins (P0[27] and P0[28])** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD(3V3)}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD(3V3)}$ | V |
| $V_{hys}$ | hysteresis voltage | | | - | $0.05V_{DD(3V3)}$ | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OLS}$ = 3 mA | [9] | - | - | 0.4 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{DD(3V3)}$ | [13] | - | 2 | 4 | μA |
| | | $V_I$ = 5 V | | - | 10 | 22 | μA |
| **Oscillator pins** | | | | | | | |
| $V_{i(XTAL1)}$ | input voltage on pin XTAL1 | | | −0.5 | 1.8 | 1.95 | V |
| $V_{o(XTAL2)}$ | output voltage on pin XTAL2 | | | −0.5 | 1.8 | 1.95 | V |
| $V_{i(RTCX1)}$ | input voltage on pin RTCX1 | | | −0.5 | 1.8 | 1.95 | V |
| $V_{o(RTCX2)}$ | output voltage on pin RTCX2 | | | −0.5 | 1.8 | 1.95 | V |




$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C

**Fig 9. RTC battery maximum supply current $I_{BAT}$ versus temperature in Deep power-down mode**




$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

**Fig 10. Total DC-to-DC converter maximum supply current $I_{DD(DCDC)dpd(3V3)}$ versus temperature in Deep power-down mode**

## 11.4 Flash memory

**Table 13. Dynamic characteristics of flash**

*$T_{amb}$ = −40 °C to +85 °C for standard devices, −40 °C to +125 °C for LPC2364HBD only, unless otherwise specified; $V_{DD(3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $N_{endu}$ | endurance | | [1] | 10000 | 100000 | - | cycles |
| $t_{ret}$ | retention time | powered; < 100 cycles | | 10 | - | - | years |
| | | unpowered; < 100 cycles | | 20 | - | - | years |
| $t_{er}$ | erase time | sector or multiple consecutive sectors | | 95 | 100 | 105 | ms |
| $t_{prog}$ | programming time | | [2] | 0.95 | 1 | 1.05 | ms |

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

## 14.5 Standard I/O pin configuration

Figure 23 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Analog input (for ADC input channels)

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

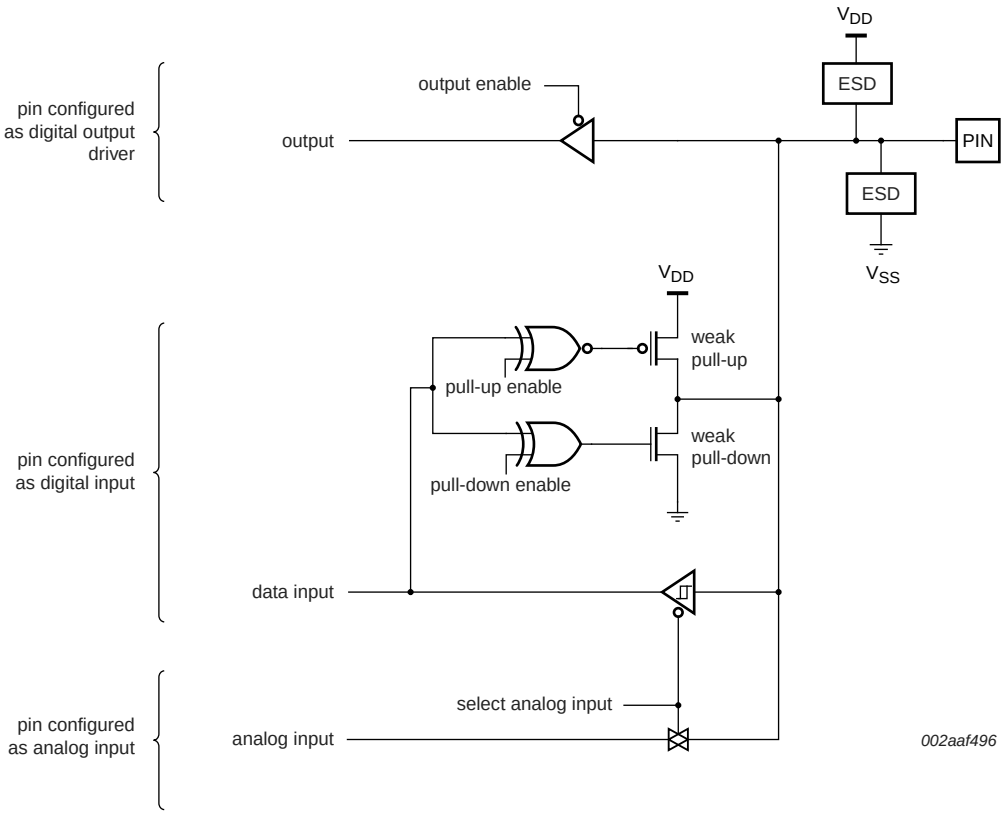



**Fig 23. Standard I/O pin configuration with analog input**

# 16. Abbreviations

**Table 19. Abbreviations**

| Acronym | Description |
|---|---|
| ADC | Analog-to-Digital Converter |
| AHB | Advanced High-performance Bus |
| AMBA | Advanced Microcontroller Bus Architecture |
| APB | Advanced Peripheral Bus |
| BOD | BrownOut Detection |
| CAN | Controller Area Network |
| DAC | Digital-to-Analog Converter |
| DCC | Debug Communication Channel |
| DMA | Direct Memory Access |
| DSP | Digital Signal Processing |
| EOP | End Of Packet |
| ETM | Embedded Trace Macrocell |
| GPIO | General Purpose Input/Output |
| IrDA | Infrared Data Association |
| JTAG | Joint Test Action Group |
| MII | Media Independent Interface |
| MIIM | Media Independent Interface Management |
| PHY | Physical Layer |
| PLL | Phase-Locked Loop |
| PWM | Pulse Width Modulator |
| RMII | Reduced Media Independent Interface |
| SE0 | Single Ended Zero |
| SPI | Serial Peripheral Interface |
| SSI | Serial Synchronous Interface |
| SSP | Synchronous Serial Port |
| TTL | Transistor-Transistor Logic |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |

**Table 20. Revision history** *…continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC2364_65_66_67_68 v.6 | 20100201 | Product data sheet | - | LPC2364_65_66_67_68 v.5 |
| Modifications: | • Table 5 “Limiting values”: Changed $V_{ESD}$ min/max to −2500/+2500.<br>• Table 6: Updated min, typical and max values for oscillator pins.<br>• Table 6: Updated conditions and typical values for $I_{DD(DCDC)pd(3V3)}$, $I_{BATact}$; $I_{DD(DCDC)dpd(3V3)}$ and $I_{BAT}$ added.<br>• Table 9 “Dynamic characteristics of flash”: Changed flash endurance spec from 100000 to 10000 minimum cycles.<br>• Added Table 11 “DAC electrical characteristics”.<br>• Section 7.2 “On-chip flash programming memory”: Removed text regarding flash endurance minimum specs.<br>• Added Section 7.24.4.4 “Deep power-down mode”.<br>• Section 7.25.2 “Brownout detection”: Changed $V_{DD(3V3)}$ to $V_{DD(DCDC)(3V3)}$.<br>• Added Section 9.2 “Deep power-down mode”.<br>• Added Section 13.2 “XTAL1 input”.<br>• Added Section 13.3 “XTAL and RTC Printed-Circuit Board (PCB) layout guidelines”.<br>• Added table note for XTAL1 and XTAL2 pins in Table 3. | | | |
| LPC2364_65_66_67_68 v.5 | 20090409 | Product data sheet | - | LPC2364_65_66_67_68 v.4 |
| Modifications: | • Added part LPC2364HBD100.<br>• Section 7.2: Added sentence clarifying SRAM speeds for LPC2364HBD.<br>• Table 5: Updated $V_{esd}$ min/max.<br>• Table 6: Updated $Z_{DRV}$ Table note [14].<br>• Table 6: $V_{hys}$, moved 0.4 from typ to min column.<br>• Table 6: $I_{pu}$, added specs for >85 °C.<br>• Table 6: Removed $R_{pu}$.<br>• Table 7: CCLK and IRC, added specs for >85 °C.<br>• Added Table 9.<br>• Updated Figure 14.<br>• Updated Figure 11. | | | |
| LPC2364_65_66_67_68 v.4 | 20080417 | Product data sheet | - | LPC2364_66_68 v.3 |
| LPC2364_66_68 v.3 | 20071220 | Product data sheet | - | LPC2364_66_68 v.2 |
| LPC2364_66_68 v.2 | 20071001 | Preliminary data sheet | - | LPC2364_66_68 v.1 |
| LPC2364_66_68 v.1 | 20070103 | Preliminary data sheet | - | - |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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