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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

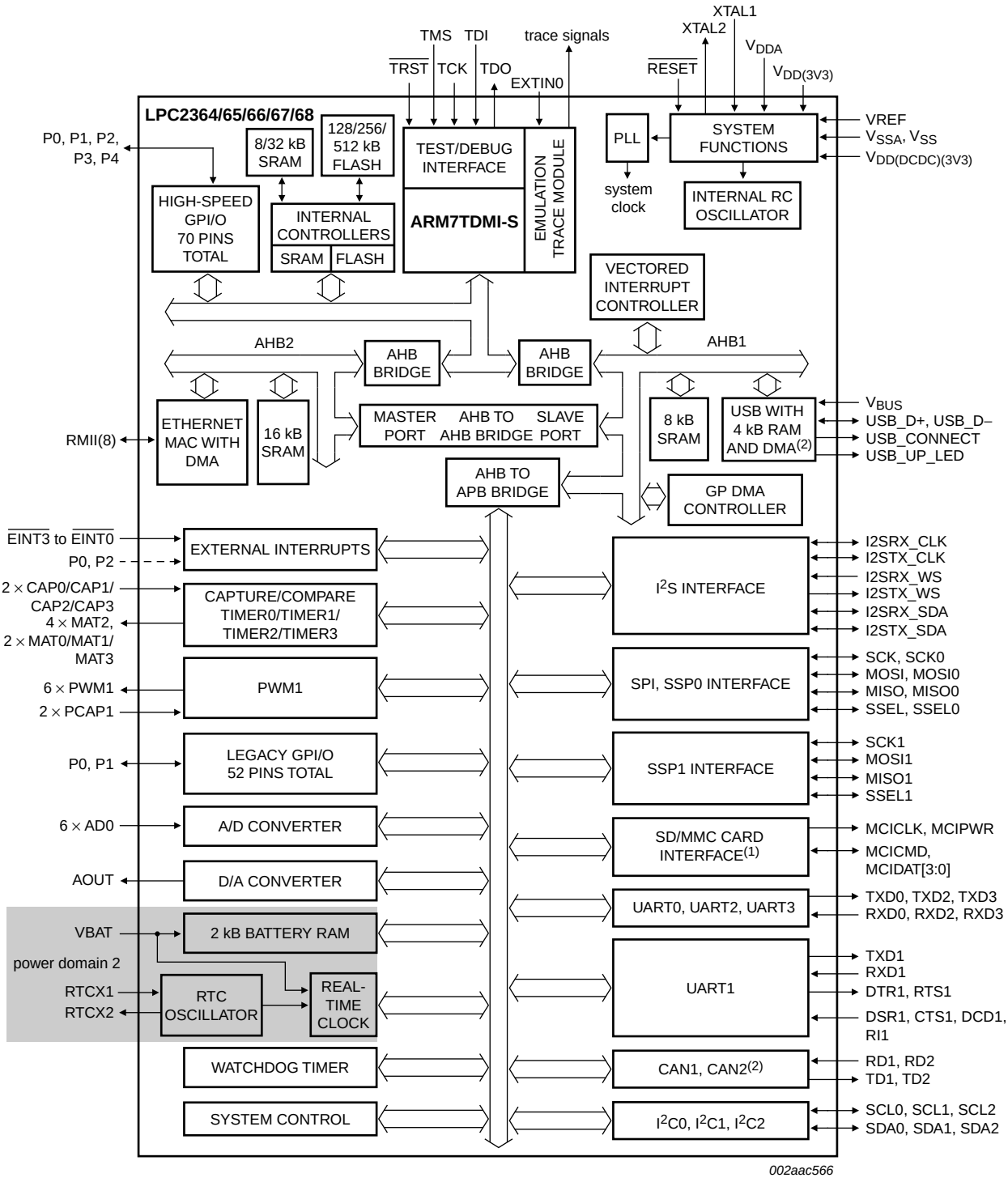
Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, Ethernet, I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	70
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2364fet100-518

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					Ethernet	USB device + 4 kB FIFO	SD/MMC	GP DMA	Channels			Temp range
		Local bus	Ethernet buffers	GP/USB	RTC	Total					CAN	ADC	DAC	
LPC2364FBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2364HBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +125 °C
LPC2364FET100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2365FBD100	256	32	16	8	2	58	RMII	no	no	yes	-	6	1	–40 °C to +85 °C
LPC2366FBD100	256	32	16	8	2	58	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2367FBD100	512	32	16	8	2	58	RMII	no	yes	yes	-	6	1	–40 °C to +85 °C
LPC2368FBD100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1	–40 °C to +85 °C
LPC2368FET100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1	–40 °C to +85 °C

5. Block diagram



(1) LPC2367/68 only.

(2) LPC2364/66/68 only.

Fig 1. LPC2364/65/66/67/68 block diagram

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row J							
1	P0[28]/SCL0	2	P0[27]/SDA0	3	P0[29]/USB_D+	4	P1[19]/CAP1[1]
5	P1[22]/MAT1[0]	6	V_{SS}	7	P1[28]/PCAP1[0]/ MAT0[0]	8	P0[1]/TD1/RXD3/SCL1
9	P2[13]/$\overline{\text{EINT3}}$/ MCIDAT3/I2STX_SDA	10	P2[10]/$\overline{\text{EINT0}}$	11	-	12	-
Row K							
1	P3[26]/MAT0[1]/ PWM1[3]	2	$V_{DD(3V3)}$	3	V_{SS}	4	P1[20]/PWM1[2]/ SCK0
5	P1[23]/PWM1[4]/ MISO0	6	P1[26]/PWM1[6]/ CAP0[0]	7	P1[27]/CAP0[1]	8	P0[0]/RD1/TXD3/SDA1
9	P0[11]/RXD2/ SCL2/MAT3[1]	10	P2[12]/$\overline{\text{EINT2}}$/ MCIDAT2/I2STX_WS	11	-	12	-

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Ball	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 0 pins depends upon the pin function selected via the pin connect block. Pins 12, 13, 14, and 31 of this port are not available.
P0[0]/RD1/TXD3/ SDA1	46[1]	K8[1]	I/O	**P0[0] —** General purpose digital input/output pin.
			I	**RD1 —** CAN1 receiver input. (LPC2364/66/68 only)
			O	**TXD3 —** Transmitter output for UART3.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[1]/TD1/RXD3/ SCL1	47[1]	J8[1]	I/O	**P0[1] —** General purpose digital input/output pin.
			O	**TD1 —** CAN1 transmitter output. (LPC2364/66/68 only)
			I	**RXD3 —** Receiver input for UART3.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[2]/TXD0	98[1]	C4[1]	I/O	**P0[2] —** General purpose digital input/output pin.
			O	**TXD0 —** Transmitter output for UART0.
P0[3]/RXD0	99[1]	A2[1]	I/O	**P0[3] —** General purpose digital input/output pin.
			I	**RXD0 —** Receiver input for UART0.
P0[4]/ I2SRX_CLK/ RD2/CAP2[0]	81[1]	A8[1]	I/O	**P0[4] —** General purpose digital input/output pin.
			I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			I	**RD2 —** CAN2 receiver input. (LPC2364/66/68 only)
			I	**CAP2[0] —** Capture input for Timer 2, channel 0.
P0[5]/ I2SRX_WS/ TD2/CAP2[1]	80[1]	D7[1]	I/O	**P0[5] —** General purpose digital input/output pin.
			I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			O	**TD2 —** CAN2 transmitter output. (LPC2364/66/68 only)
			I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0]	79[1]	B8[1]	I/O	**P0[6] —** General purpose digital input/output pin.
			I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			I/O	**SSEL1 —** Slave Select for SSP1.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.
P0[7]/ I2STX_CLK/ SCK1/MAT2[1]	78[1]	A9[1]	I/O	**P0[7] —** General purpose digital input/output pin.
			I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			I/O	**SCK1 —** Serial Clock for SSP1.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/ I2STX_WS/ MISO1/MAT2[2]	77[1]	C8[1]	I/O	**P0[8] —** General purpose digital input/output pin.
			I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			O	**MAT2[2] —** Match output for Timer 2, channel 2.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
$\overline{\text{RSTOUT}}$	14	-	O	**$\overline{\text{RSTOUT}}$ —** This is a 3.3 V pin. LOW on this pin indicates LPC2364/65/66/67/68 being in Reset state. **Note:** This pin is available in LPC2364FBD100, LPC2365FBD100, LPC2366FBD100, LPC2367FBD100, and LPC2368FBD100 devices only (LQFP100 package).
$\overline{\text{RESET}}$	17[9]	F3[9]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	22[10][11]	H2[10][11]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	23[10][11]	G3[10][11]	O	Output from the oscillator amplifier.
RTCX1	16[10][12]	F2[10][12]	I	Input to the RTC oscillator circuit.
RTCX2	18[10]	G1[10]	O	Output from the RTC oscillator circuit.
V_{SS}	15, 31, 41, 55, 72, 97, 83[13]	B3, B7, C9, F1, G7, J6, K3 [13]	I	**ground:** 0 V reference.
V_{SSA}	11[14]	E1[14]	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	28, 54, 71, 96[15]	A3, C10, H9, K2[15]	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
$V_{DD(DCDC)(3V3)}$	13, 42, 84[16]	A7, E4, H6[16]	I	**3.3 V DC-to-DC converter supply voltage:** This is the supply voltage for the on-chip DC-to-DC converter only.
V_{DDA}	10[17]	E2[17]	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC.
VREF	12[17]	E3[17]	I	**ADC reference:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC.
VBAT	19[17]	G2[17]	I	**RTC pin power supply:** 3.3 V on this pin supplies the power to the RTC peripheral.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a DAC input, digital section of the pad is disabled.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[4] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[5] Pad provides digital I/O and USB functions (LPC2364/66/68 only). It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[6] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[7] This pin has no built-in pull-up and no built-in pull-down resistor.

[8] This pin has a built-in pull-up resistor.

[9] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[10] Pad provides special analog functionality.

[11] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

[12] If the RTC is not used, these pins can be left floating.

[13] Pad provides special analog functionality.

[14] Pad provides special analog functionality.

[15] Pad provides special analog functionality.

[16] Pad provides special analog functionality.

[17] Pad provides special analog functionality.

7. Functional description

7.1 Architectural overview

The LPC2364/65/66/67/68 microcontroller consists of an ARM7TDMI-S CPU with emulation support, the ARM7 local bus for closely coupled, high-speed access to the majority of on-chip memory, the AMBA AHB interfacing to high-speed on-chip peripherals, and the AMBA APB for connection to other on-chip peripheral functions. The microcontroller permanently configures the ARM7TDMI-S processor for little-endian byte order.

The LPC2364/65/66/67/68 implements two AHB in order to allow the Ethernet block to operate without interference caused by other system activity. The primary AHB, referred to as AHB1, includes the VIC and GPDMA controller.

The second AHB, referred to as AHB2, includes only the Ethernet block and an associated 16 kB SRAM. In addition, a bus bridge is provided that allows the secondary AHB to be a bus master on AHB1, allowing expansion of Ethernet buffer space into off-chip memory or unused space in memory residing on AHB1.

In summary, bus masters with access to AHB1 are the ARM7 itself, the GPDMA function, and the Ethernet block (via the bus bridge from AHB2). Bus masters with access to AHB2 are the ARM7 and the Ethernet block.

AHB peripherals are allocated a 2 MB range of addresses at the very top of the 4 GB ARM memory space. Each AHB peripheral is allocated a 16 kB address space within the AHB address space. Lower speed peripheral functions are connected to the APB. The AHB to APB bridge interfaces the APB to the AHB. APB peripherals are also allocated a 2 MB range of addresses, beginning at the 3.5 GB address point. Each APB peripheral is allocated a 16 kB address space within the APB address space.

The ARM7TDMI-S processor is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed complex instruction set computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

7.21.1 Features

- LPC2364/65/66/67/68 has one PWM block with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

7.22 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

7.22.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

7.24.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to ±1 % accuracy.

Upon power-up or any chip reset, the LPC2364/65/66/67/68 uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.24.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 7.24.2 for additional information.

7.24.1.3 RTC oscillator

The RTC oscillator can be used as the clock source for the RTC and/or the WDT. Also, the RTC oscillator can be used to drive the PLL and the CPU.

7.24.2 PLL

The PLL accepts an input clock frequency in the range of 32 kHz to 50 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and the USB block. The USB block is available in LPC2364/66/68 only.

The PLL input, in the range of 32 kHz to 50 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL input divider is the PLL multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value ‘M’, in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL is enabled by software only. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source.

7.24.3 Wake-up timer

The LPC2364/65/66/67/68 begins operation at power-up and when awakened from Power-down and Deep power-down modes by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down and Deep-power down modes, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The Wake-up Timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.24.4 Power control

The LPC2364/65/66/67/68 supports a variety of power control features. There are four special modes of processor power reduction: Idle mode, Sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The LPC2364/65/66/67/68 also implements a separate power domain in order to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small SRAM, referred to as the battery RAM.

7.24.4.1 Idle mode

In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.24.4.2 Sleep mode

In Sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later. The 32 kHz RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The CCLK and USB clock dividers automatically get reset to zero.

The Sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Sleep mode reduces chip power consumption to a very low value. The flash memory is left on in Sleep mode, allowing a very quick wake-up.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(DCDC)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(DCDC)(3V3)}$). Having the on-chip DC-to-DC converter powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC and the battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that may be used by external hardware to restore chip power and resume operation.

7.25 System control

7.25.1 Reset

Reset has four sources on the LPC2364/65/66/67/68: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset, and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, starts the Wake-up timer (see description in Section 7.24.3 “Wake-up timer”), causing reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the Boot Block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.25.2 Brownout detection

The LPC2364/65/66/67/68 includes 2-stage monitoring of the voltage on the $V_{DD(DCDC)(3V3)}$ pins. If this voltage falls below 2.95 V, the BOD asserts an interrupt signal to the Vectored Interrupt Controller. This signal can be enabled for interrupt in the Interrupt Enable Register in the VIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register.

The second stage of low-voltage detection asserts Reset to inactivate the LPC2364/65/66/67/68 when the voltage on the $V_{DD(DCDC)(3V3)}$ pins falls below 2.65 V. This Reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the power-on reset circuitry maintains the overall Reset.

Both the 2.95 V and 2.65 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.95 V detection to reliably interrupt, or a regularly executed event loop to sense the condition.

7.25.6 Memory mapping control

The memory mapping control alters the mapping of the interrupt vectors that appear at the beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the Boot ROM or the SRAM. This allows code running in different memory spaces to have control of the interrupts.

7.26 Emulation and debugging

The LPC2364/65/66/67/68 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on P2[0] to P2[9]. This means that all communication, timer, and interface peripherals residing on other pins are available during the development and debugging phase as they are when the application is run in the embedded system itself.

7.26.1 EmbeddedICE

The EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. The EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM7TDMI-S core present on the target system.

The ARM core has a Debug Communication Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The DCC is accessed as a coprocessor 14 by the program running on the ARM7TDMI-S core. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $1/6$ of the CPU clock (CCLK) for the JTAG interface to operate.

7.26.2 Embedded trace

Since the LPC2364/65/66/67/68 have significant amounts of on-chip memories, it is not possible to determine how the processor core is operating simply by observing the external pins. The ETM provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to a trace port. A software debugger allows configuration of the ETM using a JTAG interface and displays the trace information that has been captured.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external Trace Port Analyzer captures the trace information under software debugger control. The trace port can broadcast the Instruction trace information. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 6. Thermal characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	125	°C

Table 7. Thermal resistance value (C/W): ±15 %

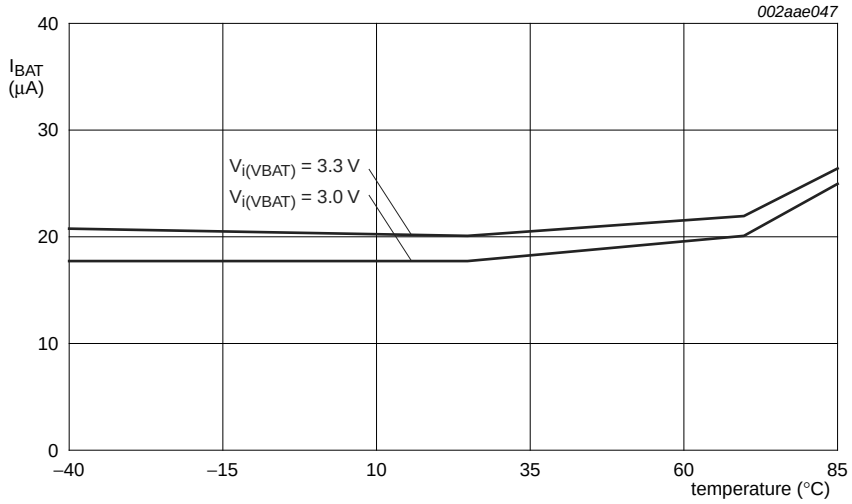
V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

LQFP100		**TFBGA100**	
θja		**θja**	
JEDEC (4.5 in × 4 in)		**JEDEC (4.5 in × 4 in)**	
0 m/s	37.3	0 m/s	53.9
1 m/s	32.2	1 m/s	45.5
2.5 m/s	29.5	2.5 m/s	39.5
Single-layer (4.5 in × 3 in)		**8-layer (4.5 in × 3 in)**	
0 m/s	54.4	0 m/s	44.3
1 m/s	42.9	1 m/s	39.2
2.5 m/s	38.8	2.5 m/s	34.2
θjc	6.7	θjc	9.4
θjb	12	θjb	10.8

Table 8. Static characteristics *…continued*

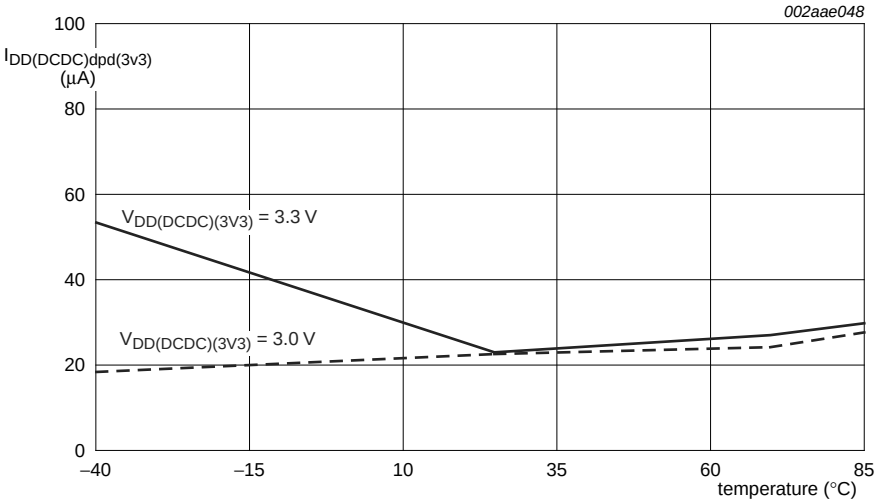
T_{amb} = −40 °C to +85 °C for standard devices, −40 °C to +125 °C for LPC2364HBD only, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	[5][6] [7][8]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[9]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[9]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[9]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[9]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[10]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[11]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; −40 °C to +85 °C		−15	−50	−85	μA
		V_I = 0 V; > 85 °C	[12]	−15	−50	−100	μA
		$V_{DD(3V3)} < V_I < 5$ V	[11]	0	0	0	μA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[9]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[13]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	1.8	1.95	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	1.8	1.95	V



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C

Fig 9. RTC battery maximum supply current I_{BAT} versus temperature in Deep power-down mode



$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 10. Total DC-to-DC converter maximum supply current $I_{DD(DCDC)dpd(3V3)}$ versus temperature in Deep power-down mode

11.4 Flash memory

Table 13. Dynamic characteristics of flash

T_{amb} = −40 °C to +85 °C for standard devices, −40 °C to +125 °C for LPC2364HBD only, unless otherwise specified; $V_{DD(3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered; < 100 cycles		10	-	-	years
		unpowered; < 100 cycles		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

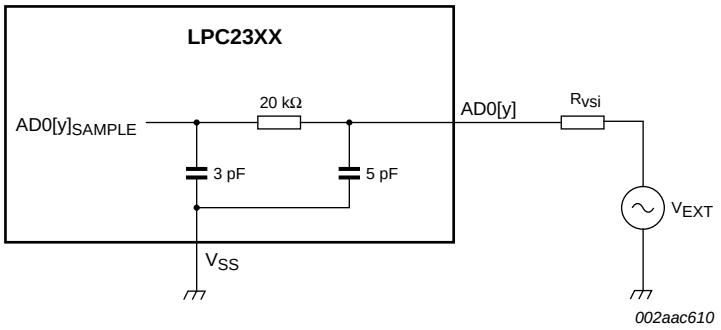


Fig 17. Suggested ADC interface - LPC2364/65/66/67/68 AD0[y] pin

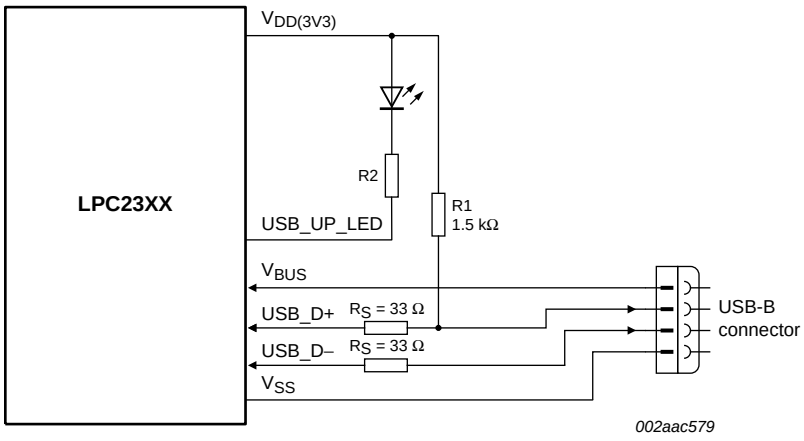


Fig 19. LPC2364/66/68 USB interface on a bus-powered device

14.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor C_i / (C_i + C_g). In slave mode, a minimum of 200 mV (RMS) is needed.

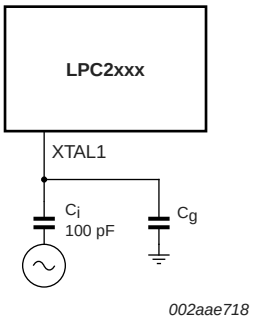


Fig 20. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 20), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTAL2 pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 21 and in Table 16 and Table 17. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 21 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

17. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2364_65_66_67_68 v.7.1	20131016	Product data sheet	-	LPC2364_65_66_67_68 v.7
Modifications:	• Table 4 “Pin description”, Table note 6: Changed glitch filter spec from 5 ns to 10 ns. • Table 9 “Dynamic characteristics”: Changed min clock cycle time from 42 to 40.			
LPC2364_65_66_67_68 v.7	20111020	Product data sheet	-	LPC2364_65_66_67_68 v.6
Modifications:	• Table 13 “Dynamic characteristics of flash”: Added characteristics for t_{er} and t_{prog}. • Table 4 “Pin description”: Updated description for USB_UP_LED. • Table 4 “Pin description”: Added Table note 12 “If the RTC is not used, these pins can be left floating.” for RTCX1 and RTCX2 pins. • Table 4 “Pin description”: Added Table note 8 “This pin has a built-in pull-up resistor.” for DBGEN, TMS, TDI, TRST, and RTCK pins. • Table 4 “Pin description”: Added Table note 7 “This pin has no built-in pull-up and no built-in pull-down resistor.” for TCK and TDO pins. • Table 5 “Limiting values”: Added “non-operating” to conditions column of T_{stg}. • Table 5 “Limiting values”: Updated Table note 5 “The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.”. • Table 5 “Limiting values”: Updated storage temperature min/max to −65/+150. • Added Table 7 “Thermal resistance value (C/W): ±15 %”. • Added Table 10 “Dynamic characteristic: internal oscillators”. • Added Table 11 “Dynamic characteristic: I/O pins[1]”. • Table 8 “Static characteristics”: Changed V_{hys} typ value from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$. • Table 13 “Dynamic characteristics of flash”: Updated table. • Added Section 9 “Thermal characteristics”. • Added Section 10.3 “Electrical pin characteristics”. • Added Section 14.2 “Crystal oscillator XTAL input and component selection”. • Added Section 14.3 “RTC 32 kHz oscillator component selection”. • Added Section 14.4 “XTAL and RTCX Printed Circuit Board (PCB) layout guidelines”. • Added Section 14.5 “Standard I/O pin configuration”. • Added Section 14.6 “Reset pin configuration”.			

Table 20. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2364_65_66_67_68 v.6	20100201	Product data sheet	-	LPC2364_65_66_67_68 v.5
Modifications:	• Table 5 “Limiting values”: Changed V_{ESD} min/max to −2500/+2500. • Table 6: Updated min, typical and max values for oscillator pins. • Table 6: Updated conditions and typical values for $I_{DD(DCDC)pd(3V3)}$, I_{BATact}; $I_{DD(DCDC)dpd(3V3)}$ and I_{BAT} added. • Table 9 “Dynamic characteristics of flash”: Changed flash endurance spec from 100000 to 10000 minimum cycles. • Added Table 11 “DAC electrical characteristics”. • Section 7.2 “On-chip flash programming memory”: Removed text regarding flash endurance minimum specs. • Added Section 7.24.4.4 “Deep power-down mode”. • Section 7.25.2 “Brownout detection”: Changed $V_{DD(3V3)}$ to $V_{DD(DCDC)(3V3)}$. • Added Section 9.2 “Deep power-down mode”. • Added Section 13.2 “XTAL1 input”. • Added Section 13.3 “XTAL and RTC Printed-Circuit Board (PCB) layout guidelines”. • Added table note for XTAL1 and XTAL2 pins in Table 3.			
LPC2364_65_66_67_68 v.5	20090409	Product data sheet	-	LPC2364_65_66_67_68 v.4
Modifications:	• Added part LPC2364HBD100. • Section 7.2: Added sentence clarifying SRAM speeds for LPC2364HBD. • Table 5: Updated V_{esd} min/max. • Table 6: Updated Z_{DRV} Table note [14]. • Table 6: V_{hys}, moved 0.4 from typ to min column. • Table 6: I_{pu}, added specs for >85 °C. • Table 6: Removed R_{pu}. • Table 7: CCLK and IRC, added specs for >85 °C. • Added Table 9. • Updated Figure 14. • Updated Figure 11.			
LPC2364_65_66_67_68 v.4	20080417	Product data sheet	-	LPC2364_66_68 v.3
LPC2364_66_68 v.3	20071220	Product data sheet	-	LPC2364_66_68 v.2
LPC2364_66_68 v.2	20071001	Preliminary data sheet	-	LPC2364_66_68 v.1
LPC2364_66_68 v.1	20070103	Preliminary data sheet	-	-

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