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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	Ethernet, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	70
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	58K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2365fbd100-551

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					Ethernet	USB device + 4 kB FIFO	SD/MMC	GP DMA	Channels			Temp range
		Local bus	Ethernet buffers	GP/USB	RTC	Total					CAN	ADC	DAC	
LPC2364FBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2364HBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +125 °C
LPC2364FET100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2365FBD100	256	32	16	8	2	58	RMII	no	no	yes	-	6	1	–40 °C to +85 °C
LPC2366FBD100	256	32	16	8	2	58	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2367FBD100	512	32	16	8	2	58	RMII	no	yes	yes	-	6	1	–40 °C to +85 °C
LPC2368FBD100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1	–40 °C to +85 °C
LPC2368FET100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1	–40 °C to +85 °C

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	TDO	2	P0[3]/RXD0	3	$V_{DD(3V3)}$	4	P1[4]/ENET_TX_EN
5	P1[10]/ENET_RXD1	6	P1[16]/ENET_MDC	7	$V_{DD(DCDC)(3V3)}$	8	P0[4]/I2SRX_CLK/ RD2/CAP2[0]
9	P0[7]/I2STX_CLK/ SCK1/MAT2[1]	10	P0[9]/I2STX_SDA/ MOSI1/MAT2[3]	11	-	12	-
Row B							
1	TMS	2	RTCK	3	V_{SS}	4	P1[1]/ENET_TXD1
5	P1[9]/ENET_RXD0	6	P1[17]/ ENET_MDIO	7	V_{SS}	8	P0[6]/I2SRX_SDA/ SSEL1/MAT2[0]
9	P2[0]/PWM1[1]/ TXD1/TRACECLK	10	P2[1]/PWM1[2]/ RXD1/PIPESTAT0	11	-	12	-
Row C							
1	TCK	2	$\overline{\text{TRST}}$	3	TDI	4	P0[2]/TXD0
5	P1[8]/ENET_CRS	6	P1[15]/ ENET_REF_CLK	7	P4[28]/MAT2[0]/ TXD3	8	P0[8]/I2STX_WS/ MISO1/MAT2[2]
9	V_{SS}	10	$V_{DD(3V3)}$	11	-	12	-
Row D							
1	P0[24]/AD0[1]/ I2SRX_WS/CAP3[1]	2	P0[25]/AD0[2]/ I2SRX_SDA/TXD3	3	P0[26]/AD0[3]/ AOUT/RXD3	4	DBGEN
5	P1[0]/ENET_TXD0	6	P1[14]/ENET_RX_ER	7	P0[5]/I2SRX_WS/ TD2/CAP2[1]	8	P2[2]/PWM1[3]/ CTS1/PIPESTAT1
9	P2[4]/PWM1[5]/ DSR1/TRACESYNC	10	P2[5]/PWM1[6]/ DTR1/TRACEPKT0	11	-	12	-
Row E							
1	V_{SSA}	2	V_{DDA}	3	VREF	4	$V_{DD(DCDC)(3V3)}$
5	P0[23]/AD0[0]/ I2SRX_CLK/CAP3[0]	6	P4[29]/MAT2[1]/ RXD3	7	P2[3]/PWM1[4]/ DCD1/PIPESTAT2	8	P2[6]/PCAP1[0]/RI1/ TRACEPKT1
9	P2[7]/RD2/ RTS1/TRACEPKT2	10	P2[8]/TD2/ TXD2/TRACEPKT3	11	-	12	-
Row F							
1	V_{SS}	2	RTCX1	3	$\overline{\text{RESET}}$	4	P1[31]/SCK1/ AD0[5]
5	P1[21]/PWM1[3]/ SSEL0	6	P0[18]/DCD1/ MOSI0/MOSI	7	P2[9]/USB_CONNECT/ RXD2/EXTIN0	8	P0[16]/RXD1/ SSEL0/SSEL
9	P0[17]/CTS1/ MISO0/MISO	10	P0[15]/TXD1/ SCK0/SCK	11	-	12	-
Row G							
1	RTCX2	2	VBAT	3	XTAL2	4	P0[30]/USB_D−
5	P1[25]/MAT1[1]	6	P1[29]/PCAP1[1]/ MAT0[1]	7	V_{SS}	8	P0[21]/RI1/ MCIPWR/RD1
9	P0[20]/DTR1/ MCICMD/SCL1	10	P0[19]/DSR1/ MCICLK/SDA1	11	-	12	-
Row H							

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row J							
1	P0[28]/SCL0	2	P0[27]/SDA0	3	P0[29]/USB_D+	4	P1[19]/CAP1[1]
5	P1[22]/MAT1[0]	6	V_{SS}	7	P1[28]/PCAP1[0]/ MAT0[0]	8	P0[1]/TD1/RXD3/SCL1
9	P2[13]/$\overline{\text{EINT3}}$/ MCIDAT3/I2STX_SDA	10	P2[10]/$\overline{\text{EINT0}}$	11	-	12	-
Row K							
1	P3[26]/MAT0[1]/ PWM1[3]	2	$V_{DD(3V3)}$	3	V_{SS}	4	P1[20]/PWM1[2]/ SCK0
5	P1[23]/PWM1[4]/ MISO0	6	P1[26]/PWM1[6]/ CAP0[0]	7	P1[27]/CAP0[1]	8	P0[0]/RD1/TXD3/SDA1
9	P0[11]/RXD2/ SCL2/MAT3[1]	10	P2[12]/$\overline{\text{EINT2}}$/ MCIDAT2/I2STX_WS	11	-	12	-

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Ball	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 0 pins depends upon the pin function selected via the pin connect block. Pins 12, 13, 14, and 31 of this port are not available.
P0[0]/RD1/TXD3/ SDA1	46[1]	K8[1]	I/O	**P0[0] —** General purpose digital input/output pin.
			I	**RD1 —** CAN1 receiver input. (LPC2364/66/68 only)
			O	**TXD3 —** Transmitter output for UART3.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[1]/TD1/RXD3/ SCL1	47[1]	J8[1]	I/O	**P0[1] —** General purpose digital input/output pin.
			O	**TD1 —** CAN1 transmitter output. (LPC2364/66/68 only)
			I	**RXD3 —** Receiver input for UART3.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[2]/TXD0	98[1]	C4[1]	I/O	**P0[2] —** General purpose digital input/output pin.
			O	**TXD0 —** Transmitter output for UART0.
P0[3]/RXD0	99[1]	A2[1]	I/O	**P0[3] —** General purpose digital input/output pin.
			I	**RXD0 —** Receiver input for UART0.
P0[4]/ I2SRX_CLK/ RD2/CAP2[0]	81[1]	A8[1]	I/O	**P0[4] —** General purpose digital input/output pin.
			I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			I	**RD2 —** CAN2 receiver input. (LPC2364/66/68 only)
			I	**CAP2[0] —** Capture input for Timer 2, channel 0.
P0[5]/ I2SRX_WS/ TD2/CAP2[1]	80[1]	D7[1]	I/O	**P0[5] —** General purpose digital input/output pin.
			I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			O	**TD2 —** CAN2 transmitter output. (LPC2364/66/68 only)
			I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0]	79[1]	B8[1]	I/O	**P0[6] —** General purpose digital input/output pin.
			I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			I/O	**SSEL1 —** Slave Select for SSP1.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.
P0[7]/ I2STX_CLK/ SCK1/MAT2[1]	78[1]	A9[1]	I/O	**P0[7] —** General purpose digital input/output pin.
			I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			I/O	**SCK1 —** Serial Clock for SSP1.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/ I2STX_WS/ MISO1/MAT2[2]	77[1]	C8[1]	I/O	**P0[8] —** General purpose digital input/output pin.
			I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			O	**MAT2[2] —** Match output for Timer 2, channel 2.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P0[21]/RI1/ MCIPWR/RD1	57[1]	G8[1]	I/O	**P0[21] —** General purpose digital input/output pin.
			I	**RI1 —** Ring Indicator input for UART1.
			O	**MCIPWR —** Power Supply Enable for external SD/MMC power supply. (LPC2367/68 only)
			I	**RD1 —** CAN1 receiver input. (LPC2364/66/68 only)
P0[22]/RTS1/ MCIDAT0/TD1	56[1]	H10[1]	I/O	**P0[22] —** General purpose digital input/output pin.
			O	**RTS1 —** Request to Send output for UART1.
			O	**MCIDAT0 —** Data line for SD/MMC interface. (LPC2367/68 only)
			O	**TD1 —** CAN1 transmitter output. (LPC2364/66/68 only)
P0[23]/AD0[0]/ I2SRX_CLK/ CAP3[0]	9[2]	E5[2]	I/O	**P0[23] —** General purpose digital input/output pin.
			I	**AD0[0] —** A/D converter 0, input 0.
			I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			I	**CAP3[0] —** Capture input for Timer 3, channel 0.
P0[24]/AD0[1]/ I2SRX_WS/ CAP3[1]	8[2]	D1[2]	I/O	**P0[24] —** General purpose digital input/output pin.
			I	**AD0[1] —** A/D converter 0, input 1.
			I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			I	**CAP3[1] —** Capture input for Timer 3, channel 1.
P0[25]/AD0[2]/ I2SRX_SDA/ TXD3	7[2]	D2[2]	I/O	**P0[25] —** General purpose digital input/output pin.
			I	**AD0[2] —** A/D converter 0, input 2.
			I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			O	**TXD3 —** Transmitter output for UART3.
P0[26]/AD0[3]/ AOUT/RXD3	6[3]	D3[3]	I/O	**P0[26] —** General purpose digital input/output pin.
			I	**AD0[3] —** A/D converter 0, input 3.
			O	**AOUT —** D/A converter output.
			I	**RXD3 —** Receiver input for UART3.
P0[27]/SDA0	25[4]	J2[4]	I/O	**P0[27] —** General purpose digital input/output pin. Output is open-drain.
			I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
P0[28]/SCL0	24[4]	J1[4]	I/O	**P0[28] —** General purpose digital input/output pin. Output is open-drain.
			I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
P0[29]/USB_D+	29[5]	J3[5]	I/O	**P0[29] —** General purpose digital input/output pin.
			I/O	**USB_D+ —** USB bidirectional D+ line. (LPC2364/66/68 only)
P0[30]/USB_D−	30[5]	G4[5]	I/O	**P0[30] —** General purpose digital input/output pin.
			I/O	**USB_D− —** USB bidirectional D− line. (LPC2364/66/68 only)
P1[0] to P1[31]			I/O	**Port 1:** Port 1 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 1 pins depends upon the pin function selected via the pin connect block. Pins 2, 3, 5, 6, 7, 11, 12, and 13 of this port are not available.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P2[3]/PWM1[4]/ DCD1/ PIPESTAT2	70[1]	E7[1]	I/O	**P2[3] —** General purpose digital input/output pin.
			O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
			I	**DCD1 —** Data Carrier Detect input for UART1.
			O	**PIPESTAT2 —** Pipeline Status, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACESYNC	69[1]	D9[1]	I/O	**P2[4] —** General purpose digital input/output pin.
			O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
			I	**DSR1 —** Data Set Ready input for UART1.
			O	**TRACESYNC —** Trace Synchronization.
P2[5]/PWM1[6]/ DTR1/ TRACEPKT0	68[1]	D10[1]	I/O	**P2[5] —** General purpose digital input/output pin.
			O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
			O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**TRACEPKT0 —** Trace Packet, bit 0.
P2[6]/PCAP1[0]/ RI1/ TRACEPKT1	67[1]	E8[1]	I/O	**P2[6] —** General purpose digital input/output pin.
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
			I	**RI1 —** Ring Indicator input for UART1.
			O	**TRACEPKT1 —** Trace Packet, bit 1.
P2[7]/RD2/ RTS1/ TRACEPKT2	66[1]	E9[1]	I/O	**P2[7] —** General purpose digital input/output pin.
			I	**RD2 —** CAN2 receiver input. (LPC2364/66/68 only)
			O	**RTS1 —** Request to Send output for UART1.
			O	**TRACEPKT2 —** Trace Packet, bit 2.
P2[8]/TD2/ TXD2/ TRACEPKT3	65[1]	E10[1]	I/O	**P2[8] —** General purpose digital input/output pin.
			O	**TD2 —** CAN2 transmitter output. (LPC2364/66/68 only)
			O	**TXD2 —** Transmitter output for UART2.
			O	**TRACEPKT3 —** Trace Packet, bit 3.
P2[9]/ USB_CONNECT/ RXD2/EXTIN0	64[1]	F7[1]	I/O	**P2[9] —** General purpose digital input/output pin.
			O	**USB_CONNECT —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. (LPC2364/66/68 only)
			I	**RXD2 —** Receiver input for UART2.
			I	**EXTIN0 —** External Trigger Input.
P2[10]/$\overline{\text{EINT0}}$	53[6]	J10[6]	I/O	**P2[10] —** General purpose digital input/output pin. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after a reset.
			I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
P2[11]/$\overline{\text{EINT1}}$/ MCIDAT1/ I2STX_CLK	52[6]	H8[6]	I/O	**P2[11] —** General purpose digital input/output pin.
			I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
			O	**MCIDAT1 —** Data line for SD/MMC interface. (LPC2367/68 only)
			I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
$\overline{\text{RSTOUT}}$	14	-	O	**$\overline{\text{RSTOUT}}$ —** This is a 3.3 V pin. LOW on this pin indicates LPC2364/65/66/67/68 being in Reset state. **Note:** This pin is available in LPC2364FBD100, LPC2365FBD100, LPC2366FBD100, LPC2367FBD100, and LPC2368FBD100 devices only (LQFP100 package).
$\overline{\text{RESET}}$	17[9]	F3[9]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	22[10][11]	H2[10][11]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	23[10][11]	G3[10][11]	O	Output from the oscillator amplifier.
RTCX1	16[10][12]	F2[10][12]	I	Input to the RTC oscillator circuit.
RTCX2	18[10]	G1[10]	O	Output from the RTC oscillator circuit.
V_{SS}	15, 31, 41, 55, 72, 97, 83[13]	B3, B7, C9, F1, G7, J6, K3 [13]	I	**ground:** 0 V reference.
V_{SSA}	11[14]	E1[14]	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	28, 54, 71, 96[15]	A3, C10, H9, K2[15]	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
$V_{DD(DCDC)(3V3)}$	13, 42, 84[16]	A7, E4, H6[16]	I	**3.3 V DC-to-DC converter supply voltage:** This is the supply voltage for the on-chip DC-to-DC converter only.
V_{DDA}	10[17]	E2[17]	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC.
VREF	12[17]	E3[17]	I	**ADC reference:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC.
VBAT	19[17]	G2[17]	I	**RTC pin power supply:** 3.3 V on this pin supplies the power to the RTC peripheral.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a DAC input, digital section of the pad is disabled.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[4] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[5] Pad provides digital I/O and USB functions (LPC2364/66/68 only). It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[6] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[7] This pin has no built-in pull-up and no built-in pull-down resistor.

[8] This pin has a built-in pull-up resistor.

[9] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[10] Pad provides special analog functionality.

[11] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set
- A 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

7.2 On-chip flash programming memory

The LPC2364/65/66/67/68 incorporate a 128 kB, 256 kB, and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port (UART0). The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field and firmware upgrades.

The flash memory is 128 bits wide and includes pre-fetching and buffering techniques to allow it to operate at SRAM speeds of 72 MHz. LPC2364HBD flash operates up to 72 MHz from −40 °C to +85 °C, up to 60 MHz from 85 °C to 125 °C.

7.3 On-chip SRAM

The LPC2364/65/66/67/68 include SRAM memory of 8 kB or 32 kB, reserved for the ARM processor exclusive use. This RAM may be used for code and/or data storage and may be accessed as 8 bits, 16 bits, and 32 bits.

A 16 kB SRAM block serving as a buffer for the Ethernet controller and an 8 kB SRAM used by the GPDMA controller or the USB device can be used both for data and code storage. The 2 kB RTC SRAM can be used for data storage only. The RTC SRAM is battery powered and retains the content in the absence of the main power supply.

7.4 Memory map

The LPC2364/65/66/67/68 memory map incorporates several distinct regions as shown in Figure 4.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (default), boot ROM, or SRAM (see Section 7.25.6).

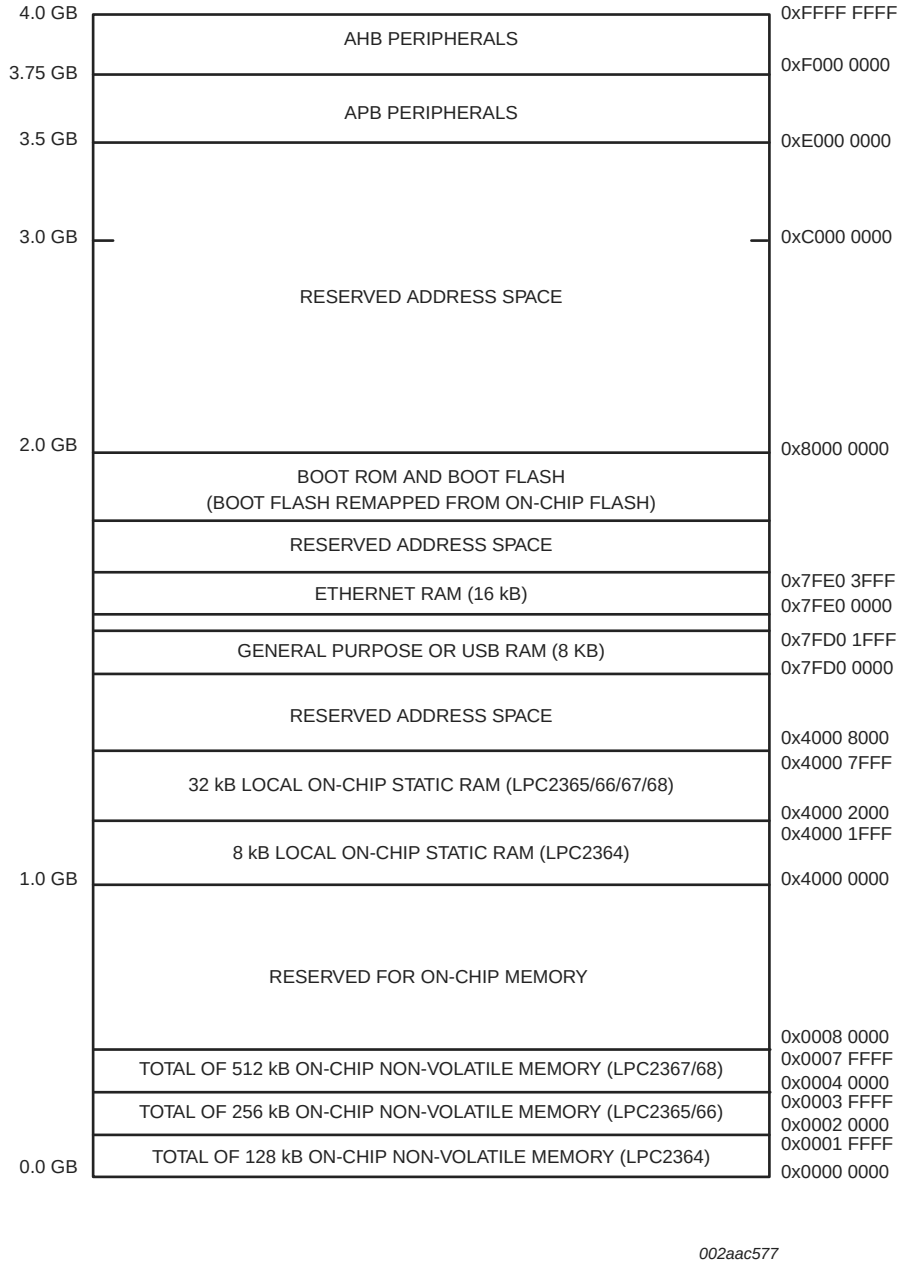


Fig 4. LPC2364/65/66/67/68 memory map

7.5 Interrupt controller

The ARM processor core has two interrupt inputs called Interrupt Request (IRQ) and Fast Interrupt Request (FIQ). The VIC takes 32 interrupt request inputs which can be programmed as FIQ or vectored IRQ types. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

- Double buffer implementation for Bulk and Isochronous endpoints.

7.11 CAN controller and acceptance filters (LPC2364/66/68 only)

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.11.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

7.12 10-bit ADC

The LPC2364/65/66/67/68 contain one ADC. It is a single 10-bit successive approximation ADC with six channels.

7.12.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 6 pins.
- Power-down mode.
- Measurement range 0 V to $V_{i(VREF)}$.
- 10-bit conversion time $\geq$ 2.44 μs.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the RTC clock, the Internal RC oscillator (IRC), or the APB peripheral clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring, for increased reliability.

7.23 RTC and battery RAM

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power in Power-down and Deep power-down modes. On the LPC2364/65/66/67/68, the RTC can be clocked by a separate 32.768 kHz oscillator, or by a programmable prescale divider based on the APB clock. Also, the RTC is powered by its own power supply pin, VBAT, which can be connected to a battery or to the same 3.3 V supply used by the rest of the device.

The VBAT pin supplies power only to the RTC and the battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery.

7.23.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values.
- 2 kB data SRAM powered by VBAT.
- RTC and battery RAM power supply is isolated from the rest of the chip.

7.24 Clocking and power control

7.24.1 Crystal oscillators

The LPC2364/65/66/67/68 includes three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2364/65/66/67/68 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

7.25.6 Memory mapping control

The memory mapping control alters the mapping of the interrupt vectors that appear at the beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the Boot ROM or the SRAM. This allows code running in different memory spaces to have control of the interrupts.

7.26 Emulation and debugging

The LPC2364/65/66/67/68 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on P2[0] to P2[9]. This means that all communication, timer, and interface peripherals residing on other pins are available during the development and debugging phase as they are when the application is run in the embedded system itself.

7.26.1 EmbeddedICE

The EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. The EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM7TDMI-S core present on the target system.

The ARM core has a Debug Communication Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The DCC is accessed as a coprocessor 14 by the program running on the ARM7TDMI-S core. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $1/6$ of the CPU clock (CCLK) for the JTAG interface to operate.

7.26.2 Embedded trace

Since the LPC2364/65/66/67/68 have significant amounts of on-chip memories, it is not possible to determine how the processor core is operating simply by observing the external pins. The ETM provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to a trace port. A software debugger allows configuration of the ETM using a JTAG interface and displays the trace information that has been captured.

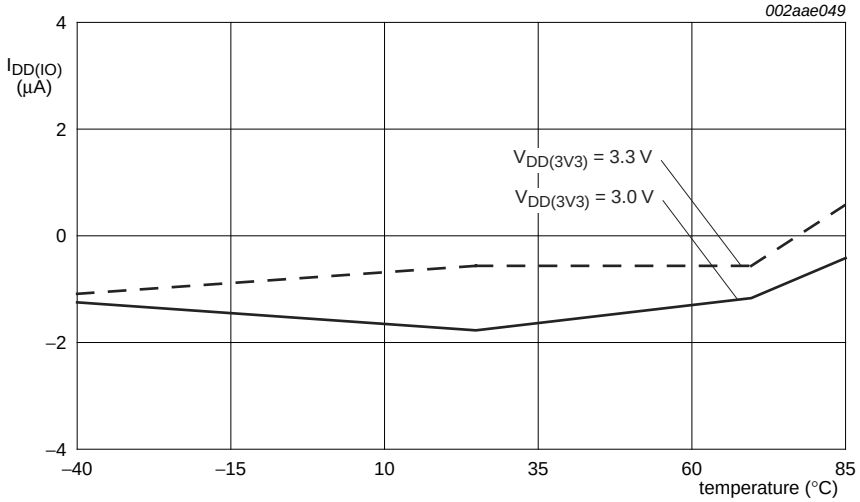
The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external Trace Port Analyzer captures the trace information under software debugger control. The trace port can broadcast the Instruction trace information. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers.

Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

7.26.3 RealMonitor

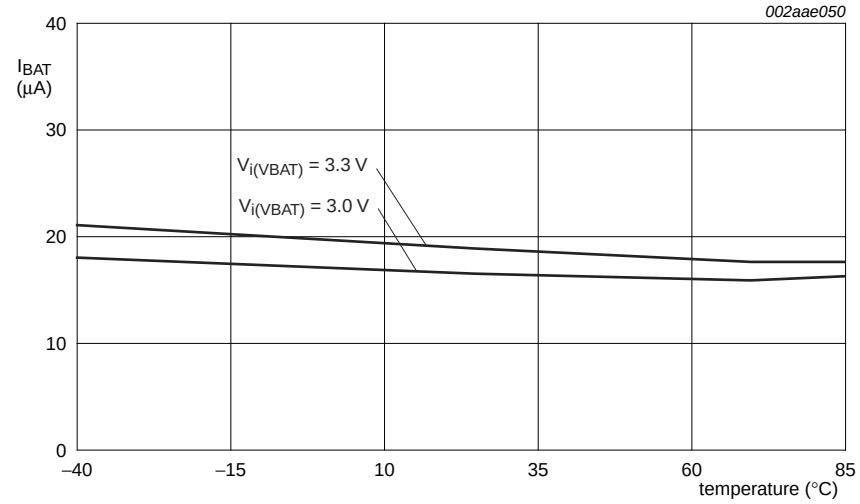
RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2364/65/66/67/68 contain a specific configuration of RealMonitor software programmed into the on-chip ROM memory.

10.1 Power-down mode



$V_{i(VBAT)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 5. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Power-down mode



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 6. RTC battery maximum supply current I_{BAT}versus temperature in Power-down mode

11.5 Timing

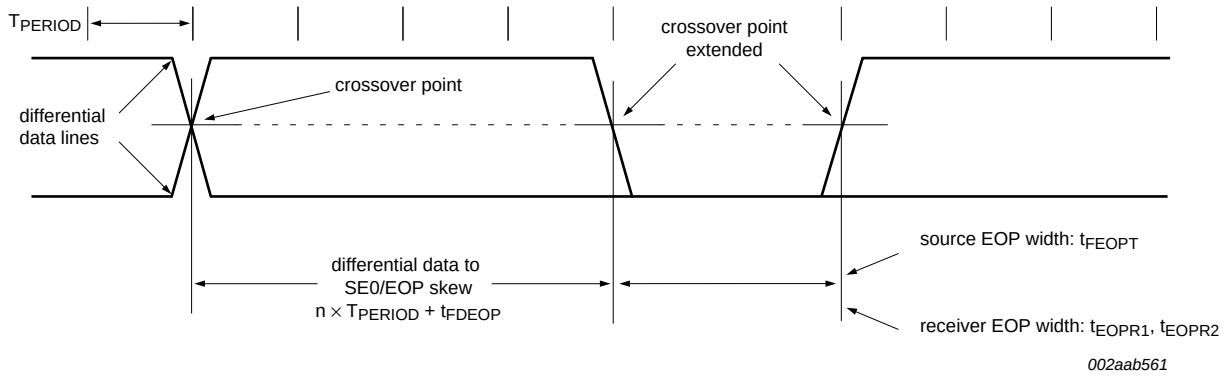


Fig 14. Differential data-to-EOP transition skew and EOP width

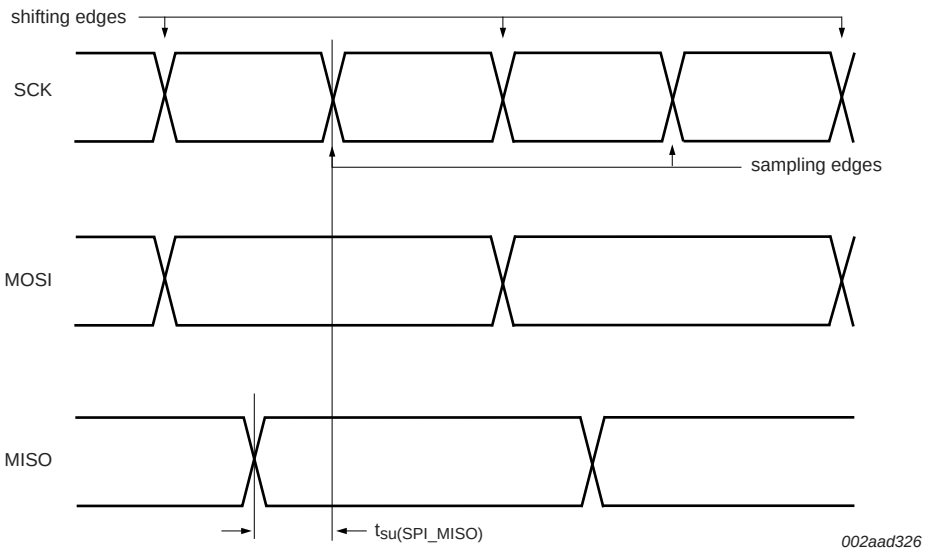
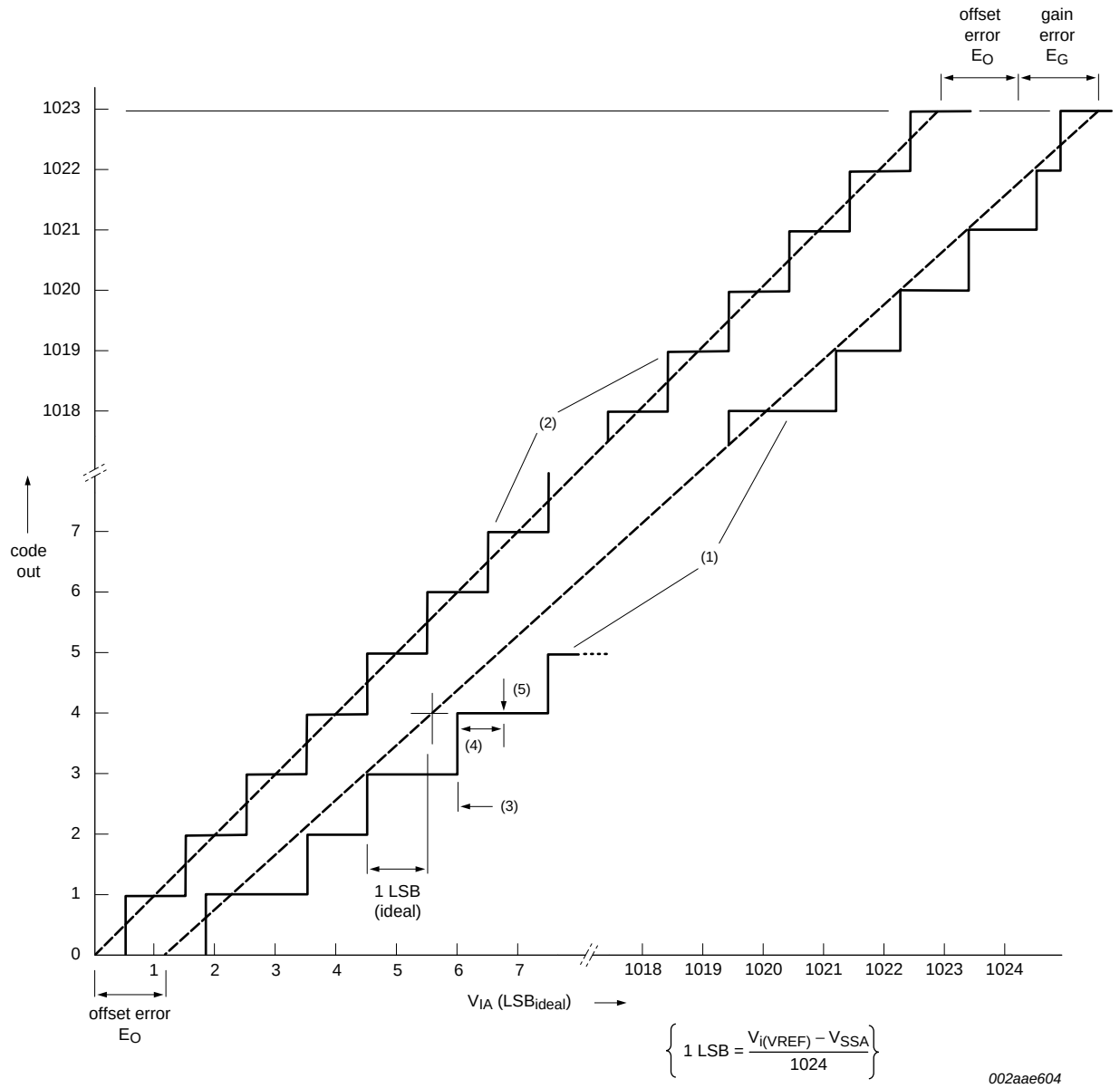


Fig 15. MISO line set-up time in SSP Master mode



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 16. ADC characteristics

13. DAC electrical characteristics

Table 15. DAC electrical characteristics

V_{DDA} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_D	differential linearity error		-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		-	±1.5	-	LSB
E_O	offset error		-	0.6	-	%
E_G	gain error		-	0.6	-	%
C_L	load capacitance		-	200	-	pF
R_L	load resistance		1	-	-	kΩ

14. Application information

14.1 Suggested USB interface solutions (LPC2364/66/68 only)

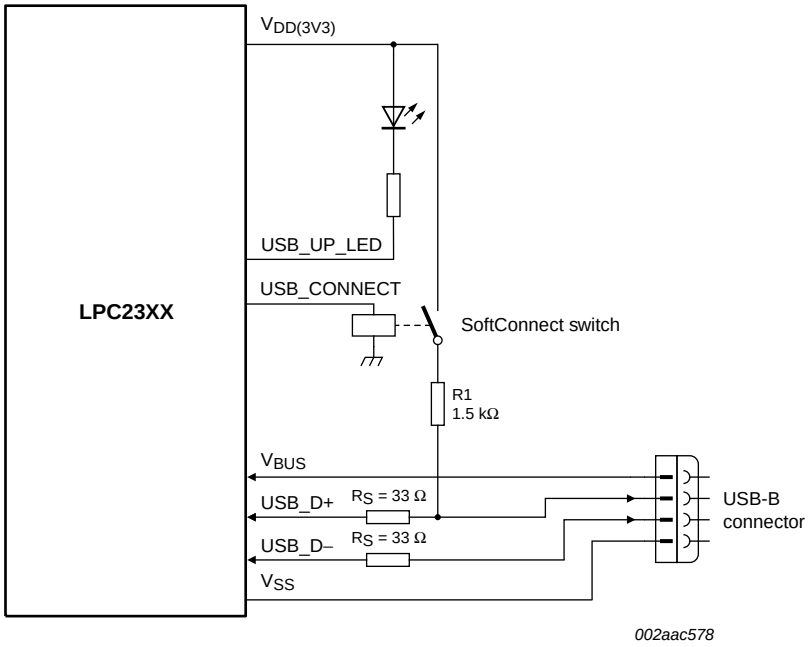


Fig 18. LPC2364/66/68 USB interface on a self-powered device

14.3 RTC 32 kHz oscillator component selection

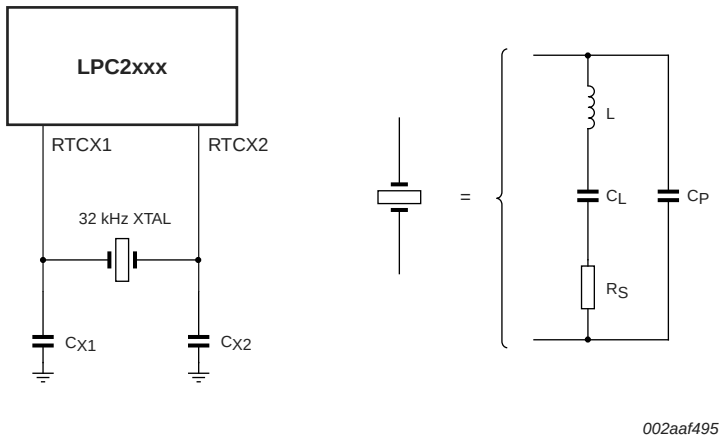


Fig 22. RTC oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

The RTC external oscillator circuit is shown in Figure 22. Since the feedback resistance is integrated on chip, only a crystal, the capacitances C_{X1} and C_{X2} need to be connected externally to the microcontroller.

Table 18 gives the crystal parameters that should be used. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual C_L influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in Table 18 that belong to a specific C_L. The value of external capacitances C_{X1} and C_{X2} specified in this table are calculated from the internal parasitic capacitances and the C_L. Parasitics from PCB and package are not taken into account.

Table 18. Recommended values for the RTC external 32 kHz oscillator C_{X1}/C_{X2} components

Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
11 pF	< 100 kΩ	18 pF, 18 pF
13 pF	< 100 kΩ	22 pF, 22 pF
15 pF	< 100 kΩ	27 pF, 27 pF

14.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

14.6 Reset pin configuration

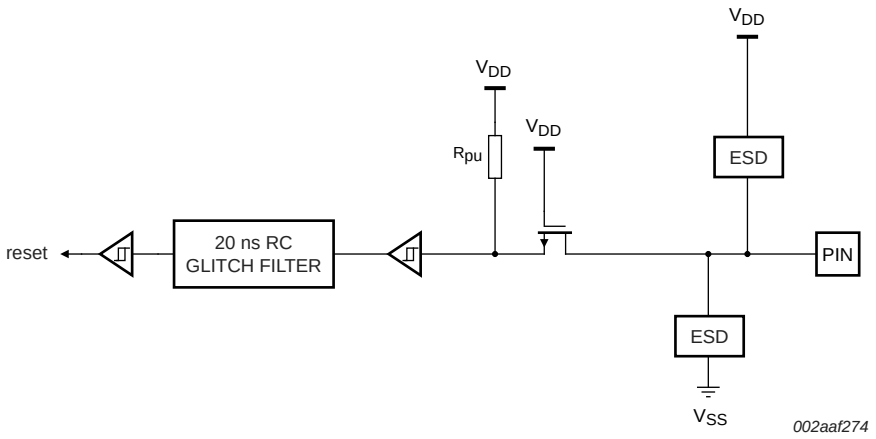
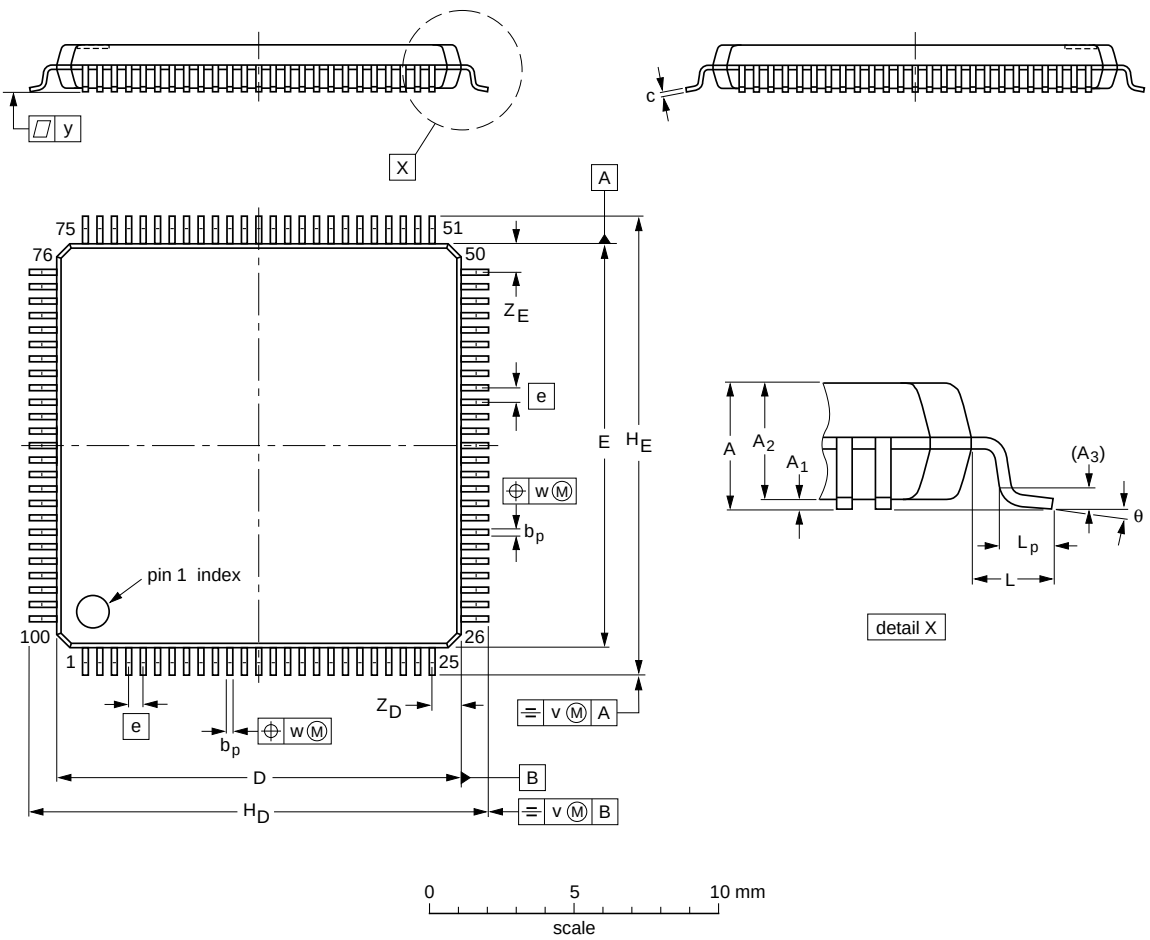


Fig 24. Reset pin configuration

15. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 25. Package outline SOT407-1 (LQFP100)