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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, Ethernet, I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	70
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	58K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2366fbd100-551

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					Ethernet	USB device + 4 kB FIFO	SD/MMC	GP DMA	Channels			Temp range
		Local bus	Ethernet buffers	GP/USB	RTC	Total					CAN	ADC	DAC	
LPC2364FBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2364HBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +125 °C
LPC2364FET100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2365FBD100	256	32	16	8	2	58	RMII	no	no	yes	-	6	1	–40 °C to +85 °C
LPC2366FBD100	256	32	16	8	2	58	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2367FBD100	512	32	16	8	2	58	RMII	no	yes	yes	-	6	1	–40 °C to +85 °C
LPC2368FBD100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1	–40 °C to +85 °C
LPC2368FET100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1	–40 °C to +85 °C

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	P1[30]/V_{BUS}/ AD0[4]	2	XTAL1	3	P3[25]/MAT0[0]/ PWM1[2]	4	P1[18]/USB_UP_LED/ PWM1[1]/CAP1[0]
5	P1[24]/PWM1[5]/ MOSI0	6	$V_{DD(DCDC)(3V3)}$	7	P0[10]/TXD2/ SDA2/MAT3[0]	8	P2[11]/$\overline{\text{EINT1}}$/ MCIDAT1/I2STX_CLK
9	$V_{DD(3V3)}$	10	P0[22]/RTS1/ MCIDAT0/TD1	11	-	12	-

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set
- A 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

7.2 On-chip flash programming memory

The LPC2364/65/66/67/68 incorporate a 128 kB, 256 kB, and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port (UART0). The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field and firmware upgrades.

The flash memory is 128 bits wide and includes pre-fetching and buffering techniques to allow it to operate at SRAM speeds of 72 MHz. LPC2364HBD flash operates up to 72 MHz from −40 °C to +85 °C, up to 60 MHz from 85 °C to 125 °C.

7.3 On-chip SRAM

The LPC2364/65/66/67/68 include SRAM memory of 8 kB or 32 kB, reserved for the ARM processor exclusive use. This RAM may be used for code and/or data storage and may be accessed as 8 bits, 16 bits, and 32 bits.

A 16 kB SRAM block serving as a buffer for the Ethernet controller and an 8 kB SRAM used by the GPDMA controller or the USB device can be used both for data and code storage. The 2 kB RTC SRAM can be used for data storage only. The RTC SRAM is battery powered and retains the content in the absence of the main power supply.

7.4 Memory map

The LPC2364/65/66/67/68 memory map incorporates several distinct regions as shown in Figure 4.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (default), boot ROM, or SRAM (see Section 7.25.6).

Additionally, any pin on Port 0 and Port 2 (total of 42 pins) providing a digital function can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake up the chip from Power-down mode.

7.8.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Backward compatibility with other earlier devices is maintained with legacy Port 0 and Port 1 registers appearing at the original addresses on the APB.

7.9 Ethernet

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share a dedicated AHB subsystem that is used to access the Ethernet SRAM for Ethernet data, control, and status information. All other AHB traffic in the LPC2364/65/66/67/68 takes place on a different AHB subsystem, effectively separating Ethernet activity from the rest of the system. The Ethernet DMA can also access the USB SRAM if it is not being used by the USB block.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.9.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with *IEEE standard 802.3*.
  - Fully compliant with 802.3x full duplex flow control and half duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:

- Receive filtering.
- Multicast and broadcast frame support for both transmit and receive.
- Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
- Selectable automatic transmit frame padding.
- Over-length frame support for both transmit and receive allows any length frames.
- Promiscuous receive mode.
- Automatic collision back-off and frame retransmission.
- Includes power management by clock switching.
- Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.

- Physical interface:
  - Attachment of external PHY chip through standard RMII interface.
  - PHY register access is available via the MIIM interface.

7.10 USB interface (LPC2364/66/68 only)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and a number (127 maximum) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, unplugging, and dynamic configuration of the devices. All transactions are initiated by the host controller.

7.10.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory, and the DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. The DMA controller when enabled transfers data between the endpoint buffer and the USB RAM.

7.10.2 Features

- Fully compliant with *USB 2.0 specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB USB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, LPC2364/65/66/67/68 can enter one of the reduced power modes and wake up on a USB activity.
- Supports DMA transfers with the DMA RAM of 8 kB on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.

7.18.1 Features

- I²C0 is a standard I²C compliant bus interface with open-drain pins.
- I²C1 and I²C2 use standard I/O pins and do not support powering off of individual devices connected to the same bus lines.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.

7.19 I²S-bus serial I/O controllers

The I²S-bus provides a standard communication interface for digital audio applications.

The *I²S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S connection has one master, which is always the master, and one slave. The I²S interface on the LPC2364/65/66/67/68 provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.19.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I²S input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S input and I²S output.

7.20 General purpose 32-bit timers/external event counters

The LPC2364/65/66/67/68 include four 32-bit Timer/Counters. The Timer/Counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The Timer/Counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.20.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit prescaler.
- Counter or Timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.21 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2364/65/66/67/68. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

On the wake-up of Sleep mode, if the IRC was used before entering Sleep mode, the code execution and peripherals activities will resume after 4 cycles expire. If the main external oscillator was used, the code execution will resume when 4096 cycles expire.

The customers need to reconfigure the PLL and clock dividers accordingly.

7.24.4.3 Power-down mode

Power-down mode does everything that Sleep mode does, but also turns off the IRC oscillator and the flash memory. This saves more power, but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 4 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. The customers need to reconfigure the PLL and clock dividers accordingly.

7.24.4.4 Deep power-down mode

Deep power-down mode is similar to the Power-down mode, but now the on-chip regulator that supplies power to the internal logic is also shut off. This produces the lowest possible power consumption without removing power from the entire chip. Since the Deep power-down mode shuts down the on-chip logic power supply, there is no register or memory retention, and resumption of operation involves the same activities as a full chip reset.

If power is supplied to the LPC2364/65/66/67/68 during Deep power-down mode, wake-up can be caused by the RTC Alarm interrupt or by external Reset.

While in Deep power-down mode, external device power may be removed. In this case, the LPC2364/65/66/67/68 will start up when external power is restored.

Essential data may be retained through Deep power-down mode (or through complete powering off of the chip) by storing data in the Battery RAM, as long as the external power to the VBAT pin is maintained.

7.24.4.5 Power domains

The LPC2364/65/66/67/68 provides two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the battery RAM.

On the LPC2364/65/66/67/68, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(DCDC)(3V3)}$ pin powers the on-chip DC-to-DC converter which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC2364/65/66/67/68 application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(DCDC)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(DCDC)(3V3)}$). Having the on-chip DC-to-DC converter powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC and the battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that may be used by external hardware to restore chip power and resume operation.

7.25 System control

7.25.1 Reset

Reset has four sources on the LPC2364/65/66/67/68: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset, and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, starts the Wake-up timer (see description in Section 7.24.3 “Wake-up timer”), causing reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the Boot Block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.25.2 Brownout detection

The LPC2364/65/66/67/68 includes 2-stage monitoring of the voltage on the $V_{DD(DCDC)(3V3)}$ pins. If this voltage falls below 2.95 V, the BOD asserts an interrupt signal to the Vectored Interrupt Controller. This signal can be enabled for interrupt in the Interrupt Enable Register in the VIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register.

The second stage of low-voltage detection asserts Reset to inactivate the LPC2364/65/66/67/68 when the voltage on the $V_{DD(DCDC)(3V3)}$ pins falls below 2.65 V. This Reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the power-on reset circuitry maintains the overall Reset.

Both the 2.95 V and 2.65 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.95 V detection to reliably interrupt, or a regularly executed event loop to sense the condition.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	core and external rail		3.0	3.6	V
$V_{DD(DCDC)(3V3)}$	DC-to-DC converter supply voltage (3.3 V)			3.0	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			−0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		−0.5	+4.6	V
$V_{i(VREF)}$	input voltage on pin VREF			−0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		−0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(3V3)}$ supply voltage is present	[2]	−0.5	+6.0	V
		other I/O pins	[2][3]	−0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current	per supply pin	[4]	-	100	mA
I_{SS}	ground current	per ground pin	[4]	-	100	mA
T_{stg}	storage temperature	non-operating	[5]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[6]	−2500	+2500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The peak current is limited to 25 times the corresponding maximum current.

[5] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for standard devices, −40 °C to +125 °C for LPC2364HBD only, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
USB pins (LPC2364/66/68 only)							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V		-	-	±10	μA
V_{BUS}	bus supply voltage			-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V		-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND		2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND		-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[14]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[3] $V_{DD(DCDC)(3V3)}$ = 3.3 V; $V_{DD(3V3)}$ = 3.3 V; $V_{i(VBAT)}$ = 3.3 V; T_{amb} = 25 °C.

[4] On pin VBAT.

[5] Including voltage on outputs in 3-state mode.

[6] $V_{DD(3V3)}$ supply voltages must be present.

[7] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[8] Please also see the errata note in errata sheet.

[9] Accounts for 100 mV voltage drop in all supply lines.

[10] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

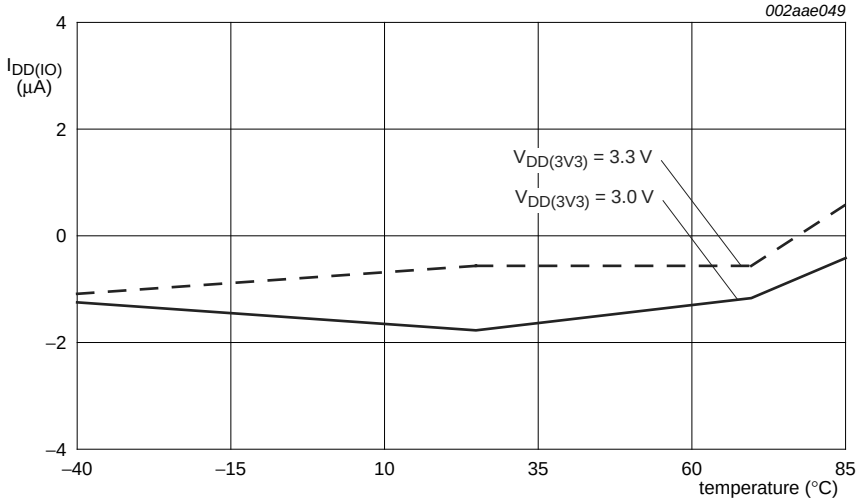
[11] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[12] LPC2364HBD only.

[13] To V_{SS}.

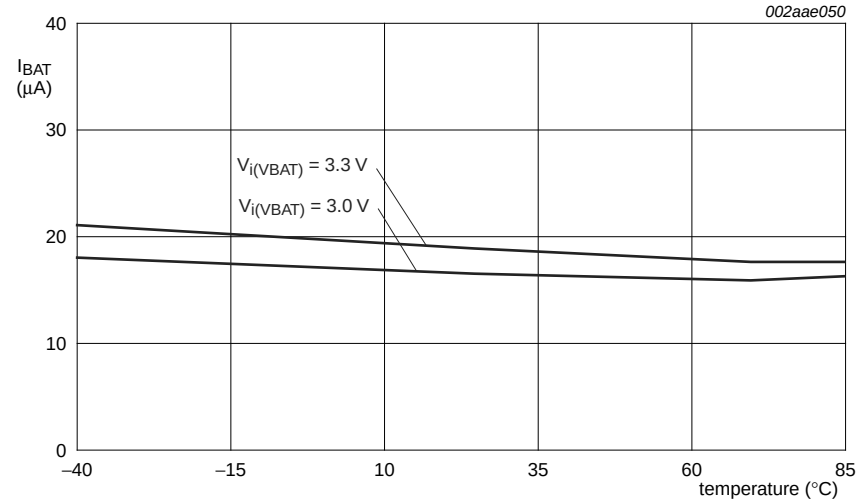
[14] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

10.1 Power-down mode



$V_{i(VBAT)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

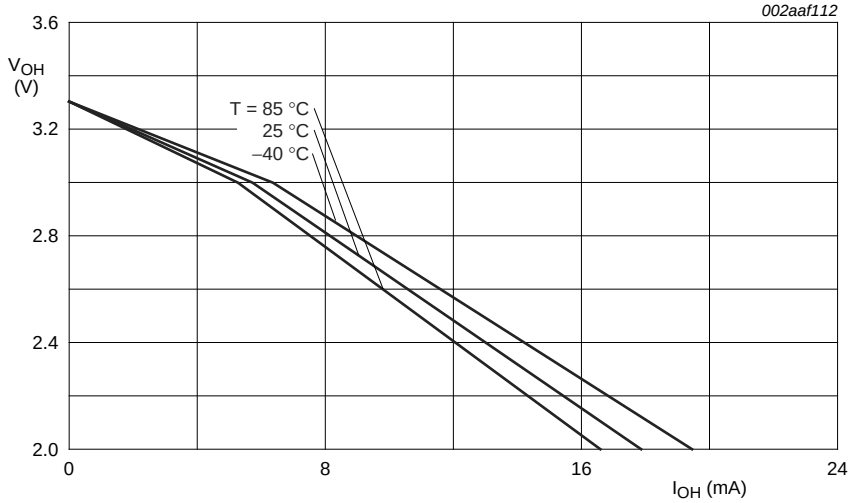
Fig 5. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Power-down mode



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

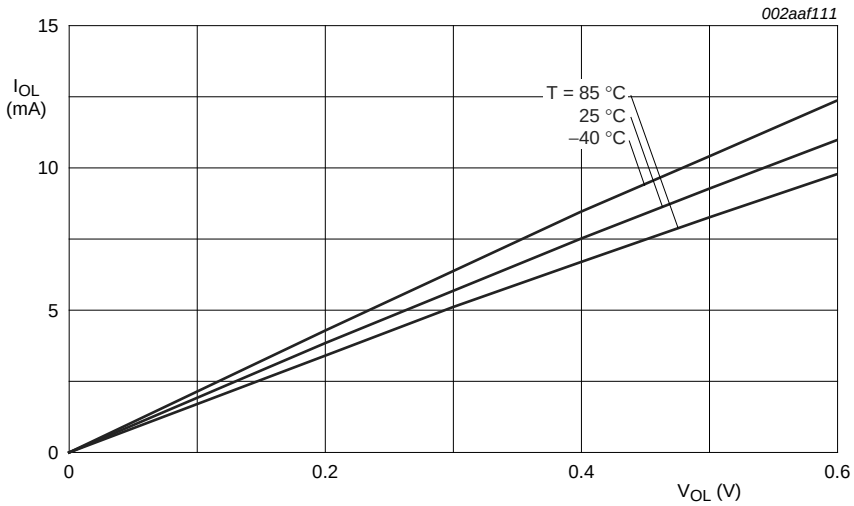
Fig 6. RTC battery maximum supply current I_{BAT}versus temperature in Power-down mode

10.3 Electrical pin characteristics



Conditions: $V_{DD(3V3)}$ = 3.3 V; standard port pins.

Fig 11. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: $V_{DD(3V3)}$ = 3.3 V; standard port pins.

Fig 12. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

11.5 Timing

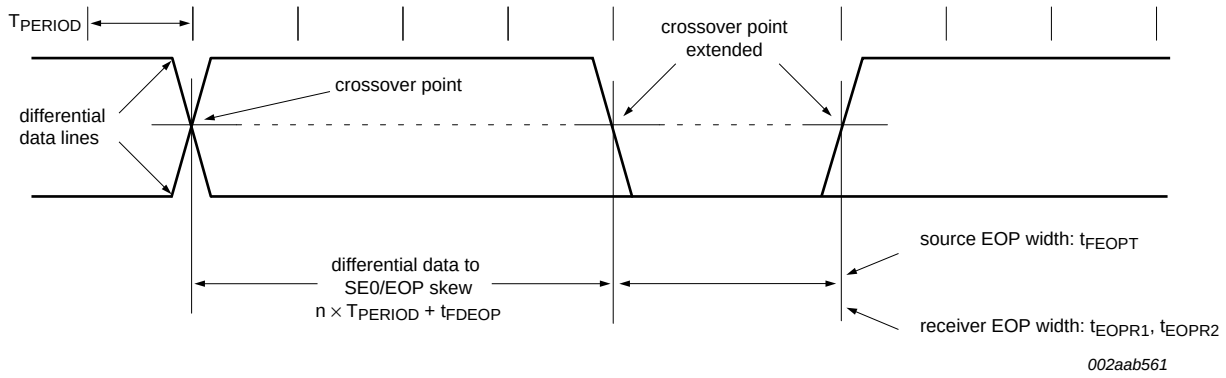


Fig 14. Differential data-to-EOP transition skew and EOP width

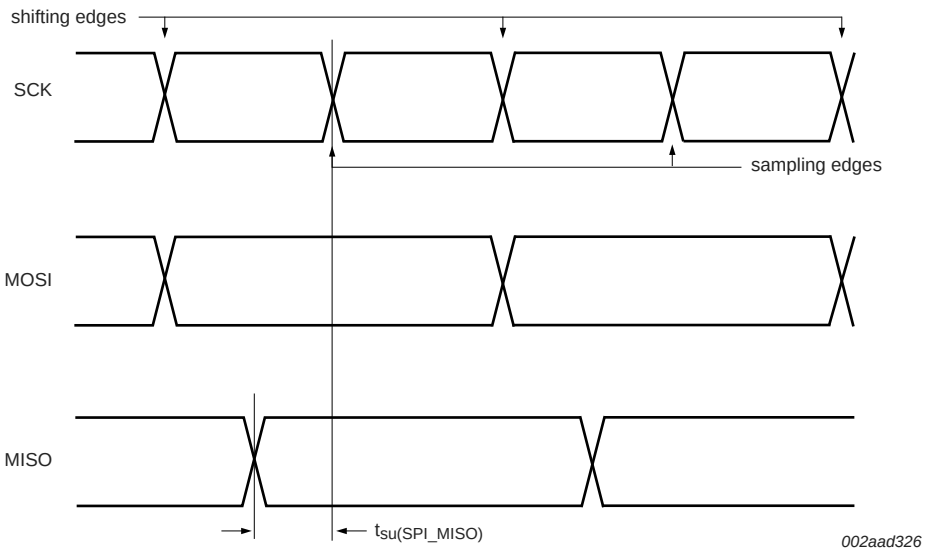
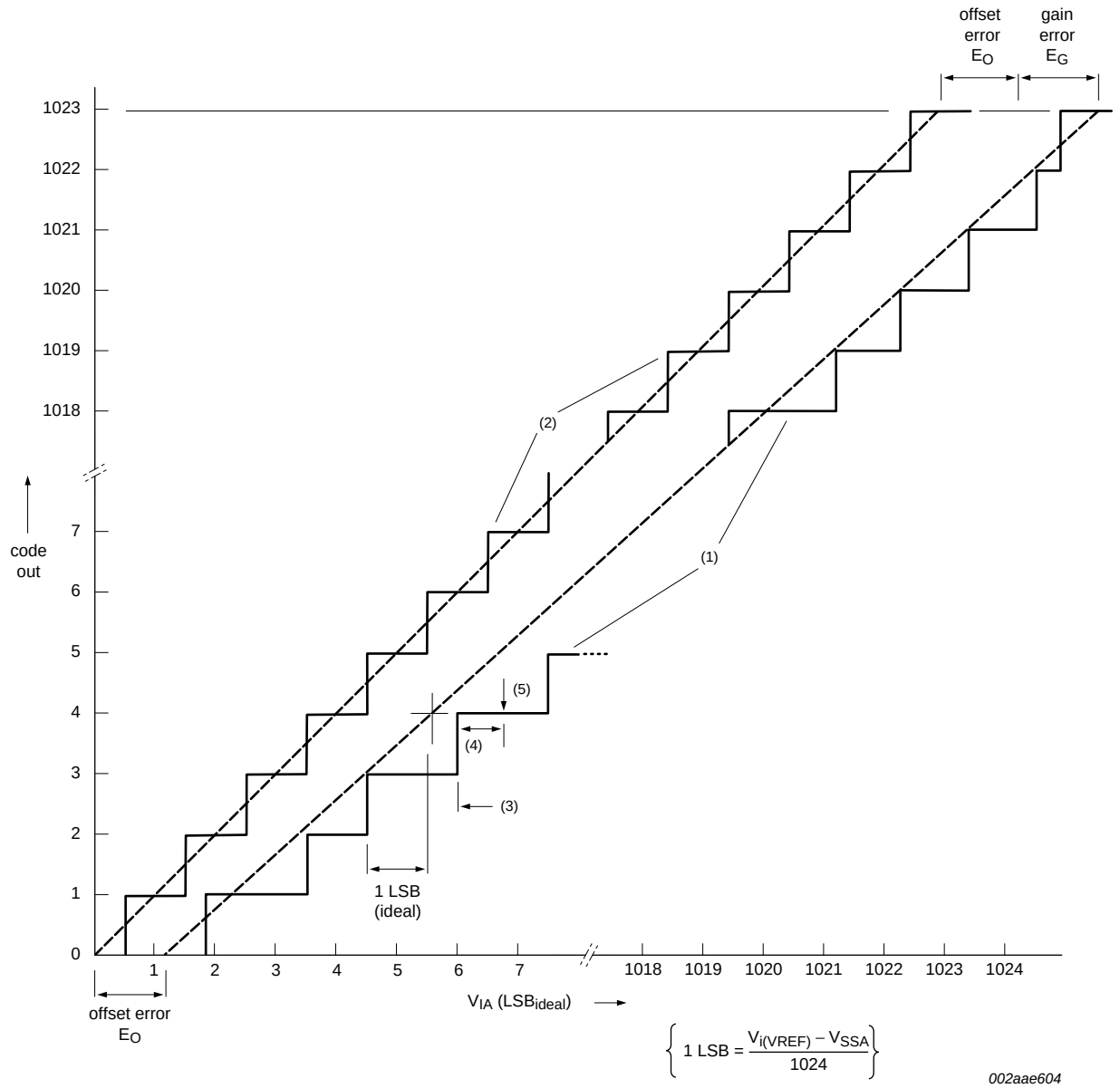


Fig 15. MISO line set-up time in SSP Master mode



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 16. ADC characteristics

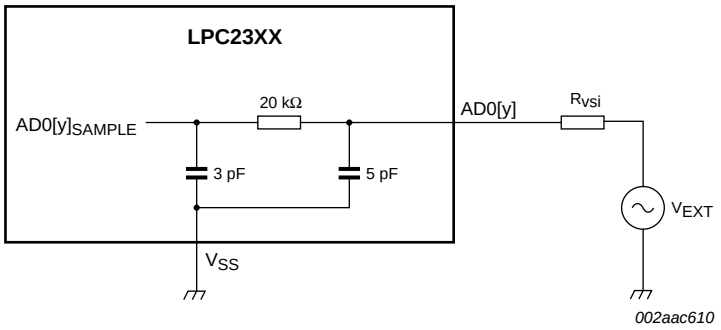


Fig 17. Suggested ADC interface - LPC2364/65/66/67/68 AD0[y] pin

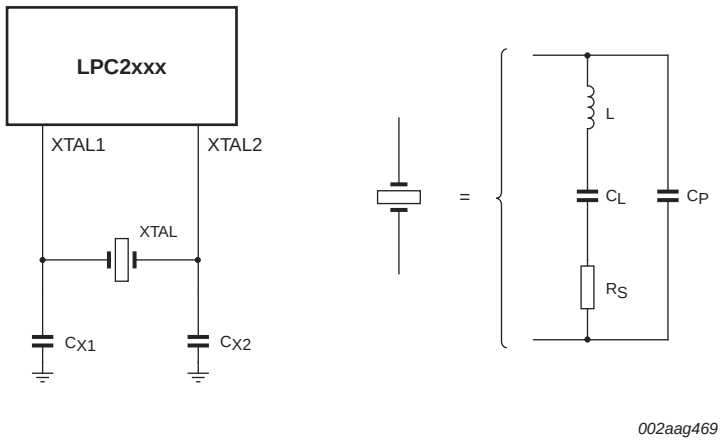


Fig 21. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 16. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 17. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

17. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2364_65_66_67_68 v.7.1	20131016	Product data sheet	-	LPC2364_65_66_67_68 v.7
Modifications:	• Table 4 “Pin description”, Table note 6: Changed glitch filter spec from 5 ns to 10 ns. • Table 9 “Dynamic characteristics”: Changed min clock cycle time from 42 to 40.			
LPC2364_65_66_67_68 v.7	20111020	Product data sheet	-	LPC2364_65_66_67_68 v.6
Modifications:	• Table 13 “Dynamic characteristics of flash”: Added characteristics for t_{er} and t_{prog}. • Table 4 “Pin description”: Updated description for USB_UP_LED. • Table 4 “Pin description”: Added Table note 12 “If the RTC is not used, these pins can be left floating.” for RTCX1 and RTCX2 pins. • Table 4 “Pin description”: Added Table note 8 “This pin has a built-in pull-up resistor.” for DBGEN, TMS, TDI, TRST, and RTCK pins. • Table 4 “Pin description”: Added Table note 7 “This pin has no built-in pull-up and no built-in pull-down resistor.” for TCK and TDO pins. • Table 5 “Limiting values”: Added “non-operating” to conditions column of T_{stg}. • Table 5 “Limiting values”: Updated Table note 5 “The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.”. • Table 5 “Limiting values”: Updated storage temperature min/max to −65/+150. • Added Table 7 “Thermal resistance value (C/W): ±15 %”. • Added Table 10 “Dynamic characteristic: internal oscillators”. • Added Table 11 “Dynamic characteristic: I/O pins[1]”. • Table 8 “Static characteristics”: Changed V_{hys} typ value from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$. • Table 13 “Dynamic characteristics of flash”: Updated table. • Added Section 9 “Thermal characteristics”. • Added Section 10.3 “Electrical pin characteristics”. • Added Section 14.2 “Crystal oscillator XTAL input and component selection”. • Added Section 14.3 “RTC 32 kHz oscillator component selection”. • Added Section 14.4 “XTAL and RTCX Printed Circuit Board (PCB) layout guidelines”. • Added Section 14.5 “Standard I/O pin configuration”. • Added Section 14.6 “Reset pin configuration”.			

Table 20. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2364_65_66_67_68 v.6	20100201	Product data sheet	-	LPC2364_65_66_67_68 v.5
Modifications:	• Table 5 “Limiting values”: Changed V_{ESD} min/max to −2500/+2500. • Table 6: Updated min, typical and max values for oscillator pins. • Table 6: Updated conditions and typical values for $I_{DD(DCDC)pd(3V3)}$, I_{BATact}; $I_{DD(DCDC)dpd(3V3)}$ and I_{BAT} added. • Table 9 “Dynamic characteristics of flash”: Changed flash endurance spec from 100000 to 10000 minimum cycles. • Added Table 11 “DAC electrical characteristics”. • Section 7.2 “On-chip flash programming memory”: Removed text regarding flash endurance minimum specs. • Added Section 7.24.4.4 “Deep power-down mode”. • Section 7.25.2 “Brownout detection”: Changed $V_{DD(3V3)}$ to $V_{DD(DCDC)(3V3)}$. • Added Section 9.2 “Deep power-down mode”. • Added Section 13.2 “XTAL1 input”. • Added Section 13.3 “XTAL and RTC Printed-Circuit Board (PCB) layout guidelines”. • Added table note for XTAL1 and XTAL2 pins in Table 3.			
LPC2364_65_66_67_68 v.5	20090409	Product data sheet	-	LPC2364_65_66_67_68 v.4
Modifications:	• Added part LPC2364HBD100. • Section 7.2: Added sentence clarifying SRAM speeds for LPC2364HBD. • Table 5: Updated V_{esd} min/max. • Table 6: Updated Z_{DRV} Table note [14]. • Table 6: V_{hys}, moved 0.4 from typ to min column. • Table 6: I_{pu}, added specs for >85 °C. • Table 6: Removed R_{pu}. • Table 7: CCLK and IRC, added specs for >85 °C. • Added Table 9. • Updated Figure 14. • Updated Figure 11.			
LPC2364_65_66_67_68 v.4	20080417	Product data sheet	-	LPC2364_66_68 v.3
LPC2364_66_68 v.3	20071220	Product data sheet	-	LPC2364_66_68 v.2
LPC2364_66_68 v.2	20071001	Preliminary data sheet	-	LPC2364_66_68 v.1
LPC2364_66_68 v.1	20070103	Preliminary data sheet	-	-

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