**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM7® |
| Core Size | 16/32-Bit |
| Speed | 72MHz |
| Connectivity | CANbus, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 70 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 58K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x10b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TFBGA |
| Supplier Device Package | 100-TFBGA (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2368fet100-518 |

**Table 4. Pin description** *…continued*

| Symbol | Pin | Ball | Type | Description |
|---|---|---|---|---|
| P1[23]/PWM1[4]/ MISO0 | 37[1] | K5[1] | I/O | **P1[23] —** General purpose digital input/output pin. |
| | | | O | **PWM1[4] —** Pulse Width Modulator 1, channel 4 output. |
| | | | I/O | **MISO0 —** Master In Slave Out for SSP0. |
| P1[24]/PWM1[5]/ MOSI0 | 38[1] | H5[1] | I/O | **P1[24] —** General purpose digital input/output pin. |
| | | | O | **PWM1[5] —** Pulse Width Modulator 1, channel 5 output. |
| | | | I/O | **MOSI0 —** Master Out Slave in for SSP0. |
| P1[25]/MAT1[1] | 39[1] | G5[1] | I/O | **P1[25] —** General purpose digital input/output pin. |
| | | | O | **MAT1[1] —** Match output for Timer 1, channel 1. |
| P1[26]/PWM1[6]/ CAP0[0] | 40[1] | K6[1] | I/O | **P1[26] —** General purpose digital input/output pin. |
| | | | O | **PWM1[6] —** Pulse Width Modulator 1, channel 6 output. |
| | | | I | **CAP0[0] —** Capture input for Timer 0, channel 0. |
| P1[27]/CAP0[1] | 43[1] | K7[1] | I/O | **P1[27] —** General purpose digital input/output pin. |
| | | | I | **CAP0[1] —** Capture input for Timer 0, channel 1. |
| P1[28]/ PCAP1[0]/ MAT0[0] | 44[1] | J7[1] | I/O | **P1[28] —** General purpose digital input/output pin. |
| | | | I | **PCAP1[0] —** Capture input for PWM1, channel 0. |
| | | | O | **MAT0[0] —** Match output for Timer 0, channel 0. |
| P1[29]/ PCAP1[1]/ MAT0[1] | 45[1] | G6[1] | I/O | **P1[29] —** General purpose digital input/output pin. |
| | | | I | **PCAP1[1] —** Capture input for PWM1, channel 1. |
| | | | O | **MAT0[1] —** Match output for Timer 0, channel 0. |
| P1[30]/$V_{BUS}$/ AD0[4] | 21[2] | H1[2] | I/O | **P1[30] —** General purpose digital input/output pin. |
| | | | I | **$V_{BUS}$ —** Monitors the presence of USB bus power. (LPC2364/66/68 only)<br>**Note:** This signal must be HIGH for USB reset to occur. |
| | | | I | **AD0[4] —** A/D converter 0, input 4. |
| P1[31]/SCK1/ AD0[5] | 20[2] | F4[2] | I/O | **P1[31] —** General purpose digital input/output pin. |
| | | | I/O | **SCK1 —** Serial Clock for SSP1. |
| | | | I | **AD0[5] —** A/D converter 0, input 5. |
| P2[0] to P2[31] | | | I/O | **Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 2 pins depends upon the pin function selected via the pin connect block. Pins 14 through 31 of this port are not available. |
| P2[0]/PWM1[1]/ TXD1/ TRACECLK | 75[1] | B9[1] | I/O | **P2[0] —** General purpose digital input/output pin. |
| | | | O | **PWM1[1] —** Pulse Width Modulator 1, channel 1 output. |
| | | | O | **TXD1 —** Transmitter output for UART1. |
| | | | O | **TRACECLK —** Trace Clock. |
| P2[1]/PWM1[2]/ RXD1/ PIPESTAT0 | 74[1] | B10[1] | I/O | **P2[1] —** General purpose digital input/output pin. |
| | | | O | **PWM1[2] —** Pulse Width Modulator 1, channel 2 output. |
| | | | I | **RXD1 —** Receiver input for UART1. |
| | | | O | **PIPESTAT0 —** Pipeline Status, bit 0. |
| P2[2]/PWM1[3]/ CTS1/ PIPESTAT1 | 73[1] | D8[1] | I/O | **P2[2] —** General purpose digital input/output pin. |
| | | | O | **PWM1[3] —** Pulse Width Modulator 1, channel 3 output. |
| | | | I | **CTS1 —** Clear to Send input for UART1. |
| | | | O | **PIPESTAT1 —** Pipeline Status, bit 1. |

**Table 4. Pin description** *…continued*

| Symbol | Pin | Ball | Type | Description |
|---|---|---|---|---|
| P2[12]/EINT2/ MCIDAT2/ I2STX_WS | 51[6] | K10[6] | I/O | **P2[12] —** General purpose digital input/output pin. |
| | | | I | **EINT2 —** External interrupt 2 input. |
| | | | O | **MCIDAT2 —** Data line for SD/MMC interface. (LPC2367/68 only) |
| | | | I/O | **I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. |
| P2[13]/EINT3/ MCIDAT3/ I2STX_SDA | 50[6] | J9[6] | I/O | **P2[13] —** General purpose digital input/output pin. |
| | | | I | **EINT3 —** External interrupt 3 input. |
| | | | O | **MCIDAT3 —** Data line for SD/MMC interface. (LPC2367/68 only) |
| | | | I/O | **I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. |
| P3[0] to P3[31] | | | I/O | **Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 3 pins depends upon the pin function selected via the pin connect block. Pins 0 through 24, and 27 through 31 of this port are not available. |
| P3[25]/MAT0[0]/ PWM1[2] | 27[1] | H3[1] | I/O | **P3[25] —** General purpose digital input/output pin. |
| | | | O | **MAT0[0] —** Match output for Timer 0, channel 0. |
| | | | O | **PWM1[2] —** Pulse Width Modulator 1, output 2. |
| P3[26]/MAT0[1]/ PWM1[3] | 26[1] | K1[1] | I/O | **P3[26] —** General purpose digital input/output pin. |
| | | | O | **MAT0[1] —** Match output for Timer 0, channel 1. |
| | | | O | **PWM1[3] —** Pulse Width Modulator 1, output 3. |
| P4[0] to P4[31] | | | I/O | **Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 4 pins depends upon the pin function selected via the pin connect block. Pins 0 through 27, 30, and 31 of this port are not available. |
| P4[28]/MAT2[0]/ TXD3 | 82[1] | C7[1] | I/O | **P4[28] —** General purpose digital input/output pin. |
| | | | O | **MAT2[0] —** Match output for Timer 2, channel 0. |
| | | | O | **TXD3 —** Transmitter output for UART3. |
| P4[29]/MAT2[1]/ RXD3 | 85[1] | E6[1] | I/O | **P4[29] —** General purpose digital input/output pin. |
| | | | O | **MAT2[1] —** Match output for Timer 2, channel 1. |
| | | | I | **RXD3 —** Receiver input for UART3. |
| DBGEN | - | D4[1][8] | I | **DBGEN —** JTAG interface control signal. Also used for boundary scanning.<br>**Note:** This pin is available in LPC2364FET100 and LPC2368FET100 devices only (TFBGA package). |
| TDO | 1[1][7] | A1[1][7] | O | **TDO —** Test Data out for JTAG interface. |
| TDI | 2[1][8] | C3[1][8] | I | **TDI —** Test Data in for JTAG interface. |
| TMS | 3[1][8] | B1[1][8] | I | **TMS —** Test Mode Select for JTAG interface. |
| TRST | 4[1][8] | C2[1][8] | I | **TRST —** Test Reset for JTAG interface. |
| TCK | 5[1][7] | C1[1][7] | I | **TCK —** Test Clock for JTAG interface. This clock must be slower than 1/6 of the CPU clock (CCLK) for the JTAG interface to operate |
| RTCK | 100[1][8] | B2[1][8] | I/O | **RTCK —** JTAG interface control signal.<br>**Note:** LOW on this pin while RESET is LOW enables ETM pins (P2[9:0]) to operate as trace port after reset. |

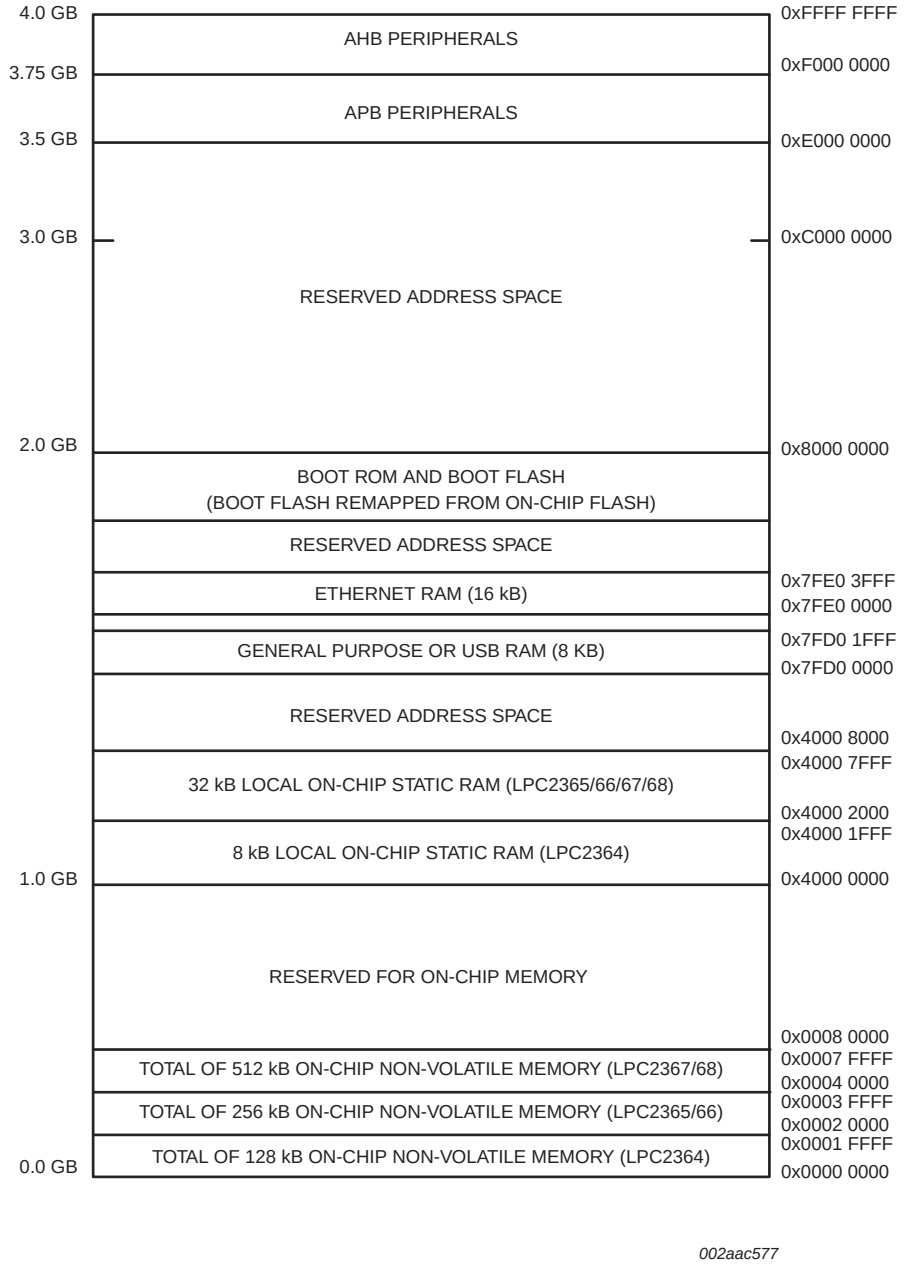



**Fig 4. LPC2364/65/66/67/68 memory map**

## 7.5 Interrupt controller

The ARM processor core has two interrupt inputs called Interrupt Request (IRQ) and Fast Interrupt Request (FIQ). The VIC takes 32 interrupt request inputs which can be programmed as FIQ or vectored IRQ types. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

- Single DMA and burst DMA request signals. Each peripheral connected to the GPDMA can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the GPDMA.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority. Each DMA channel has a specific hardware priority. DMA channel 0 has the highest priority and channel 1 has the lowest priority. If requests from two channels become active at the same time the channel with the highest priority is serviced first.
- AHB slave DMA programming interface. The GPDMA is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB master for transferring data. This interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data. Usually the burst size is set to half the size of the FIFO in the peripheral.
- Internal four-word FIFO per channel.
- Supports 8-bit, 16-bit, and 32-bit wide transactions.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Interrupt masking. The DMA error and DMA terminal count interrupt requests can be masked.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

## 7.8 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC2364/65/66/67/68 use accelerated GPIO functions:

- GPIO registers are relocated to the ARM local bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.

## 7.13 10-bit DAC

The DAC allows the LPC2364/65/66/67/68 to generate a variable analog output. The maximum output value of the DAC is $V_{i(VREF)}$.

### 7.13.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive

## 7.14 UARTs

The LPC2364/65/66/67/68 each contain four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

### 7.14.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- UART3 includes an IrDA mode to support infrared communication.

## 7.15 SPI serial I/O controller

The LPC2364/65/66/67/68 each contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

### 7.15.1 Features

- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

## 7.20 General purpose 32-bit timers/external event counters

The LPC2364/65/66/67/68 include four 32-bit Timer/Counters. The Timer/Counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The Timer/Counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

### 7.20.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit prescaler.
- Counter or Timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

## 7.21 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2364/65/66/67/68. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

On the wake-up of Sleep mode, if the IRC was used before entering Sleep mode, the code execution and peripherals activities will resume after 4 cycles expire. If the main external oscillator was used, the code execution will resume when 4096 cycles expire.

The customers need to reconfigure the PLL and clock dividers accordingly.

#### 7.24.4.3 Power-down mode

Power-down mode does everything that Sleep mode does, but also turns off the IRC oscillator and the flash memory. This saves more power, but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 4 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. The customers need to reconfigure the PLL and clock dividers accordingly.

#### 7.24.4.4 Deep power-down mode

Deep power-down mode is similar to the Power-down mode, but now the on-chip regulator that supplies power to the internal logic is also shut off. This produces the lowest possible power consumption without removing power from the entire chip. Since the Deep power-down mode shuts down the on-chip logic power supply, there is no register or memory retention, and resumption of operation involves the same activities as a full chip reset.

If power is supplied to the LPC2364/65/66/67/68 during Deep power-down mode, wake-up can be caused by the RTC Alarm interrupt or by external Reset.

While in Deep power-down mode, external device power may be removed. In this case, the LPC2364/65/66/67/68 will start up when external power is restored.

Essential data may be retained through Deep power-down mode (or through complete powering off of the chip) by storing data in the Battery RAM, as long as the external power to the VBAT pin is maintained.

#### 7.24.4.5 Power domains

The LPC2364/65/66/67/68 provides two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the battery RAM.

On the LPC2364/65/66/67/68, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(DCDC)(3V3)}$ pin powers the on-chip DC-to-DC converter which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC2364/65/66/67/68 application, a design can use two power options to manage power consumption.

### 7.25.3 Code security (Code Read Protection - CRP)

This feature of the LPC2364/65/66/67/68 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P2[10] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

**CAUTION**

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

### 7.25.4 AHB

The LPC2364/65/66/67/68 implement two AHBs in order to allow the Ethernet block to operate without interference caused by other system activity. The primary AHB, referred to as AHB1, includes the Vectored Interrupt Controller, GPDMA controller, USB interface, and 8 kB SRAM primarily intended for use by the USB. The USB interface is available on LPC2364/66/68 only.

The second AHB, referred to as AHB2, includes only the Ethernet block and an associated 16 kB SRAM. In addition, a bus bridge is provided that allows the secondary AHB to be a bus master on AHB1, allowing expansion of Ethernet buffer space into unused space in memory residing on AHB1.

In summary, bus masters with access to AHB1 are the ARM7 itself, the USB block, the GPDMA function, and the Ethernet block (via the bus bridge from AHB2). Bus masters with access to AHB2 are the ARM7 and the Ethernet block.

### 7.25.5 External interrupt inputs

The LPC2364/65/66/67/68 include up to 46 edge sensitive interrupt inputs combined with up to four level sensitive external interrupt inputs as selectable pin functions. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD(3V3)}$ | supply voltage (3.3 V) | core and external rail | | 3.0 | 3.6 | V |
| $V_{DD(DCDC)(3V3)}$ | DC-to-DC converter supply voltage (3.3 V) | | | 3.0 | 3.6 | V |
| $V_{DDA}$ | analog 3.3 V pad supply voltage | | | −0.5 | +4.6 | V |
| $V_{i(VBAT)}$ | input voltage on pin VBAT | for the RTC | | −0.5 | +4.6 | V |
| $V_{i(VREF)}$ | input voltage on pin VREF | | | −0.5 | +4.6 | V |
| $V_{IA}$ | analog input voltage | on ADC related pins | | −0.5 | +5.1 | V |
| $V_I$ | input voltage | 5 V tolerant I/O pins; only valid when the $V_{DD(3V3)}$ supply voltage is present | [2] | −0.5 | +6.0 | V |
| | | other I/O pins | [2][3] | −0.5 | $V_{DD(3V3)}$ + 0.5 | V |
| $I_{DD}$ | supply current | per supply pin | [4] | - | 100 | mA |
| $I_{SS}$ | ground current | per ground pin | [4] | - | 100 | mA |
| $T_{stg}$ | storage temperature | non-operating | [5] | −65 | +150 | °C |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | | - | 1.5 | W |
| $V_{ESD}$ | electrostatic discharge voltage | human body model; all pins | [6] | −2500 | +2500 | V |

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The peak current is limited to 25 times the corresponding maximum current.

[5] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

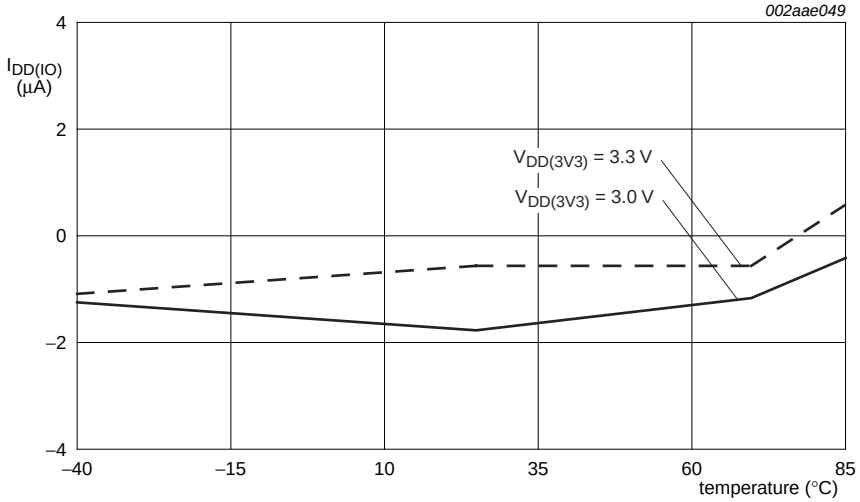
# 10. Static characteristics

**Table 8. Static characteristics**

*$T_{amb}$ = −40 °C to +85 °C for standard devices, −40 °C to +125 °C for LPC2364HBD only, unless otherwise specified.*

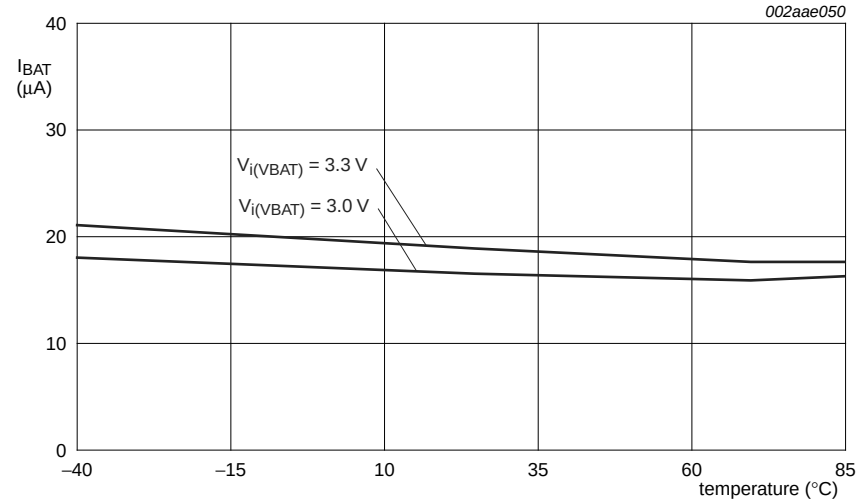
| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD(3V3)}$ | supply voltage (3.3 V) | core and external rail | | 3.0 | 3.3 | 3.6 | V |
| $V_{DD(DCDC)(3V3)}$ | DC-to-DC converter supply voltage (3.3 V) | | | 3.0 | 3.3 | 3.6 | V |
| $V_{DDA}$ | analog 3.3 V pad supply voltage | | | 3.0 | 3.3 | 3.6 | V |
| $V_{i(VBAT)}$ | input voltage on pin VBAT | | [2] | 2.0 | 3.3 | 3.6 | V |
| $V_{i(VREF)}$ | input voltage on pin VREF | | | 2.5 | 3.3 | $V_{DDA}$ | V |
| $I_{DD(DCDC)act(3V3)}$ | active mode DC-to-DC converter supply current (3.3 V) | $V_{DD(DCDC)(3V3)}$ = 3.3 V; $T_{amb}$ = 25 °C; code `while(1){}` executed from flash; no peripherals enabled; PCLK = CCLK | | | | | |
| | | CCLK = 10 MHz | | - | 15 | - | mA |
| | | CCLK = 72 MHz | | - | 63 | - | mA |
| | | all peripherals enabled; PCLK = CCLK / 8 | | | | | |
| | | CCLK = 10 MHz | | - | 21 | - | mA |
| | | CCLK = 72 MHz | | - | 92 | - | mA |
| | | all peripherals enabled; PCLK = CCLK | | | | | |
| | | CCLK = 10 MHz | | - | 27 | - | mA |
| | | CCLK = 72 MHz | | - | 125 | - | mA |
| $I_{DD(DCDC)pd(3V3)}$ | Power-down mode DC-to-DC converter supply current (3.3 V) | $V_{DD(DCDC)(3V3)}$ = 3.3 V; $T_{amb}$ = 25 °C | [3] | - | 113 | - | µA |
| $I_{DD(DCDC)dpd(3V3)}$ | Deep power-down mode DC-to-DC converter supply current (3.3 V) | | [3] | - | 20 | - | µA |
| $I_{BATact}$ | active mode battery supply current | | [4] | - | 20 | - | µA |
| $I_{BAT}$ | battery supply current | Deep power-down mode | [3] | - | 20 | - | µA |
| **Standard port pins, $\overline{\text{RESET}}$, RTCK** | | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; no pull-up | | - | - | 3 | µA |
| $I_{IH}$ | HIGH-level input current | $V_I = V_{DD(3V3)}$; no pull-down | | - | - | 3 | µA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O = V_{DD(3V3)}$; no pull-up/down | | - | - | 3 | µA |

## 10.1 Power-down mode



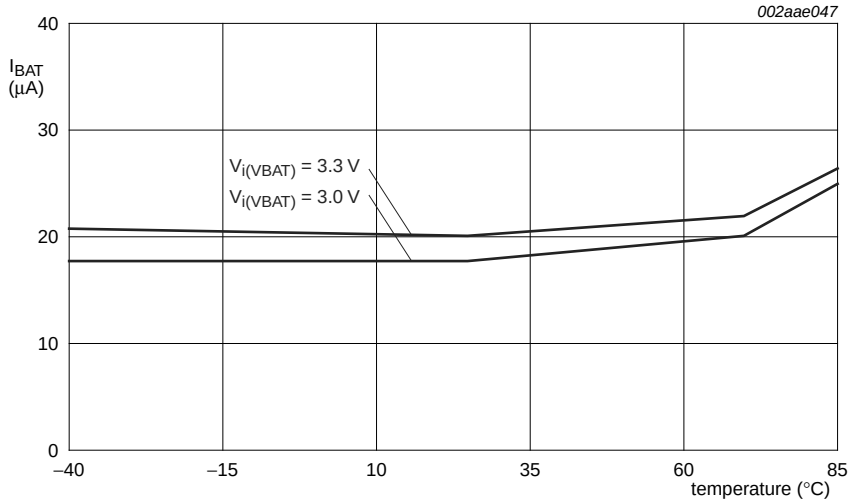

$V_{i(VBAT)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

**Fig 5. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Power-down mode**



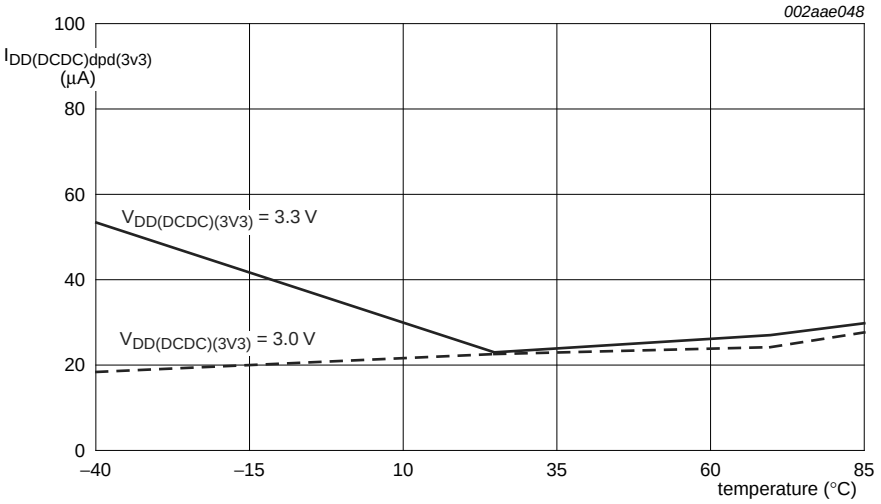

$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

**Fig 6. RTC battery maximum supply current $I_{BAT}$versus temperature in Power-down mode**



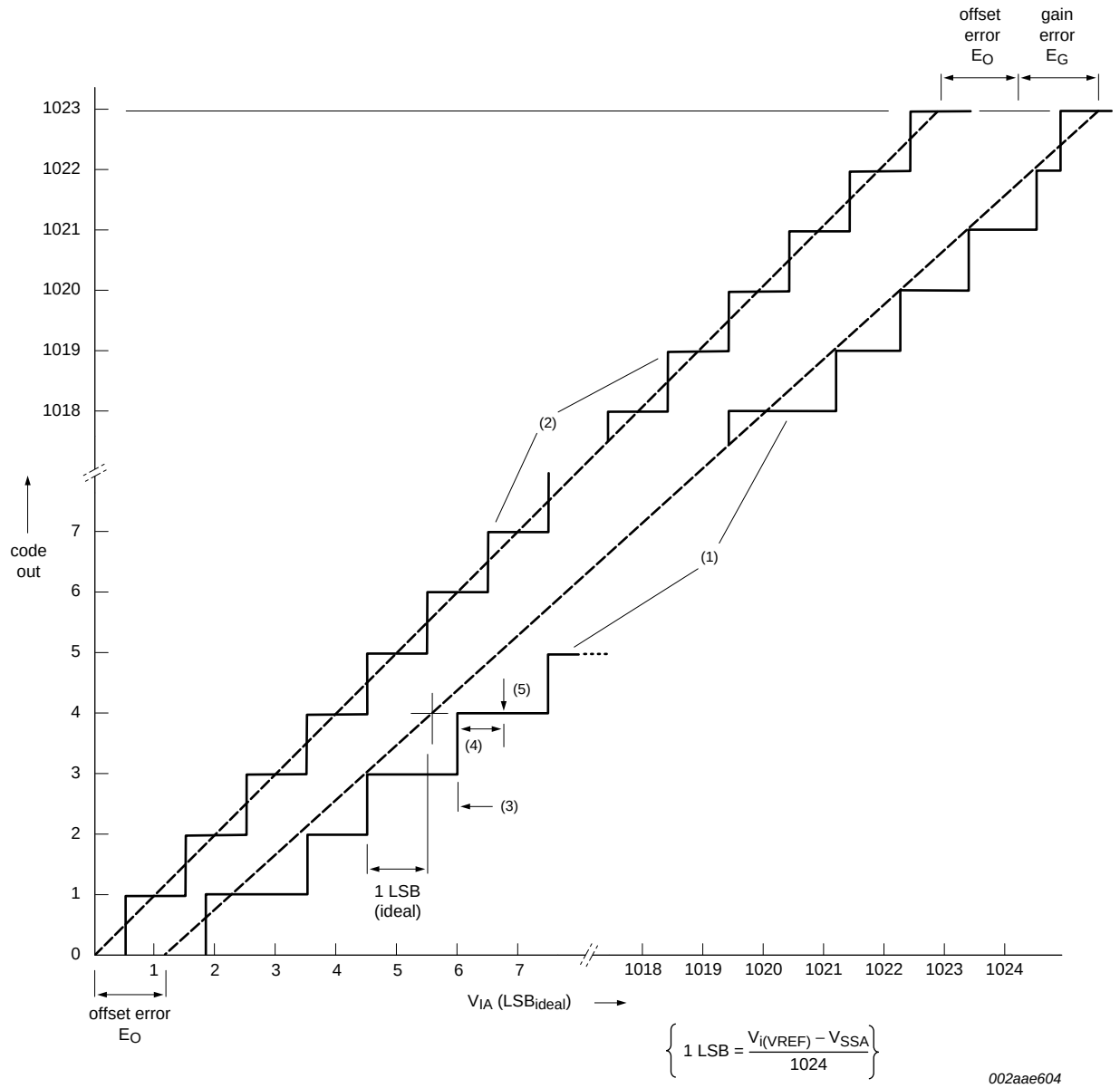

$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C

**Fig 9. RTC battery maximum supply current $I_{BAT}$ versus temperature in Deep power-down mode**




$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

**Fig 10. Total DC-to-DC converter maximum supply current $I_{DD(DCDC)dpd(3V3)}$ versus temperature in Deep power-down mode**




(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error ($E_D$).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

**Fig 16. ADC characteristics**

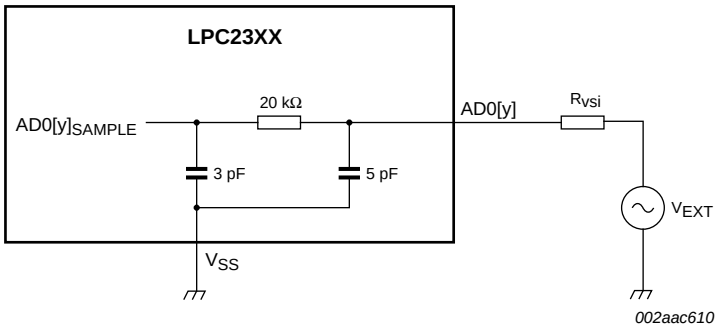



**Fig 17. Suggested ADC interface - LPC2364/65/66/67/68 AD0[y] pin**

# 13. DAC electrical characteristics

**Table 15. DAC electrical characteristics**

*$V_{DDA}$ = 3.0 V to 3.6 V; $T_{amb}$ = −40 °C to +85 °C unless otherwise specified*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $E_D$ | differential linearity error | | - | ±1 | - | LSB |
| $E_{L(adj)}$ | integral non-linearity | | - | ±1.5 | - | LSB |
| $E_O$ | offset error | | - | 0.6 | - | % |
| $E_G$ | gain error | | - | 0.6 | - | % |
| $C_L$ | load capacitance | | - | 200 | - | pF |
| $R_L$ | load resistance | | 1 | - | - | kΩ |

# 14. Application information

## 14.1 Suggested USB interface solutions (LPC2364/66/68 only)

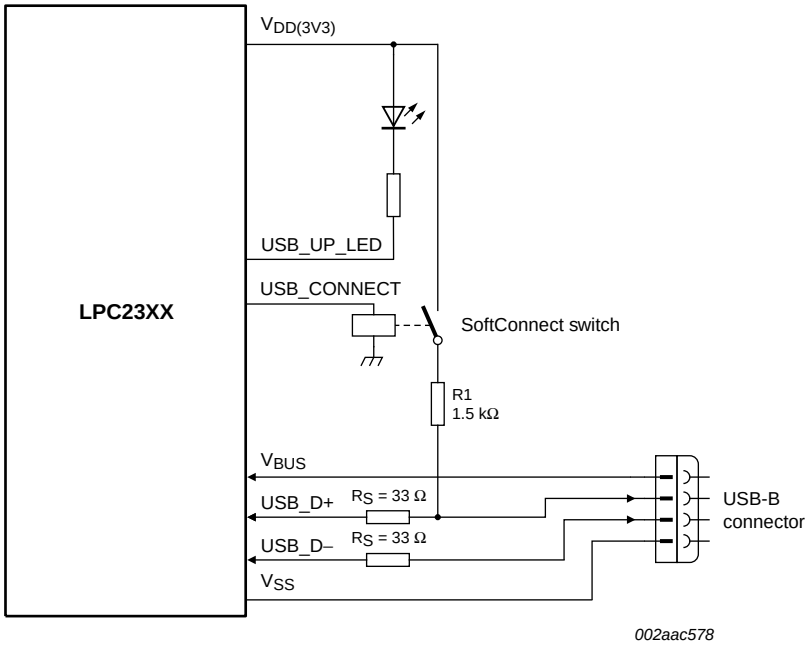



**Fig 18. LPC2364/66/68 USB interface on a self-powered device**

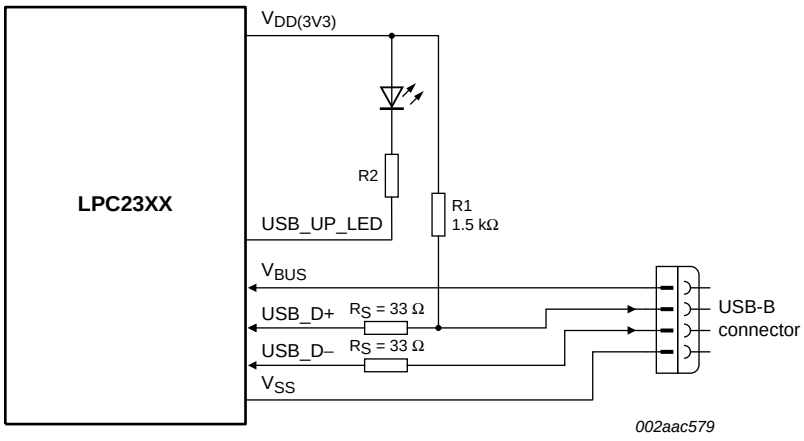



**Fig 19. LPC2364/66/68 USB interface on a bus-powered device**

## 14.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i$ = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground $C_g$ which attenuates the input voltage by a factor $C_i$ / ($C_i$ + $C_g$). In slave mode, a minimum of 200 mV (RMS) is needed.

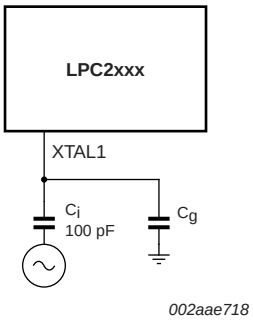



**Fig 20. Slave mode operation of the on-chip oscillator**

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 20), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTAL2 pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 21 and in Table 16 and Table 17. Since the feedback resistance is integrated on chip, only a crystal and the capacitances $C_{X1}$ and $C_{X2}$ need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, $C_L$ and $R_S$). Capacitance $C_P$ in Figure 21 represents the parallel package capacitance and should not be larger than 7 pF. Parameters $F_{OSC}$, $C_L$, $R_S$ and $C_P$ are supplied by the crystal manufacturer.

## 14.6 Reset pin configuration

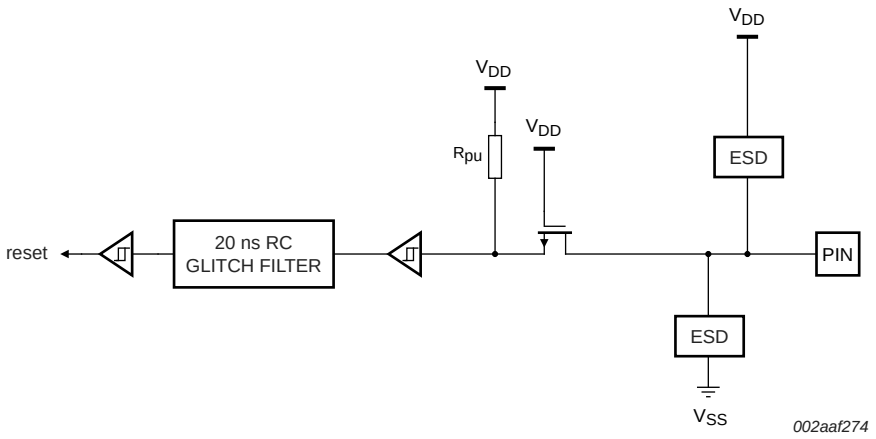
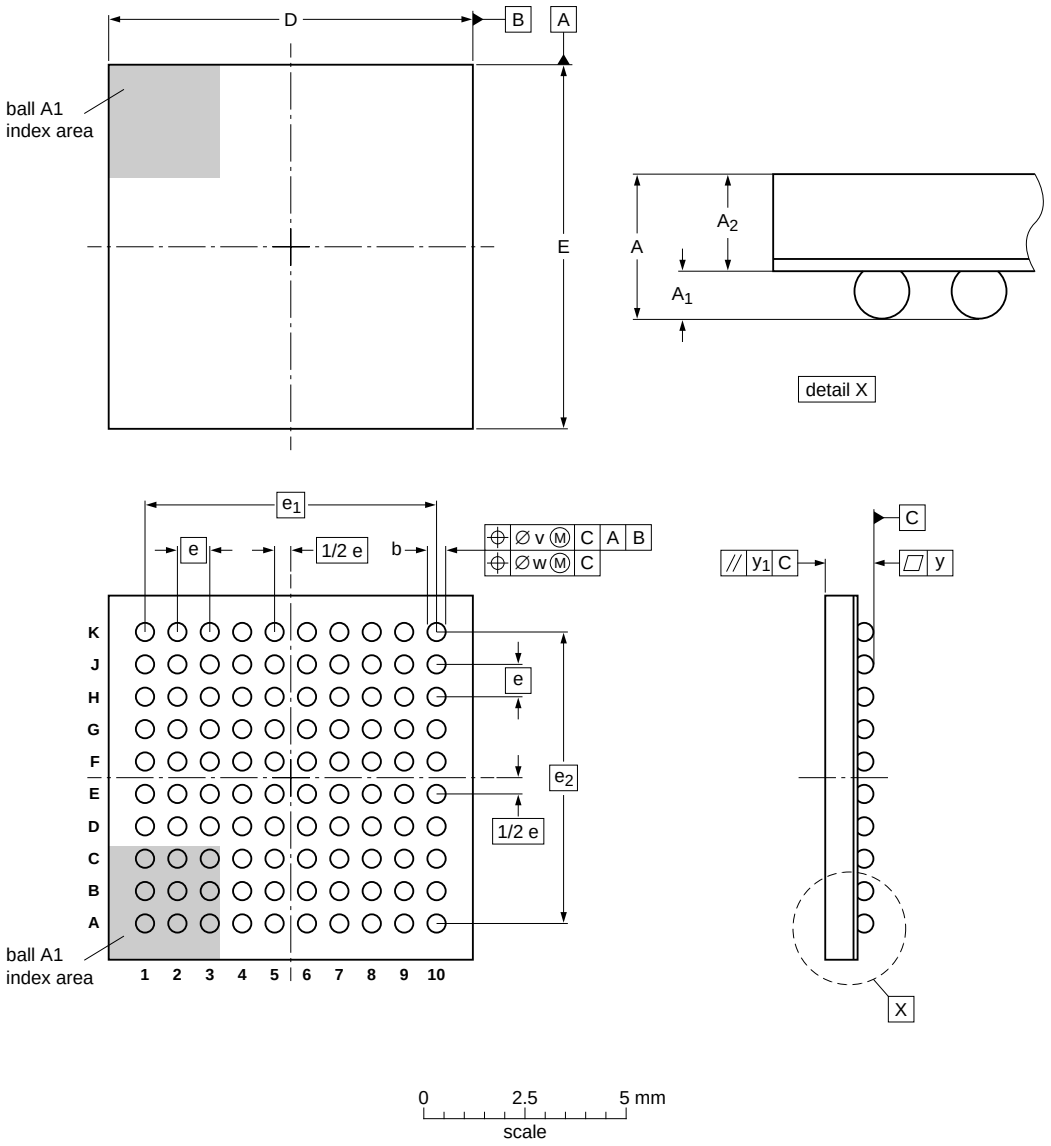



**Fig 24. Reset pin configuration**

**TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm** **SOT926-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.4<br>0.3 | 0.8<br>0.65 | 0.5<br>0.4 | 9.1<br>8.9 | 9.1<br>8.9 | 0.8 | 7.2 | 7.2 | 0.15 | 0.05 | 0.08 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT926-1 | - - - | - - - | - - - | | | ~~05-12-09~~<br>05-12-22 |

**Fig 26. Package outline SOT926-1 (TFBGA100)**

# 16. Abbreviations

**Table 19. Abbreviations**

| Acronym | Description |
|---|---|
| ADC | Analog-to-Digital Converter |
| AHB | Advanced High-performance Bus |
| AMBA | Advanced Microcontroller Bus Architecture |
| APB | Advanced Peripheral Bus |
| BOD | BrownOut Detection |
| CAN | Controller Area Network |
| DAC | Digital-to-Analog Converter |
| DCC | Debug Communication Channel |
| DMA | Direct Memory Access |
| DSP | Digital Signal Processing |
| EOP | End Of Packet |
| ETM | Embedded Trace Macrocell |
| GPIO | General Purpose Input/Output |
| IrDA | Infrared Data Association |
| JTAG | Joint Test Action Group |
| MII | Media Independent Interface |
| MIIM | Media Independent Interface Management |
| PHY | Physical Layer |
| PLL | Phase-Locked Loop |
| PWM | Pulse Width Modulator |
| RMII | Reduced Media Independent Interface |
| SE0 | Single Ended Zero |
| SPI | Serial Peripheral Interface |
| SSI | Serial Synchronous Interface |
| SSP | Synchronous Serial Port |
| TTL | Transistor-Transistor Logic |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 18.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 18.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.