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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u5dvm10ad

— 32 KByte L1 Instruction Cache

— 32 KByte L1 Data Cache

— Private Timer and Watchdog

— Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support

- Global Timer

- Snoop Control Unit (SCU)

- 512 KB unified I/D L2 cache:

  — Used by one core in i.MX 6Solo

  — Shared by two cores in i.MX 6DualLite

- Two Master AXI bus interfaces output of L2 cache

- Frequency of the core (including NEON and L1 cache), as per Table 8.

- NEON MPE coprocessor

  — SIMD Media Processing Architecture

  — NEON register file with 32x64-bit general-purpose registers

  — NEON Integer execute pipeline (ALU, Shift, MAC)

  — NEON dual, single-precision floating point execute pipeline (FADD, FMUL)

  — NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

— Boot ROM, including HAB (96 KB)

— Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)

— Secure/non-secure RAM (16 KB)

- External memory interfaces: The i.MX 6Solo/6DualLite processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.

  — 16/32-bit LP-DDR2-800, 16/32-bit DDR3-800 and DDR3L-800 in i.MX 6Solo; 16/32/64-bit LP-DDR2-800, 16/32/64-bit DDR3-800 and DDR3L-800, supporting DDR interleaving mode for 2x32 LPDDR2-800 in i.MX 6DualLite

  — 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.

  — 16/32-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.

  — 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Solo/6DualLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total of five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to two interfaces may be active in parallel (excluding EPDC).

  — One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)

- — Four Pulse Width Modulators (PWM)
- — System JTAG Controller (SJC)
- — GPIO with interrupt capabilities
- — 8x8 Key Pad Port (KPP)
- — Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
- — Two Controller Area Network (FlexCAN), 1 Mbps each
- — Two Watchdog timers (WDOG)
- — Audio MUX (AUDMUX)
- — MLB (MediaLB) provides interface to MOST Networks (MOST25, MOST50, MOST150) with the option of DTCP cipher accelerator

The i.MX 6Solo/6DualLite processors integrate advanced power management unit and controllers:

- • Provide PMU, including LDO supplies, for on-chip resources
- • Use Temperature Sensor for monitoring the die temperature
- • Support DVFS techniques for low power modes
- • Use SW State Retention and Power Gating for ARM and MPE
- • Support various levels of system power modes
- • Use flexible clock gating control scheme

The i.MX 6Solo/6DualLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Solo/6DualLite processors incorporate the following hardware accelerators:

- • VPU—Video Processing Unit
- • IPUv3H—Image Processing Unit version 3H
- • GPU3Dv5—3D Graphics Processing Unit (OpenGL ES 2.0) version 5
- • GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- • PXP—PiXel Processing Pipeline. Off loading key pixel processing operations are required to support the EPD display applications.
- • ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- • ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- • SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- • CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 16 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- • SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- • CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E-INK^{TM} EPD panels, supporting a wide variety of TFT backplanes. It is available in both i.MX 6DualLite and i.MX 6Solo.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit "set and forget" timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Solo/6DualLite processors consist of 512x8-bit fuse fox accessible through OCOTP_CTRL interface.

The choice of a clock source must be based on real-time clock use and precision timeout.

4.1.5   Maximum Supply Currents

The Power Virus numbers shown in Table 10 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 10, however a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Solo/6DualLite Power Consumption Measurement Application Note (AN4576) for more details on typical power consumption under various use case definitions.

Table 10. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	i.MX 6DualLite: 996 MHz ARM clock based on Power Virus operation	2200	mA
	i.MX 6Solo: 996 MHz ARM clock based on Power Virus operation	1320	mA
VDD_SOC_IN	996 MHz ARM clock	1260	mA
VDD_HIGH_IN	—	125[1]	mA
VDD_SNVS_IN	—	275[2]	µA
USB_OTG_VBUS/ USB_H1_VBUS (LDO 3P0)	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	—[4]	—
NVCC_ENET	N=10	Use maximum IO equation[5]	—
NVCC_LCD	N=29	Use maximum IO equation[5]	—
NVCC_GPIO	N=24	Use maximum IO equation[5]	—
NVCC_CSI	N=20	Use maximum IO equation[5]	—
NVCC_EIM	N=53	Use maximum IO equation[5]	—
NVCC_JTAG	N=6	Use maximum IO equation[5]	—
NVCC_RGMII	N=6	Use maximum IO equation[5]	—
NVCC_SD1	N=6	Use maximum IO equation[5]	—
NVCC_SD2	N=6	Use maximum IO equation[5]	—
NVCC_SD3	N=11	Use maximum IO equation[5]	—
NVCC_NANDF	N=26	Use maximum IO equation[5]	—

Table 10. Maximum Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_LVDS2P5[6]	—	NVCC_LVDS2P5 is connected to VDD_HIGH_CAP at the board level. VDD_HIGH_CAP is capable of handing the current required by NVCC_LVDS2P5.	—
MISC			
DDR_VREF	—	1	mA

[1] The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI and PCIe VPH supplies).

[2] Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown in Table 10. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

[3] This is the maximum current per active USB physical interface.

[4] The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6Solo/DualLite Power Consumption Measurement Application Note (AN4576) for examples of DRAM power consumption during specific use case scenarios.

[5] General equation for estimated, maximum power consumption of an IO power supply:

$Imax = N \times C \times V \times (0.5 \times F)$

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

[6] NVCC_LVDS2P5 is supplied by VDD_HIGH_CAP (by external connection) so the maximum supply current is included in the current shown for VDD_HIGH_IN. The maximum supply current for NVCC_LVDS2P5 has not been characterized separately.

4.1.6 Low Power Mode Supply Currents

Table 11 shows the current core consumption (not including I/O) of i.MX 6Solo/6DualLite processors in selected low power modes.

Table 11. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Units
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 • HIGH LDO set to 2.5 V • Clocks are gated. • DDR is in self refresh. • PLLs are active in bypass (24MHz) • Supply Voltages remain ON	VDD_ARM_IN (1.4V)	4.5	mA
		VDD_SOC_IN (1.4V)	23	
		VDD_HIGH_IN (3.0V)	13.5	
		Total	79	mW

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4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 8 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the USB Phy, LVDS Phy, HDMI Phy, MIPI Phy, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB_VBUS supply, when both are present. If only one of the USB_VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Solo/6DualLite reference manual.

Table 26. RGMII I/O 1.8V and 2.5V mode DC Electrical Characteristics[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
Pull-down Resistor (100 kΩ PD)	R_{PD_100K}	Vin=0V	—	1	µA
Keeper Circuit Resistance	R_{keep}		105	165	kΩ
Input Current (no pull-up/down)	I_{in}	VI = 0, VI = OVDD	-2.9	2.9	µA

[1] Input Mode Selection "SW_PAD_CTL_GRP_DDR_TYPE_RGMII"='10' (1.8V Mode)
"SW_PAD_CTL_GRP_DDR_TYPE_RGMII"='11' (2.5V Mode).

[2] Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

[3] To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{IL} or V_{IH}. Monotonic input transition time is from 0.1 ns to 1 s.

[4] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled (register IOMUXC_SW_PAD_CTL_PAD_RGMII_TXC[HYS]= 0).

4.6.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*" for details.

Table 27 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 27. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS	—	1.125	1.2	1.375	V

4.6.6 MLB I/O DC Parameters

The MLB interface complies with Analog Interface of 6-pin differential Media Local Bus specification version 4.1. See 6-pin differential MLB specification v4.1, "MediaLB 6-pin interface Electrical Characteristics" for details.

NOTE

The MLB 6-pin interface does not support speed mode 8192 fs.

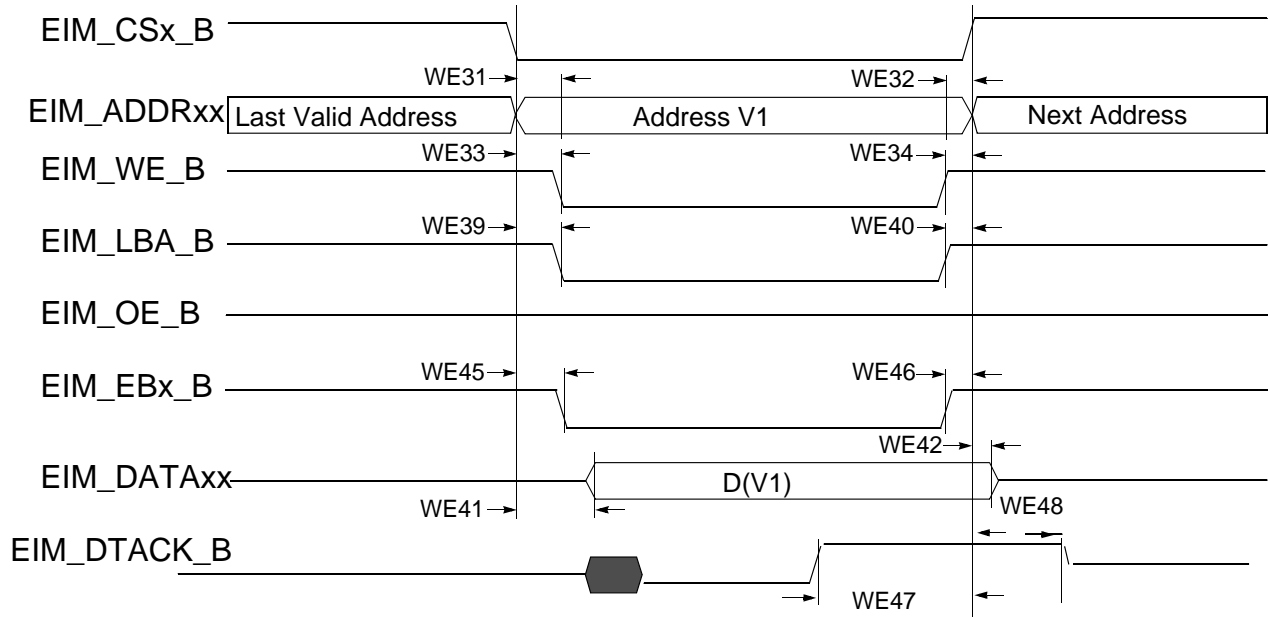Table 28 shows the Media Local Bus (MLB) I/O DC parameters.

Figure 24. DTACK Mode Write Access (DAP=0)

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip to Select

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4 - WE6 - CSA[2]	—	3 - CSA	ns
WE32	Address Invalid to EIM_CSx_B invalid	WE7 - WE5 - CSN[3]	—	3 - CSN	ns
WE32A (muxed A/D)	EIM_CSx_B valid to Address Invalid	t[4] + WE4 - WE7 + (ADVN[5] + ADVA[6] + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN_WCSN)	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-RCSA)	3 + (OEA + RADVN+RADVA+ADH +1-RCSA)	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns

Table 51. Enhanced Serial Audio Interface (ESAI) Timing Parameters (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	$2 \times T_C$	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

[1] i ck = internal clock
  x ck = external clock
  i ck a = internal clock, asynchronous mode
  (asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
  i ck s = internal clock, synchronous mode
  (synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

[2] bl = bit length
  wl = word length
  wr = word length relative

[3] ESAI_TX_CLK(SCKT pin) = transmit clock
  ESAI_RX_CLK(SCKR pin) = receive clock
  ESAI_TX_FS(FST pin) = transmit frame sync
  ESAI_RX_FS(FSR pin) = receive frame sync
  ESAI_TX_HF_CLK(HCKT pin) = transmit high frequency clock
  ESAI_RX_HF_CLK(HCKR pin) = receive high frequency clock

[4] For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

[5] The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

[6] Periodically sampled and not 100% tested.

Table 61. Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		TMDS drivers DC specifications				
V_{OFF}	Single-ended standby voltage	RT = 50 Ω For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	avddtmds ± 10 mV			mV
V_{SWING}	Single-ended output swing voltage		400	—	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds ± 10 mV			mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 200 mV	—	avddtmds + 10 mV	mV
V_L	Single-ended output low voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds - 600 mV	—	avddtmds - 400mV	mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 700 mV	—	avddtmds - 400 mV	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see Figure 53). **Note:** R_{TERM} can also be configured to be open and not present on TMDS channels.	—	50	—	200	Ω
		Hot plug detect specifications				
HPD^{VH}	Hot plug detect high range	—	2.0	—	5.3	V
$VHPD_{VL}$	Hot plug detect low range	—	0	—	0.8	V
HPD_Z	Hot plug detect input impedance	—	10	—	—	kΩ
HPD_t	Hot plug detect time delay	—	—	—	100	µs

4.11.8 Switching Characteristics

Table 62 describes switching characteristics for the HDMI 3D Tx PHY. Figure 54 to Figure 58 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

Figure 66 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set through the Register. Table 68 lists the synchronous display interface timing characteristics.
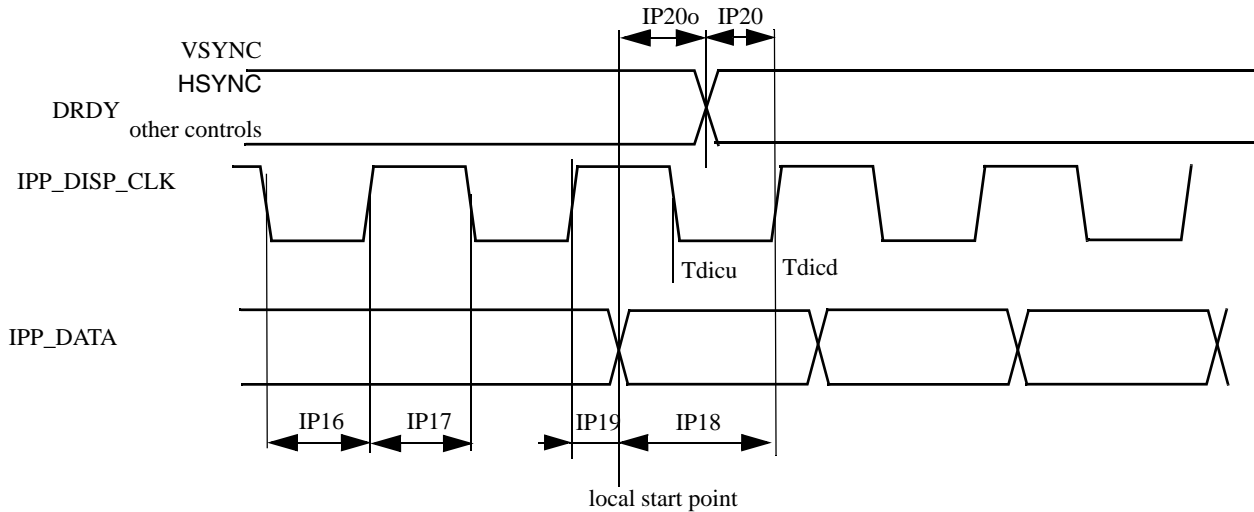

Figure 66. Synchronous Display Interface Timing Diagram—Access Level

Table 68. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

[1] The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$\text{Tdicd} = \frac{1}{2}\left(T_{diclk} \times \text{ceil}\left[\frac{2 \times \text{DISP\_CLK\_DOWN}}{\text{DI\_CLK\_PERIOD}}\right]\right)$$

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$\text{Tdicu} = \frac{1}{2}\left(T_{diclk} \times \text{ceil}\left[\frac{2 \times \text{DISP\_CLK\_UP}}{\text{DI\_CLK\_PERIOD}}\right]\right)$$

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*".

Table 69. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	V
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	V
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	-50	50	mV
Output short circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and IO Supply Voltage	247	454	mV

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x2 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Electrical and Timing Information

Table 70. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Input DC Specifications - Apply to DSI_CLK_P/DSI_CLK_N and DSI_DATA_P/DSI_DATA_N inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV
V_{LEAK}	Input leakage current	VGNDSH(min) = VI = VGNDSH(max) + VOH(absmax) Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level	—	—	—	1.45	V

Table 70. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
$t_{voh(absmax)}$	Maximum transient time above VOH(absmax)	—	—	—	20	ns
HS Line Drivers DC Specifications						
$|V_{OD}|$	HS Transmit Differential output voltage magnitude	80 Ω<= RL< = 125 Ω	140	200	270	mV
$\Delta|V_{OD}|$	Change in Differential output voltage magnitude between logic states	80 Ω<= RL< = 125 Ω	—	—	10	mV
V_{CMTX}	Steady-state common-mode output voltage.	80 Ω<= RL< = 125 Ω	150	200	250	mV
$\Delta V_{CMTX}(1,0)$	Changes in steady-state common-mode output voltage between logic states	80 Ω<= RL< = 125 Ω	—	—	5	mV
V_{OHHS}	HS output high voltage	80 Ω<= RL< = 125 Ω	—	—	360	mV
Z_{OS}	Single-ended output impedance.	—	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch.	—	—	—	10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage	—	-50		50	mV
V_{OH}	Output high-level SE voltage	—	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.	—	110	—	—	Ω
$\Delta Z_{OLP(01-10)}$	Single-ended output impedance mismatch driving opposite level	—	—	—	20	%
$\Delta Z_{OLP(0-11)}$	Single-ended output impedance mismatch driving same level	—	—	—	5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold	—	—	—	70	mV
V_{IDTL}	Differential input low voltage threshold	—	-70	—	—	mV
V_{IHHS}	Single ended input high voltage	—	—	—	460	mV
V_{ILHS}	Single ended input low voltage	—	-40	—	—	mV
V_{CMRXDC}	Input common mode voltage	—	70	—	330	mV

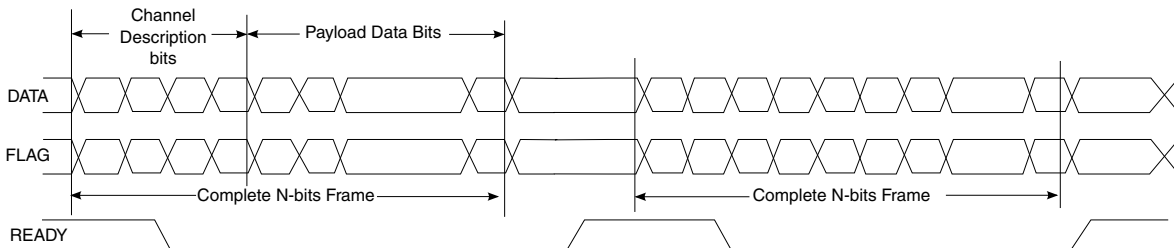## 4.11.13.5 Stream Transmission Mode Frame Transfer

Figure 78. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)
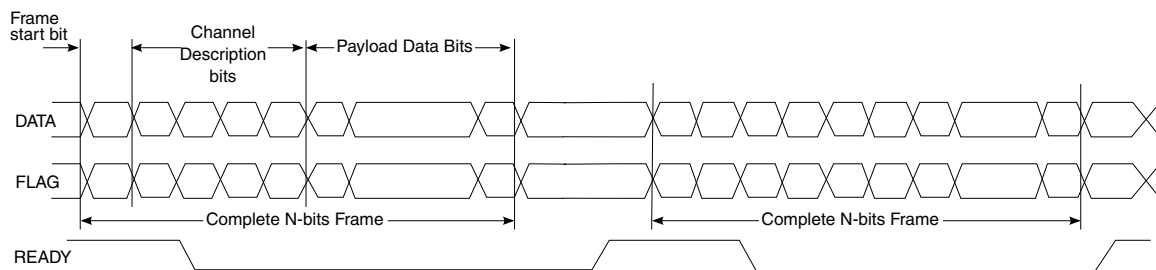

Figure 79. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)
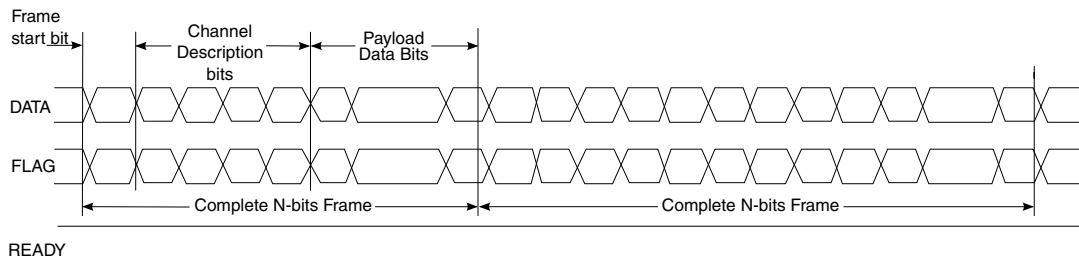

Figure 80. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 72. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10.0 ns	5.00 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2.00 ns	2.00 ns	1.00 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50.0 ns	0.5.0 ns	0.25 ns

4.11.15.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.16 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

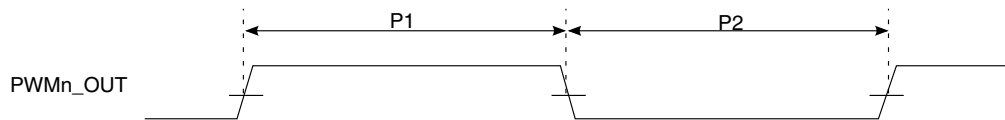Figure 84 depicts the timing of the PWM, and Table 78 lists the PWM timing parameters.

Figure 84. PWM Timing

Table 78. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.11.17 SCAN JTAG Controller (SJC) Timing Parameters

Figure 85 depicts the SJC test clock input timing. Figure 86 depicts the SJC boundary scan timing. Figure 87 depicts the SJC test access port. Signal parameters are listed in Table 79.
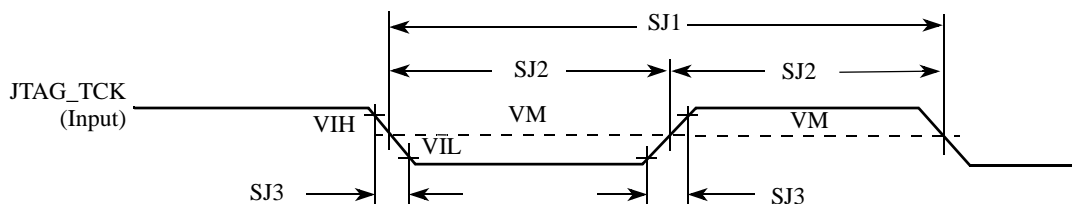

Figure 85. Test Clock Input Timing Diagram

Table 83. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.

- All timings are on Audiomux Pads when SSI is being used for data transfer.

- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).

- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.20 UART I/O Configuration and Timing Parameters

4.11.20.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Solo/6DualLite UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 86 shows the UART I/O configuration based on the enabled mode.

Table 86. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UARTx_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UARTx_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UARTx_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UARTx_DCD_ B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UARTx_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.11.20.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.11.20.2.1 UART Transmitter

Figure 95 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 87 lists the UART RS-232 serial mode transmit timing characteristics.
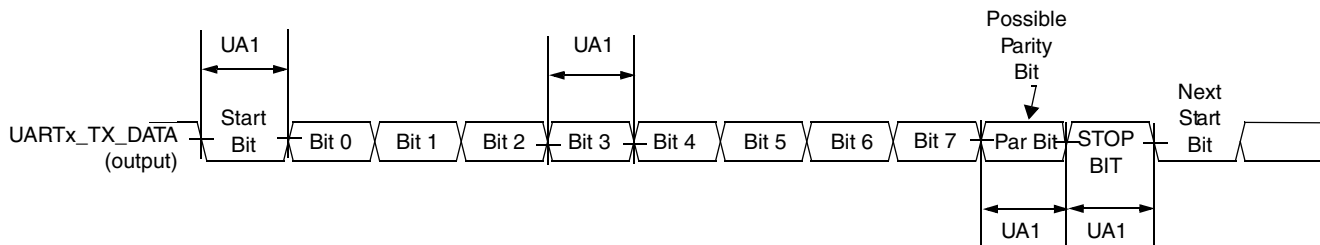

Figure 95. UART RS-232 Serial Mode Transmit Timing Diagram

Table 87. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

Table 93. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_DA14	Input	BOOT_CFG2[6]
EIM_DA15	Input	BOOT_CFG2[7]
EIM_A16	Input	BOOT_CFG3[0]
EIM_A17	Input	BOOT_CFG3[1]
EIM_A18	Input	BOOT_CFG3[2]
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

1 Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2   Boot Device Interface Allocation

Table 94 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 94. Interface Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	—

Figure 101. 21 x 21 mm BGA, Case 2240 Package Top, Bottom, and Side Views

Table 95 shows the 21 × 21 mm BGA package details.

Table 95. 21 x 21, 0.8 mm BGA Package Details

Parameter	Symbol	Common Dimensions		
		Minimum	**Normal**	**Maximum**
Total Thickness	A	—	—	1.6
Stand Off	A1	0.36	—	0.46
Substrate Thickness	A2	0.26 REF		
Mold Thickness	A3	0.7 REF		
Body Size	D	21 BSC		
	E	21 BSC		
Ball Diameter	—	0.5		
Ball Opening	—	0.4		
Ball Width	b	0.44	—	0.64
Ball Pitch	e	0.8 BSC		
Ball Count	n	624		
Edge Ball Center to Center	D1	19.2 BSC		
	E1	19.2 BSC		
Body Center to Contact Ball	SD	—		
	SE	—		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.2		
Coplanarity	ddd	0.15		
Ball Offset (Package)	eee	0.15		
Ball Offset (Ball)	fff	0.08		