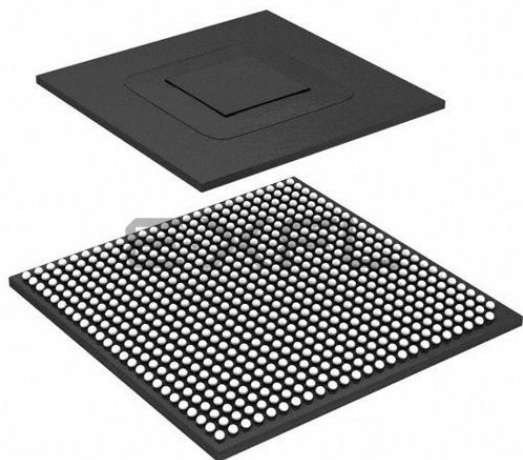




Welcome to [E-XFL.COM](#)

Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM® Cortex® -A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u5evm10ad

- Color eReaders
- IPTV
- Human Machine Interfaces (HMI)
- Portable medical
- IP phones
- Home energy management systems

The i.MX 6Solo/6DualLite applications processors feature:

- Applications processors—The processors enhance the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS requirements of operating systems and games. The Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, DDR3L, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, an image processing unit (IPU), a programmable smart DMA (SDMA) controller, and an asynchronous sample rate converter.
- Powerful graphics acceleration—Each processor provides two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with a shader and a 2D graphics accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to two displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller two CAN ports, ESAI audio interface, and a variety of other popular interfaces (such as UART, I²C, and I²S serial audio, and PCIe-II).
- Eink Panel Display Controller—The processors integrate EPD controller that supports E-INK color and monochrome with up to 1650x2332 resolution and 5-bit grayscale (32-levels per color channel).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure

Table 1. Example Orderable Part Numbers (continued)

Part Number	i.MX6 CPU Solo/ DualLite	Options	Speed Grade ¹	Temperature Grade	Package
MCIMX6S8DVM10AB	Solo	With VPU, GPU, MLB, EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S8DVM10AC	Solo	With VPU, GPU, MLB, EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S8DVM10AD	Solo	With VPU, GPU, MLB, EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5DVM10AB	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5DVM10AC	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5DVM10AD	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
SCIMX6S5DVM10CB	Solo	HDCP enabled with VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
SCIMX6S5DVM10CC	Solo	HDCP enabled with VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
SCIMX6S5DVM10CD	Solo	HDCP enabled with VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5EVM10AB	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Extended Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5EVM10AC	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Extended Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S5EVM10AD	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Extended Commercial	21 mm x 21 mm, 0.8 mm pitch, MAPBGA

¹ If a 24 MHz input clock is used (required for USB), then the maximum SoC speed is limited to 996 MHz.

Figure 1 describes the part number nomenclature to identify the characteristics of a specific part number (for example, cores, frequency, temperature grade, fuse options, and silicon revision).

The primary characteristic that differentiates which data sheet applies to a specific part is the temperature grade (junction) field. The following list describes the correct data sheet to use for a specific part:

- The *i.MX 6Solo/6DualLite Automotive and Infotainment Applications Processors* data sheet (IMX6SDLAEC) covers parts listed with an “A (Automotive temp)”
- The *i.MX 6Solo/6DualLite Applications Processors for Consumer Products* data sheet (IMX6SDLCEC) covers parts listed with a “D (Commercial temp)” or “E (Extended Commercial temp)”

- LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
- HDMI 1.4 port
- MIPI/DSI, two lanes at 1 Gbps
- EPDC, Color, and monochrome E-INK, up to 1650x2332 resolution and 5-bit grayscale
- Camera sensors:
 - Two parallel Camera ports (up to 20 bit and up to 240 MHz peak)
 - MIPI CSI-2 Serial port, supporting from 80 Mbps to 1 Gbps speed per data lane. The CSI-2 Receiver core can manage one clock lane and up to two data lanes. Each i.MX 6Solo/6DualLite processor has two lanes.
- Expansion cards:
 - Four MMC/SD/SDIO card ports all supporting:
 - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
 - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
 - One high speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
 - Three USB 2.0 (480 Mbps) hosts:
 - One HS host with integrated High Speed Phy
 - Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Expansion PCI Express port (PCIe) v2.0 one lane
 - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
 - SSI block is capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I²S mode
 - ESAI is capable of supporting audio sample frequencies up to 260 kHz in I²S mode with 7.1 multi channel outputs
 - Five UARTs, up to 5.0 Mbps each:
 - Providing RS232 interface
 - Supporting 9-bit RS485 multidrop mode
 - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
 - Four eCSPI (Enhanced CSPI)
 - Four I²C, supporting 400 kbps
 - Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000¹ Mbps

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Solo/6DualLite errata document (IMX6SDLCE).

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IPUv3H	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST[®] data network, using the standardized MediaLB protocol (up to 6144 fs). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6Solo • Supports 16/32/64-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6DualLite • Supports 2x32 LPDDR2-800 in i.MX 6DualLite • Supports up to 4 GByte DDR memory space

Table 25. DDR3/DDR3L I/O DC Electrical Characteristics¹ (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	105	165	k Ω
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.9	2.9	μ A

¹ Note that the JEDEC DDR3 specification (JESD79_3D) supersedes any specification in this document.

² OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

³ Vref – DDR3/DDR3L external reference voltage.

⁴ The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.4 RGMII I/O 2.5V I/O DC Electrical Parameters

The RGMII interface complies with the RGMII standard version 1.3. The parameters in [Table 26](#) are guaranteed per the operating ranges in [Table 8](#), unless otherwise noted.

Table 26. RGMII I/O 1.8V and 2.5V mode DC Electrical Characteristics¹

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level Output Voltage ¹	VOH	Ioh= -0.1mA (DSE=001,010) Ioh= -1mA (DSE=011,100,101,110,111)	OVDD-0.15	—	V
Low-level Output Voltage ¹	VOL	Iol= 0.1mA (DSE=001,010) Iol= 1mA (DSE=011,100,101,110,111)	—	0.15	V
Input Reference Voltage	Vref	—	0.49 $\times$ OVDD	0.51 $\times$ OVDD	V
High-Level Input Voltage ^{2 3}	VIH	—	0.7 $\times$ OVDD	OVDD	V
Low-Level Input Voltage ^{2 3}	VIL	—	0	0.3 $\times$ OVDD	V
Input Hysteresis (OVDD=1.8V)	VHYS_HighVDD	OVDD=1.8V	250	—	mV
Input Hysteresis (OVDD=2.5V)	VHYS_HighVDD	OVDD=2.5V	250	—	mV
Schmitt Trigger VT+ ^{3 4}	VTH ⁺	—	0.5 $\times$ OVDD	—	mV
Schmitt Trigger VT- ^{3 4}	VTH ⁻	—	—	0.5 $\times$ OVDD	mV
Pull-up Resistor (22 k Ω PU)	RPU_22K	Vin=0V	—	212	μ A
Pull-up Resistor (22 k Ω PU)	RPU_22K	Vin=OVDD	—	1	μ A
Pull-up Resistor (47 k Ω PU)	RPU_47K	Vin=0V	—	100	μ A
Pull-up Resistor (47 k Ω PU)	RPU_47K	Vin=OVDD	—	1	μ A
Pull-up Resistor (100 k Ω PU)	RPU_100K	Vin=0V	—	48	μ A
Pull-up Resistor (100 k Ω PU)	RPU_100K	Vin=OVDD	—	1	μ A
Pull-down Resistor (100 k Ω PD)	RPD_100K	Vin=OVDD	—	48	μ A

A 4-stage pipeline is utilized in the MLB 6-pin implementation in order to facilitate design, maximize throughput, and allow for reasonable PCB trace lengths. Each cycle is one `ipp_clk_in*` (internal clock from MLB PLL) clock period. Cycles 2, 3, and 4 are MLB PHY related. Cycle 2 includes clock-to-output delay of Signal/Data sampling flip-flop and Transmitter, Cycle 3 includes clock-to-output delay of Signal/Data clocked receiver, Cycle 4 includes clock-to-output delay of Signal/Data sampling flip-flop.

MLB 6-pin pipeline diagram is shown in [Figure 9](#).

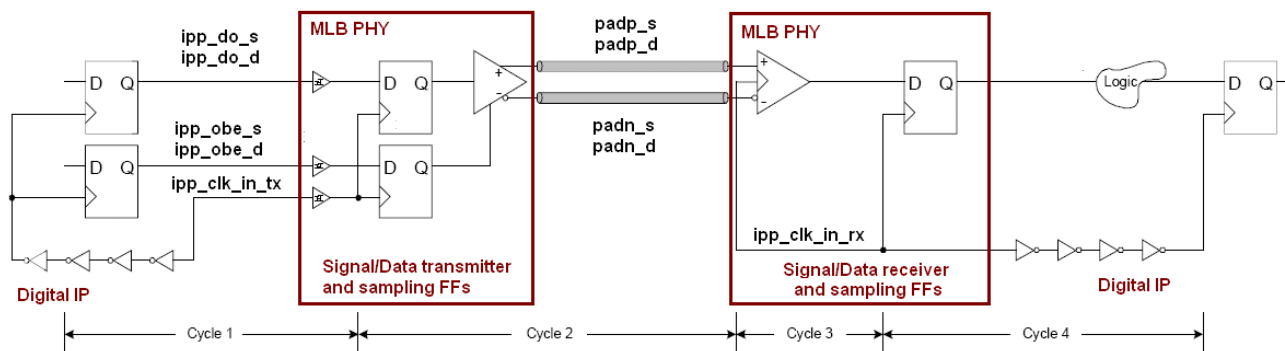


Figure 9. MLB 6-Pin Pipeline Diagram

[Table 34](#) shows the AC parameters for MLB I/O.

4.8 Output Buffer Impedance Parameters

Table 34. I/O AC Parameters of MLB PHY

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew ¹	t_{SKD}	Rload = 50 Ω between padp and padn	—	—	0.1	ns
Transition Low to High Time ²	t_{TLH}		—	—	1	
Transition High to Low Time	t_{THL}		—	—	1	
MLB external clock Operating Frequency	fclk_ext	—	—	—	102.4	MHz
MLB PLL clock Operating Frequency	fclk_pll	—	—	—	307.2	MHz

¹ $t_{SKD} = |t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

² Measurement levels are 20-80% from output voltage.

This section defines the I/O impedance parameters of the i.MX 6Solo/6DualLite processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

Table 64. Camera Input Signal Cross Reference, Format, and Bits Per Cycle (continued)

Signal Name ¹	RGB565 8 bits 2 cycles	RGB565 ² 8 bits 3 cycles	RGB666 ³ 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr ⁴ 8 bits 2 cycles	RGB565 ⁵ 16 bits 1 cycle	YCbCr ⁶ 16 bits 1 cycle	YCbCr ⁷ 16 bits 1 cycle	YCbCr ⁸ 20 bits 1 cycle
IPUx_CSIx_DATA13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
IPUx_CSIx_DATA14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
IPUx_CSIx_DATA15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
IPUx_CSIx_DATA16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
IPUx_CSIx_DATA17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
IPUx_CSIx_DATA18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
IPUx_CSIx_DATA19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

¹ IPUx_CSIx stands for IPUx_CSI0 or IPUx_CSI1.

² The MSB bits are duplicated on LSB bits implementing color extension.

³ The two MSB bits are duplicated on LSB bits implementing color extension.

⁴ YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).

⁵ RGB 16 bits—Supported in two ways: (1) As a “generic data” input, with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.

⁶ YCbCr 16 bits—Supported as a “generic-data” input, with no on-the-fly processing.

⁷ YCbCr 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).

⁸ YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.11.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPUx_CSIx_VSYNC and IPUx_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPUx_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPUx_CSIx_VSYNC and IPUx_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPUx_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPUx_CSIx_DATA_EN bus.

4.11.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The IPP_DISP_CLK is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The IPUx_DIx_PIN01—IPUx_DIx_PIN07 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any other independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The IPUx_DIx_D0_CS and IPUx_DIx_D1_CS pins are dedicated to provide chip select signals to two displays.
- The IPUx_DIx_PIN11—IPUx_DIx_PIN17 are general purpose asynchronous pins, that can be used to provide WR, RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated “local start point”. The synchronous display controls can be placed on time axis with DI's offset, up and down parameters.

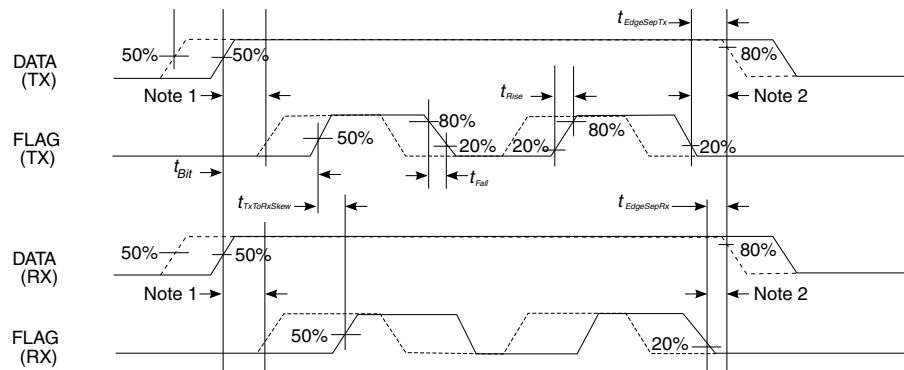
Table 67 shows timing characteristics of signals presented in Figure 64 and Figure 65.

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	(¹)	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	$\text{DISP_CLK_PER_PIXEL} \times \text{Tdicp}$	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to n components.	ns
IP7	Screen width time	Tsw	$(\text{SCREEN_WIDTH}) \times \text{Tdicp}$	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter ² .	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	$\text{BGXP} \times \text{Tdicp}$	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	$(\text{SCREEN_WIDTH} - \text{BGXP} - \text{FW}) \times \text{Tdicp}$	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	$(\text{SCREEN_HEIGHT}) \times \text{Tsw}$	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	$\text{BGYP} \times \text{Tsw}$	BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	$(\text{SCREEN_HEIGHT} - \text{BGYP} - \text{FH}) \times \text{Tsw}$	Width of second Vertical blanking interval in line. The FH should be built by suitable DI's counter.	ns
IP5o	Offset of IPP_DISP_CLK	Todicp	$\text{DISP_CLK_OFFSET} \times \text{Tdiclk}$	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter	ns

Table 72. DATA and FLAG Timing (continued)

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{\text{EdgeSepTx, min}}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4.00 ns	2.00 ns
$t_{\text{EdgeSepRx, min}}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns	1.75 ns



¹ This case shows that the DATA signal has slowed down more compared to the FLAG signal

² This case shows that the FLAG signal has slowed down more compared to the DATA signal.

Figure 81. DATA and FLAG Signal Timing

4.11.14 MediaLB (MLB) Characteristics

4.11.14.1 MediaLB (MLB) DC Characteristics

Table 73 lists the MediaLB 3-pin interface electrical characteristics.

Table 73. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note ¹	1.8	—	V
Low level output threshold	V_{OL}	$I_{OL} = 6 \text{ mA}$	—	0.4	V
High level output threshold	V_{OH}	$I_{OH} = -6 \text{ mA}$	2.0	—	V
Input leakage current	I_L	$0 < V_{in} < V_{DD}$	—	± 10	μA

¹ Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

4.11.14.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module. Figure 82 show the timing of MediaLB 3-pin interface, and Table 75 and Table 76 lists the MediaLB 3-pin interface timing characteristics.

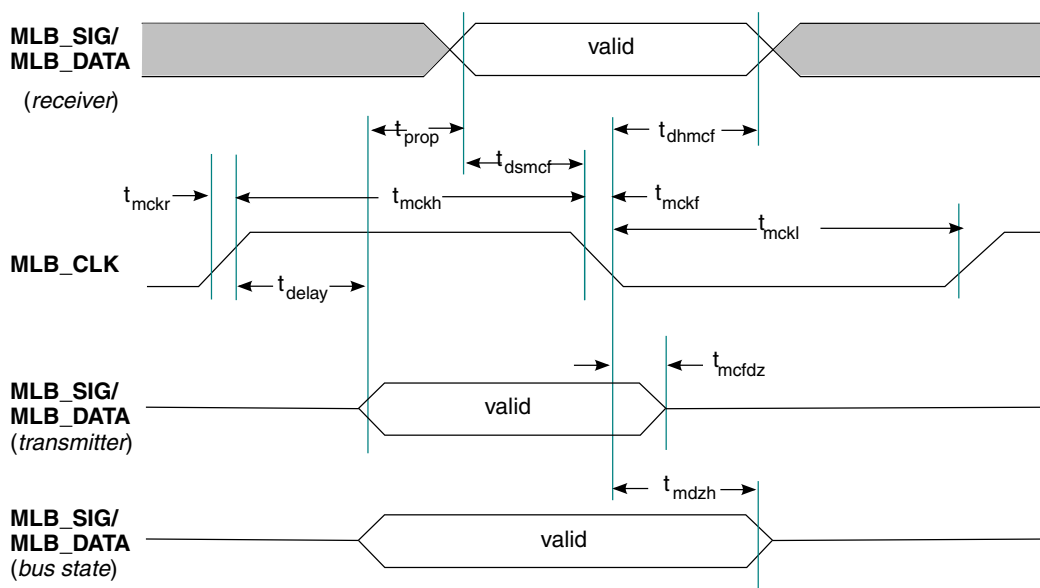


Figure 82. MediaLB 3-Pin Timing

Ground = 0.0 V; Load Capacitance = 60 pF; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 75. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLB_CLK operating frequency ¹	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz 512xFs at 50.0 kHz
MLB_CLK rise time	t_{mckr}	—	3	ns	V_{IL} TO V_{IH}
MLB_CLK fall time	t_{mckf}	—	3	ns	V_{IH} TO V_{IL}
MLB_CLK low time ²	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLB_CLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling	t_{dsmcf}	1	—	ns	—
MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLB_SIG/MLB_DATA output high impedance from MLB_CLK low	t_{mcdfz}	0	t_{mckl}	ns	³
Bus Hold from MLB_CLK low	t_{mdzh}	4	—	ns	—

4.11.15.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω . 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.16 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 84 depicts the timing of the PWM, and Table 78 lists the PWM timing parameters.

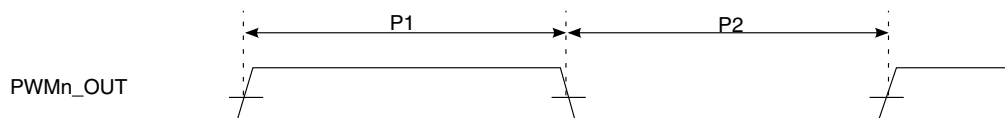


Figure 84. PWM Timing

Table 78. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.11.17 SCAN JTAG Controller (SJC) Timing Parameters

Figure 85 depicts the SJC test clock input timing. Figure 86 depicts the SJC boundary scan timing. Figure 87 depicts the SJC test access port. Signal parameters are listed in Table 79.

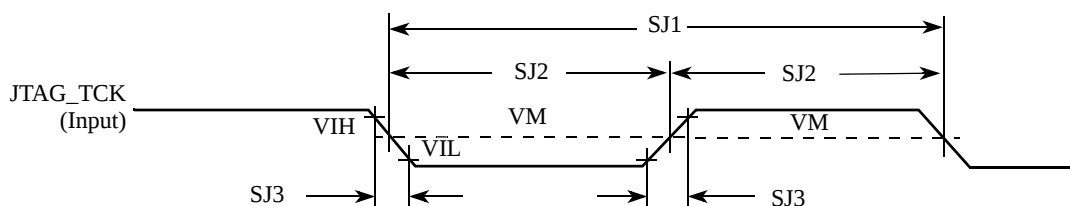


Figure 85. Test Clock Input Timing Diagram

Table 80. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf)	—	—	1.5	ns
• Skew	—	—	24.2	
• Transition rising	—	—	31.3	
SPDIF_OUT output (Load = 30pf)	—	—	1.5	ns
• Skew	—	—	13.6	
• Transition rising	—	—	18.0	
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stckp	40.0	—	ns
SPDIF_ST_CLK high period	stckph	16.0	—	ns
SPDIF_ST_CLK low period	stckpl	16.0	—	ns

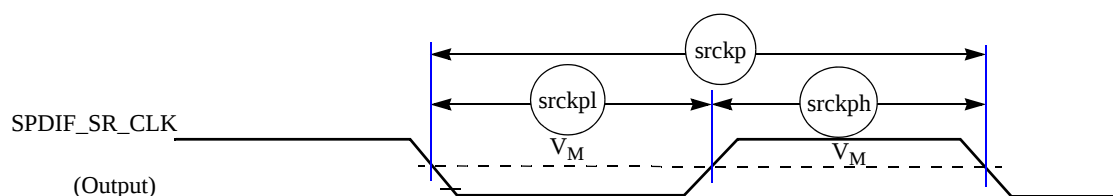


Figure 89. SPDIF_SR_CLK Timing Diagram

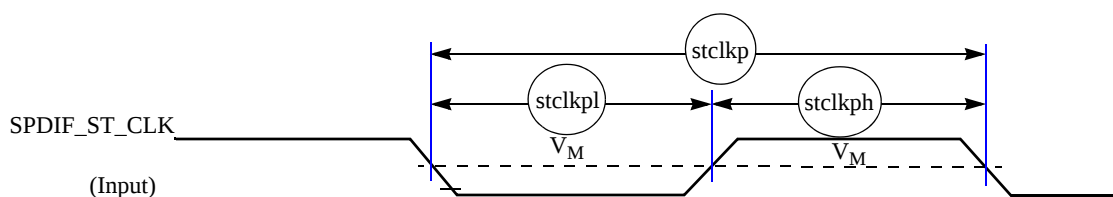


Figure 90. SPDIF_ST_CLK Timing Diagram

Table 82. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDxRXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDxRXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDxRXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDxRXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDxRXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value ²
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	100 kΩ pull-up
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	100 kΩ pull-up
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	100 kΩ pull-up
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	100 kΩ pull-up
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	100 kΩ pull-up
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	100 kΩ pull-up
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	100 kΩ pull-up
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	100 kΩ pull-up
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	100 kΩ pull-up
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	100 kΩ pull-up
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	100 kΩ pull-up
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	100 kΩ pull-up
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	100 kΩ pull-up
Note: DRAM_D32 to DRAM_D63 are only available for i.MX 6DualLite chip; for i.MX 6Solo chip, these pins are NC.							
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	100 kΩ pull-up
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	100 kΩ pull-up
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	100 kΩ pull-up
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	100 kΩ pull-up
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	100 kΩ pull-up
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	100 kΩ pull-up
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	100 kΩ pull-up
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	100 kΩ pull-up
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	100 kΩ pull-up
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	100 kΩ pull-up
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	100 kΩ pull-up
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	100 kΩ pull-up
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	DRAM_DATA44	Input	100 kΩ pull-up
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	DRAM_DATA45	Input	100 kΩ pull-up
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	DRAM_DATA46	Input	100 kΩ pull-up
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	DRAM_DATA47	Input	100 kΩ pull-up
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	DRAM_DATA48	Input	100 kΩ pull-up
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	DRAM_DATA49	Input	100 kΩ pull-up
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	DRAM_DATA50	Input	100 kΩ pull-up
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	DRAM_DATA51	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value ²
DRAM_SDCLK_1_B	AE14	NVCC_DRAM	—	—	DRAM_SDCLK1_N	—	—
DRAM_SDODT0	AC16	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	Low
DRAM_SDODT1	AB17	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	Low
DRAM_SDQS0	AE3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	Hi-Z
DRAM_SDQS0_B	AD3	NVCC_DRAM	—	—	DRAM_SDQS0_N	—	—
DRAM_SDQS1	AD6	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	Hi-Z
DRAM_SDQS1_B	AE6	NVCC_DRAM	—	—	DRAM_SDQS1_N	—	—
DRAM_SDQS2	AD8	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS2_P	Input	Hi-Z
DRAM_SDQS2_B	AE8	NVCC_DRAM	—	—	DRAM_SDQS2_N	—	—
DRAM_SDQS3	AC10	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS3_P	Input	Hi-Z
DRAM_SDQS3_B	AB10	NVCC_DRAM	—	—	DRAM_SDQS3_N	—	—
DRAM_SDQS4	AD18	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS4_P	Input	Hi-Z
DRAM_SDQS4_B	AE18	NVCC_DRAM	—	—	DRAM_SDQS4_N	—	—
DRAM_SDQS5	AD20	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS5_P	Input	Hi-Z
DRAM_SDQS5_B	AE20	NVCC_DRAM	—	—	DRAM_SDQS5_N	—	—
DRAM_SDQS6	AD23	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS6_P	Input	Hi-Z
DRAM_SDQS6_B	AE23	NVCC_DRAM	—	—	DRAM_SDQS6_N	—	—
DRAM_SDQS7	AA25	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS7_P	Input	Hi-Z
DRAM_SDQS7_B	AA24	NVCC_DRAM	—	—	DRAM_SDQS7_N	—	—
DRAM_SDWE	AB16	NVCC_DRAM	DDR	ALT0	DRAM_SDWE	Output	Low
DSI_CLK0M	H3	NVCC_MIPI	ANALOG	—	DSI_CLK_N	—	—
DSI_CLK0P	H4	NVCC_MIPI	ANALOG	—	DSI_CLK_P	—	—
DSI_D0M	G2	NVCC_MIPI	ANALOG	—	DSI_DATA0_N	—	—
DSI_D0P	G1	NVCC_MIPI	ANALOG	—	DSI_DATA0_P	—	—
DSI_D1M	H2	NVCC_MIPI	ANALOG	—	DSI_DATA1_N	—	—
DSI_D1P	H1	NVCC_MIPI	ANALOG	—	DSI_DATA1_P	—	—
EIM_A16	H25	NVCC_EIM	GPIO	ALT0	EIM_ADDR16	Output	Low
EIM_A17	G24	NVCC_EIM	GPIO	ALT0	EIM_ADDR17	Output	Low
EIM_A18	J22	NVCC_EIM	GPIO	ALT0	EIM_ADDR18	Output	Low
EIM_A19	G25	NVCC_EIM	GPIO	ALT0	EIM_ADDR19	Output	Low
EIM_A20	H22	NVCC_EIM	GPIO	ALT0	EIM_ADDR20	Output	Low
EIM_A21	H23	NVCC_EIM	GPIO	ALT0	EIM_ADDR21	Output	Low
EIM_A22	F24	NVCC_EIM	GPIO	ALT0	EIM_ADDR22	Output	Low
EIM_A23	J21	NVCC_EIM	GPIO	ALT0	EIM_ADDR23	Output	Low
EIM_A24	F25	NVCC_EIM	GPIO	ALT0	EIM_ADDR24	Output	Low
EIM_A25	H19	NVCC_EIM	GPIO	ALT0	EIM_ADDR25	Output	Low

Table 99. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo (continued)

R	P	N	M	L	K	J	H
GPIO_17	CSIO_PIXCLK	CSIO_DAT4	CSIO_DAT10	CSIO_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P
GPIO_16	CSIO_DAT5	CSIO_VSYNC	CSIO_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M
GPIO_7	CSIO_DATA_EN	CSIO_DAT7	CSIO_DAT11	CSIO_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M
GPIO_5	CSIO_MCLK	CSIO_DAT6	CSIO_DAT14	CSIO_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P
GPIO_8	GPIO_19	CSIO_DAT9	CSIO_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK
GPIO_4	GPIO_18	CSIO_DAT8	CSIO_DAT18	CSIO_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD
GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP
GND	GND	GND	GND	GND	GND	GND	GND
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN
VDDSOC_CAP	GND	GND	GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
GND	GND	NC	GND	GND	GND	GND	GND
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
GND	GND	GND	GND	GND	GND	GND	GND
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
NVCC_DRAM	GND	GND	GND	GND	GND	GND	GND
NVCC_ENET	NVCC_LCD	DIO_DISP_CLK	NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25
DISP0_DAT13	DISP0_DAT4	DIO_PIN3	EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21
DISP0_DAT10	DISP0_DAT3	DIO_PIN15	EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31
DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20
DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21
DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0
DISP0_DAT5	DIO_PIN4	DIO_PIN2	EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16
R	P	N	M	L	K	J	H

Table 99. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo (continued)

AC	AB	AA	Y	W	V	U	T
DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2
DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9
DRAM_DQM0	GND	LVDS1_TX3_N	LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6
DRAM_D2	DRAM_D6	LVDS1_TX3_P	LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1
DRAM_D13	DRAM_D12	DRAM_D3	GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0
DRAM_DQM1	DRAM_D14	DRAM_D10	DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4
DRAM_D15	DRAM_D16	GND	DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3
DRAM_D22	DRAM_DQM2	DRAM_D17	DRAM_D21	GND	GND	GND	GND
DRAM_D28	DRAM_D18	DRAM_D23	DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN
DRAM_SDQS3	DRAM_SDQS3_B	GND	DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP
DRAM_D31	DRAM_D27	DRAM_SDCKE1	DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND
DRAM_A11	DRAM_SDBA2	DRAM_A14	DRAM_A15	GND	NVCC_DRAM	GND	GND
DRAM_A6	DRAM_A8	GND	DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP
DRAM_A0	DRAM_A1	DRAM_A2	DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP
DRAM_SDBA0	DRAM_RAS	DRAM_A10	DRAM_SDBA1	GND	NVCC_DRAM	GND	GND
DRAM_SDODT0	DRAM_SDWE	GND	DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN
DRAM_A13	DRAM_SDODT1	NC	NC	GND	NVCC_DRAM	GND	GND
NC	NC	NC	NC	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
NC	NC	GND	NC	GND	GND	GND	GND
NC	NC	NC	NC	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21
NC	NC	NC	NC	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16
NC	NC	GND	NC	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15
NC	NC	NC	NC	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11
NC	GND	NC	GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12
NC	NC	NC	NC	NC	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9
AC	AB	AA	Y	W	V	U	T

Table 100. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite (continued)

M	L	K	J	H	G	F	E
CSIO_DAT10	CSIO_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P	DSI_D0P	NC	NC
CSIO_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M	DSI_D0M	NC	NC
CSIO_DAT11	CSIO_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M	GND	CSI_CLK0P	CSI_D0P
CSIO_DAT14	CSIO_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P	DSI_REXT	CSI_CLK0M	CSI_D0M
CSIO_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK	JTAG_TDI	GND	GND
CSIO_DAT18	CSIO_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD	JTAG_TDO	GND	GND
HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP	PCIE_VPH	GND	GND
GND	GND	GND	GND	GND	PCIE_VPTX	GND	NVCC_PLL_OUT
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN	VDD_SNVIS_CAP	VDDUSB_CAP	USB_OTG_VBUS
GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP	GND	USB_H1_DN	USB_H1_DP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDD_SNVIS_IN	PMIC_STBY_REQ	TAMPER
GND	GND	GND	GND	GND	NC	BOOT_MODE1	TEST_MODE
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	NC	SD3_DAT7	SD3_DAT6
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	NVCC_SD3	SD3_DAT1	SD3_DAT0
GND	GND	GND	GND	GND	NVCC_NANDF	NANDF_CS0	NANDF_WP_B
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_SD1	NANDF_D2	SD4_CLK
VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	NVCC_SD2	SD4_DAT2	NANDF_D6
GND	GND	GND	GND	GND	NVCC_RGMII	SD1_DAT3	SD4_DAT4
NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25	GND	SD2_CMD	SD1_DAT2
EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21	EIM_D20	RGMII_TD1	SD2_DAT1
EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31	EIM_D19	EIM_D17	RGMII_TD2
EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20	EIM_D25	EIM_D24	EIM_EB2
EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21	EIM_D28	EIM_EB3	EIM_D22
EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0	EIM_A17	EIM_A22	EIM_D26
EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16	EIM_A19	EIM_A24	EIM_D27
M	L	K	J	H	G	F	E

Table 100. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite (continued)

	AE	AD	AC	AB	AA
1	GND	DRAM_D5	DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P
2	DRAM_D1	DRAM_D0	DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N
3	DRAM_SDQS0	DRAM_SDQS0_B	DRAM_DQM0	GND	LVDS1_TX3_N
4	DRAM_D7	GND	DRAM_D2	DRAM_D6	LVDS1_TX3_P
5	DRAM_D9	DRAM_D8	DRAM_D13	DRAM_D12	DRAM_D3
6	DRAM_SDQS1_B	DRAM_SDQS1	DRAM_DQM1	DRAM_D14	DRAM_D10
7	DRAM_D11	GND	DRAM_D15	DRAM_D16	GND
8	DRAM_SDQS2_B	DRAM_SDQS2	DRAM_D22	DRAM_DQM2	DRAM_D17
9	DRAM_D24	DRAM_D29	DRAM_D28	DRAM_D18	DRAM_D23
10	DRAM_DQM3	GND	DRAM_SDQS3	DRAM_SDQS3_B	GND
11	DRAM_D26	DRAM_D30	DRAM_D31	DRAM_D27	DRAM_SDCKE1
12	DRAM_A9	DRAM_A12	DRAM_A11	DRAM_SDBA2	DRAM_A14
13	DRAM_A5	GND	DRAM_A6	DRAM_A8	GND
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1	DRAM_A0	DRAM_A1	DRAM_A2
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0	DRAM_SDBA0	DRAM_RAS	DRAM_A10
16	DRAM_CAS	GND	DRAM_SDODT0	DRAM_SDWE	GND
17	ZQPAD	DRAM_CS1	DRAM_A13	DRAM_SDODT1	DRAM_D32
18	DRAM_SDQS4_B	DRAM_SDQS4	DRAM_D34	DRAM_DQM4	DRAM_D33
19	DRAM_D35	GND	DRAM_D39	DRAM_D38	GND
20	DRAM_SDQS5_B	DRAM_SDQS5	DRAM_DQM5	DRAM_D41	DRAM_D45
21	DRAM_D46	DRAM_D43	DRAM_D47	DRAM_D42	DRAM_D57
22	DRAM_D49	GND	DRAM_D48	DRAM_D52	GND
23	DRAM_SDQS6_B	DRAM_SDQS6	DRAM_D53	DRAM_D60	DRAM_D61
24	DRAM_D50	DRAM_DQM6	DRAM_D51	GND	DRAM_SDQS7_B
25	GND	DRAM_D54	DRAM_D55	DRAM_D56	DRAM_SDQS7
	AE	AD	AC	AB	AA