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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	176 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc662-04-pt

PIC16C64X & PIC16C66X

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2.0 PIC16C64X & PIC16C66X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information in the Product Identification System page at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in Cerdip package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® Plus and PRO MATE® II programmers both support programming of the PIC16C64X & PIC16C66X.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

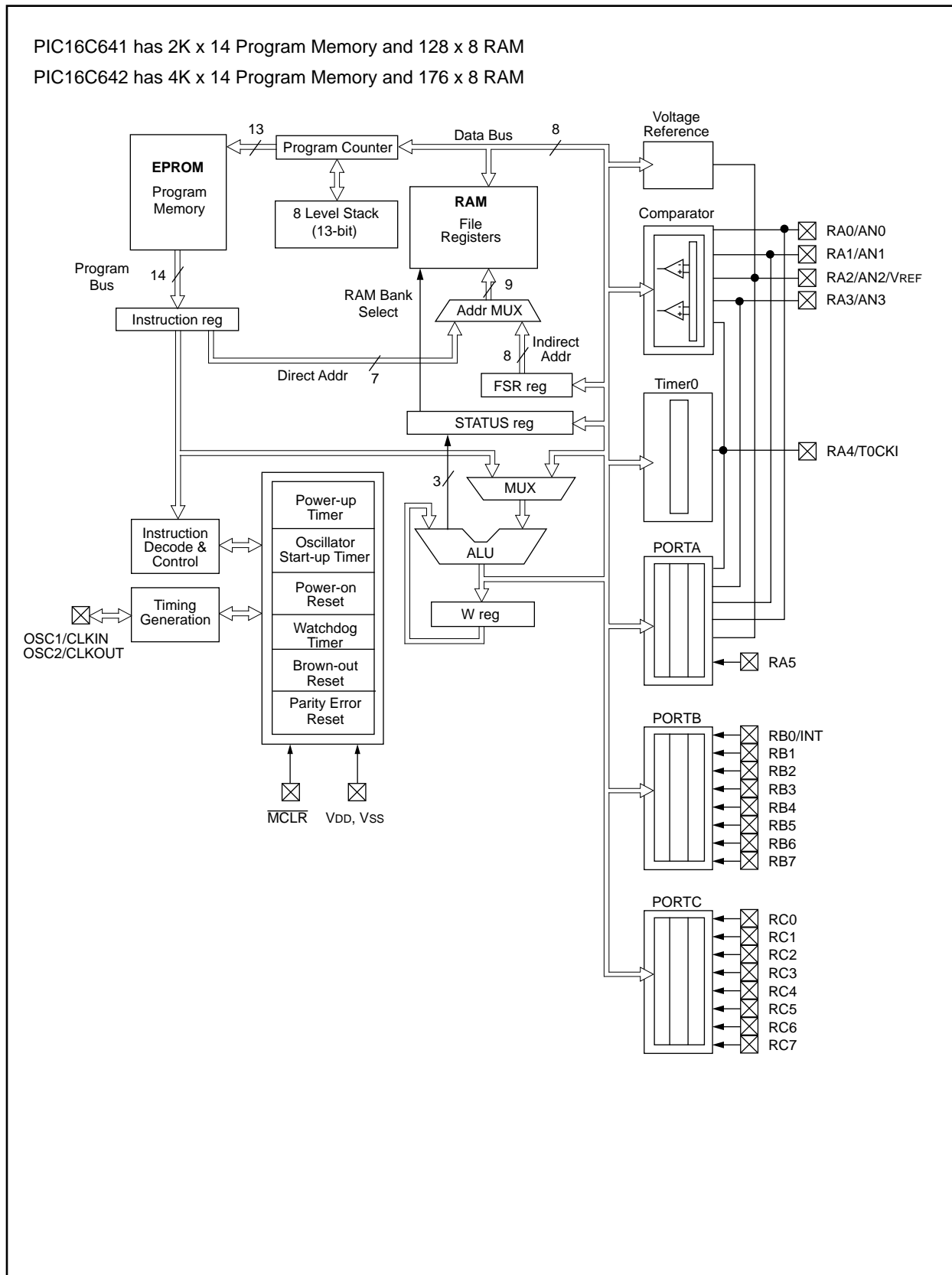
2.4 Serialized Quick-Turnaround- Production (SQTPSM) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

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FIGURE 3-1: PIC16C641/642 BLOCK DIAGRAM



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TABLE 3-1: PIC16C641/642 PINOUT DESCRIPTION

Name	Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	I	ST/CMOS	Oscillator crystal input or external clock source input.
OSC2/CLKOUT	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	1	I/P	ST	Master clear (reset) input or programming voltage input. This pin is an active low reset to the device.
RA0/AN0	2	I/O	ST	PORTA is a bi-directional I/O port. Analog comparator input. Analog comparator input. Analog comparator input or VREF output. Analog comparator input or comparator output. Can be selected to be the clock input to the Timer0 timer/counter or a comparator output. Output is open drain type.
RA1/AN1	3	I/O	ST	
RA2/AN2/VREF	4	I/O	ST	
RA3/AN3	5	I/O	ST	
RA4/T0CKI	6	I/O	ST	
RA5	7	I/O	ST	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. RB0 can also be selected as an external interrupt pin. Interrupt on change pin. Interrupt on change pin. Interrupt on change pin. Serial programming clock. Interrupt on change pin. Serial programming data.
RB0/INT	21	I/O	TTL/ST ⁽¹⁾	
RB1	22	I/O	TTL	
RB2	23	I/O	TTL	
RB3	24	I/O	TTL	
RB4	25	I/O	TTL	
RB5	26	I/O	TTL	
RB6	27	I/O	TTL/ST ⁽²⁾	
RB7	28	I/O	TTL/ST ⁽²⁾	
RC0	11	I/O	ST	PORTC is a bi-directional I/O port.
RC1	12	I/O	ST	
RC2	13	I/O	ST	
RC3	14	I/O	ST	
RC4	15	I/O	ST	
RC5	16	I/O	ST	
RC6	17	I/O	ST	
RC7	18	I/O	ST	
Vss	8,19	P	—	Ground reference for logic and I/O pins.
VDD	20	P	—	Positive supply for logic and I/O pins.

Legend: O = output I/O = input/output P = power
 I = input — = not used ST = Schmitt Trigger input
 TTL = TTL input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

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4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable and flag bits for all non-peripheral interrupt sources.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-7: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF
bit7				bit0			

R= Readable bit
W= Writable bit
U= Unimplemented bit, read as '0'
- n= Value at POR reset

bit 7: **GIE:** Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5: **TOIE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **TOIF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = When at least one of the RB7:RB4 pins changed state (See Section 5.2 to clear interrupt)
0 = None of the RB7:RB4 pins have changed state

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4.5 Indirect Addressing, INDF, and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the file select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-12. However, bit IRP is not used in the PIC16C64X & PIC16C66X.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-1.

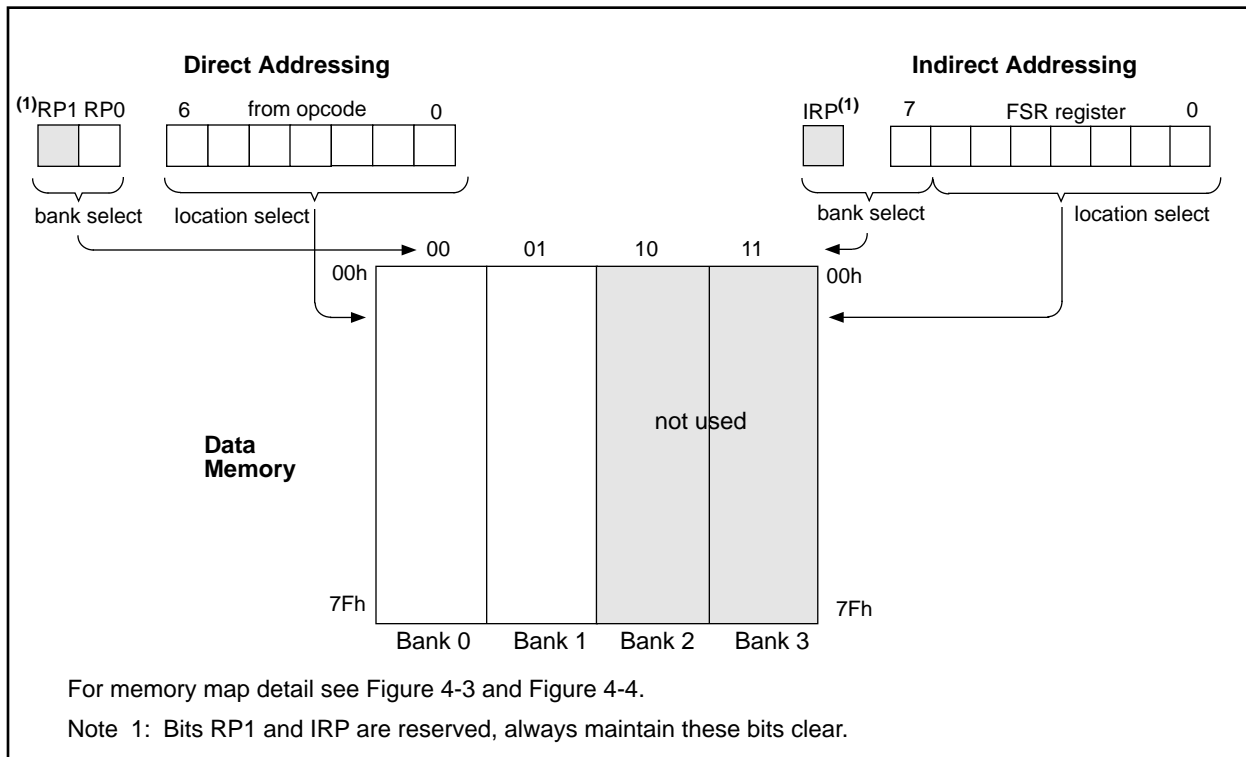
EXAMPLE 4-1: INDIRECT ADDRESSING

```

movlw 0x20 ;initialize pointer
movwf FSR ;to RAM
NEXT    clrf INDF ;clear INDF register
        incf FSR ;inc pointer
        btfss FSR,4 ;all done?
        goto NEXT ;no goto next
                ;yes continue

CONTINUE:
    
```

FIGURE 4-12: DIRECT/INDIRECT ADDRESSING



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5.7 Parallel Slave Port (PIC16C661 and PIC16C662 only)

PORTD operates as an 8-bit wide parallel slave port, or as a microprocessor port when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through \overline{RD} control input pin (RE0/ \overline{RD}) and \overline{WR} control input pin (RE1/ \overline{WR}).

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting PSPMODE enables port pin RE0/ \overline{RD} to be the \overline{RD} input, RE1/ \overline{WR} to be the \overline{WR} input and RE2/ \overline{CS} to be the \overline{CS} (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set).

There are actually two 8-bit latches, one for data-out (from the PIC16/17) and one for data input. The user writes 8-bit data to PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRISD register is ignored since the microprocessor is controlling the direction of data flow.

Input Buffer Full Status Flag bit IBF (TRISE<7>) is set if a received word is waiting to be read by the CPU. Once the PORTD input latch is read, bit IBF is cleared. IBF is a read only status bit. Output Buffer Full Status Flag bit OBF (TRISE<6>) is set if a word written to PORTD latch is waiting to be read by the external bus. Once the PORTD output latch is read by the microprocessor, bit OBF is cleared. Input Buffer Overflow Status flag bit IBOV (TRISE<5>) is set if a second write to the microprocessor port is attempted when the previous word has not been read by the CPU (the first word is retained in the buffer).

When not in Parallel Slave Port mode, bits IBF and OBF are held clear. However, if flag bit IBOV was previously set, it must be cleared in software.

An interrupt is generated and latched into flag bit PSPIF (PIR1<7>) when a read or a write operation is completed. Flag bit PSPIF must be cleared by user software. The interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).

FIGURE 5-12: PORTD AND PORTE AS A PARALLEL SLAVE PORT

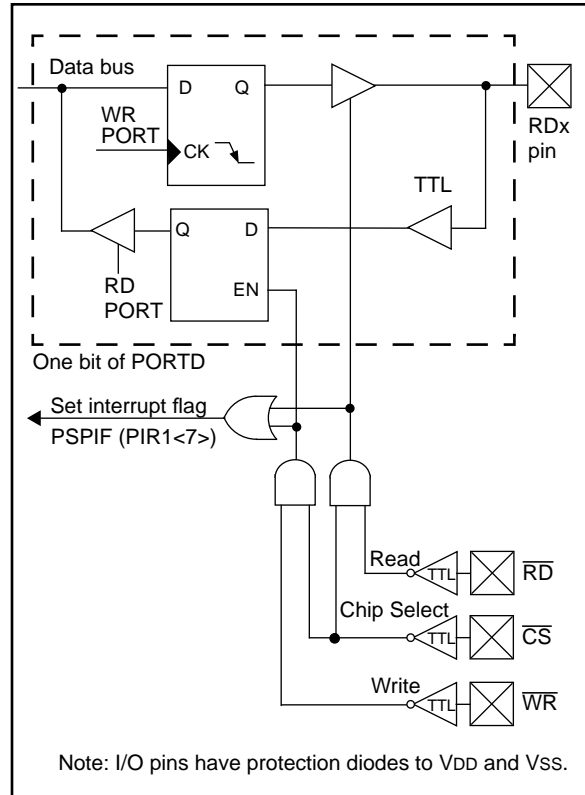


TABLE 5-11: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	PSP7	PSP6	PSP5	PSP4	PSP3	PSP2	PSP1	PSP0	xxxx xxxx	uuuu uuuu
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111
0Ch	PIR1	PSPIF ⁽¹⁾	CMIF	—	—	—	—	—	—	00-- ----	00-- ----
8Ch	PIE1	PSPIE ⁽¹⁾	CMIE	—	—	—	—	—	—	00-- ----	00-- ----

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by the PSP.

Note 1: These bits are reserved on the PIC16C641/642, always maintain these bits clear.

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FIGURE 6-3: TMR0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

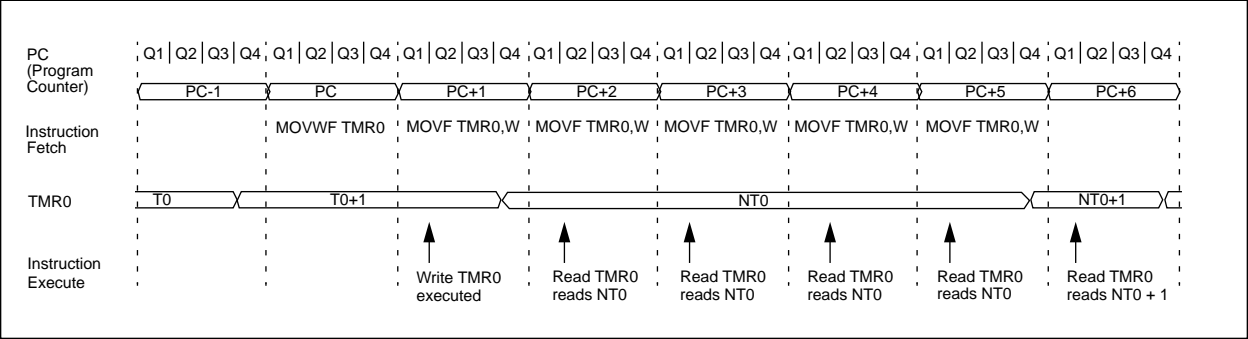
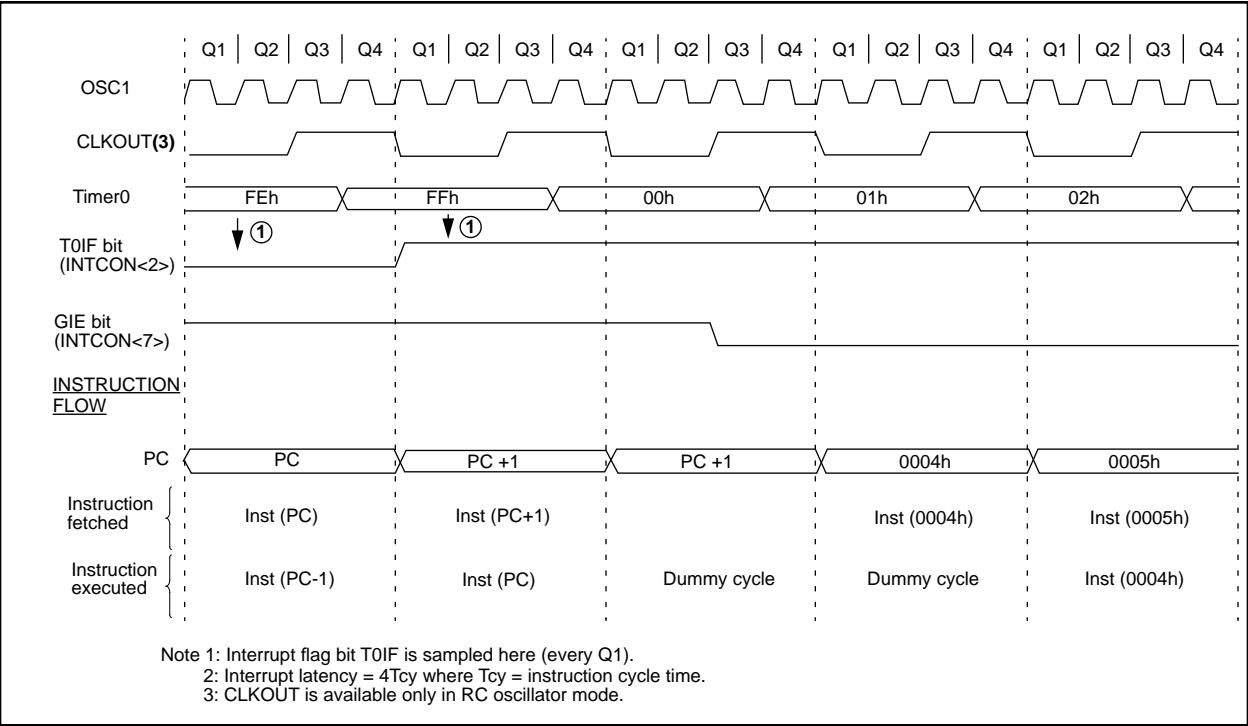


FIGURE 6-4: TMR0 INTERRUPT TIMING



6.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.2.1 EXTERNAL CLOCK SYNCHRONIZATION

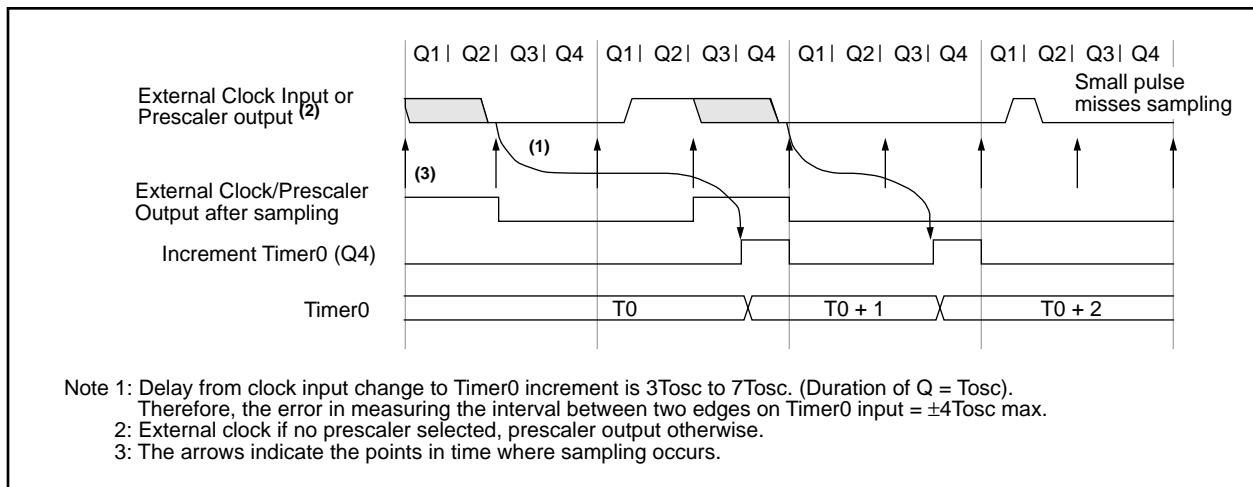
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41, and 42 in the electrical specification of the desired device.

6.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



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NOTES:

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7.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is guaranteed to have a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (Table 12-2 and Table 12-3).

7.5 Comparator Outputs

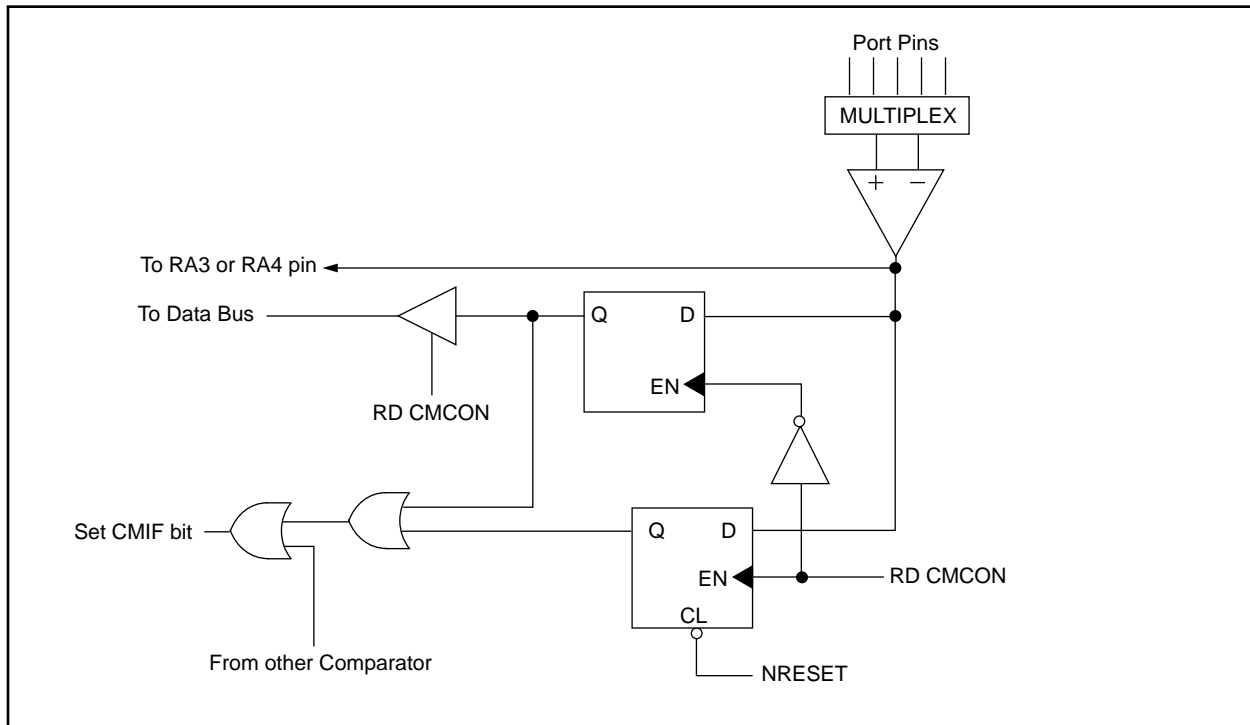
The comparator outputs are read through the CMCON register. These bits are read only. The comparator outputs may also be directly output to the RA3 and RA4 I/O pins. When CM2:CM0 = 110, multiplexors in the output path of the RA3 and RA4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 7-4 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/disable for the RA3 and RA4 pins while in this mode.

Note 1: When reading the PORTA register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.

Note 2: Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

FIGURE 7-4: COMPARATOR OUTPUT BLOCK DIAGRAM



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9.4.5 PARITY ERROR RESET (PER)

PIC16C64X & PIC16C66X devices have on-chip parity bits that can be used to verify the contents of program memory. Parity bits may be useful in applications in order to increase overall reliability of a system.

There are two parity bits for each word of Program Memory. The parity bits are computed on alternating bits of the program word. One computation is performed using even parity, the other using odd parity. As a program executes, the parity is verified. The even parity bit is XOR'd with the even bits in the program memory word. The odd parity bit is negated and XOR'd with the odd bits in the program memory word. When an error is detected, a reset is generated and the $\overline{\text{PER}}$ flag bit in the PCON register is set. This indication can allow software to act on a failure. However, there is no indication of the program memory location of the failure of the Program Memory. This flag can only be cleared in software or by a POR.

The parity array is user selectable during programming. Bit7 of the configuration word located at address 2007h can be programmed (read as '0') to disable parity checking. If left unprogrammed (read as '1'), parity checking is enabled.

9.4.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then the OST is activated. The total time-out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in RC mode with the $\overline{\text{PWRTE}}$ bit set (PWRT disabled), there will be no time-out at all. Figure 9-9, Figure 9-10 and Figure 9-11 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately (Figure 9-10). This is useful for testing purposes or to synchronize more than one device operating in parallel.

Table 9-5 shows the reset conditions for some special registers, while Table 9-6 shows the reset conditions for all the registers.

9.4.7 POWER CONTROL/STATUS REGISTER (PCON)

The power control/status register, PCON (address 8Eh) has four bits. See Figure 4-10 for register.

Bit0 is $\overline{\text{BOR}}$ (Brown-out Reset). $\overline{\text{BOR}}$ is unknown on a Power-on-reset. It must initially be set by the user and checked on subsequent resets to see if $\overline{\text{BOR}} = '0'$ indicating that a Brown-out Reset has occurred. The $\overline{\text{BOR}}$ status bit is a "don't care" bit and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

Bit1 is $\overline{\text{POR}}$ (Power-on Reset). It is cleared on a Power-on Reset and is unaffected otherwise. The user set this bit following a Power-on Reset. On subsequent resets if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset must have occurred.

Bit2 is $\overline{\text{PER}}$ (Parity Error Reset). It is cleared on a Parity Error Reset and must be set by user software. It will also be set on a Power-on Reset.

Bit7 is MPEEN (Memory Parity Error Enable). This bit reflects the status of the MPEEN bit in configuration word. It is unaffected by any reset or interrupt.

TABLE 9-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset	Wake-up from SLEEP
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$		
XT, HS, LP	72 ms + 1024 TOSC	1024 TOSC	72 ms + 1024 TOSC	1024 TOSC
RC	72 ms	—	72 ms	—

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TABLE 9-6: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset Brown-out Reset Parity Error Reset	MCLR Reset during: - normal operation - SLEEP or WDT Reset	Wake up from SLEEP through: - interrupt - WDT time-out
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1 ⁽²⁾
STATUS	03h	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--xx 0000	--xu 0000	--uu uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD ⁽⁴⁾	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE ⁽⁴⁾	09h	---- -xxx	---- -uuu	---- -uuu
CMCON	1Fh	00-- 0000	00-- 0000	uu-- uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
PIR1	0Ch	00-- ----	00-- ----	uu-- ---- ⁽¹⁾
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
TRISD ⁽⁴⁾	88h	1111 1111	1111 1111	uuuu uuuu
TRISE ⁽⁴⁾	89h	0000 -111	0000 -111	uuuu -uuu
PIE1	8Ch	00-- ----	00-- ----	uu-- ----
PCON	8Eh	u--- -qqq	u--- -uuu	u--- -uuu
VRCON	9Fh	000- 0000	000- 0000	uuu- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 9-5 for reset value for specific condition.

4: These registers are associated with the Parallel Slave Port and are not implemented on the PIC16C641/642.

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9.7 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. The block diagram is shown in Figure 9-17. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. This means that the WDT will run, even if the clock on the OSC1 and OSC2 pins has been stopped, for example, by execution of a *SLEEP* instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in *SLEEP* mode, a WDT time-out causes the device to wake-up and continue with normal operation, this is known as a WDT wake-up. The WDT can be permanently disabled by clearing configuration bit WDTE (Section 9.1).

9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out period varies with temperature, VDD and process variations from part to part (see DC specs). If longer time-outs are desired, a prescaler with a division ratio of up to 1:128 can be assigned to

the WDT, under software control, by writing to the OPTION register. Thus, time-out periods of up to 2.3 seconds can be realized.

The *CLRWDT* and *SLEEP* instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET.

The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out (WDT Reset and WDT wake-up).

9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note: When the prescaler is assigned to the WDT, always execute a *CLRWDT* instruction before changing the prescale value, otherwise a WDT reset may occur.

FIGURE 9-17: WATCHDOG TIMER BLOCK DIAGRAM

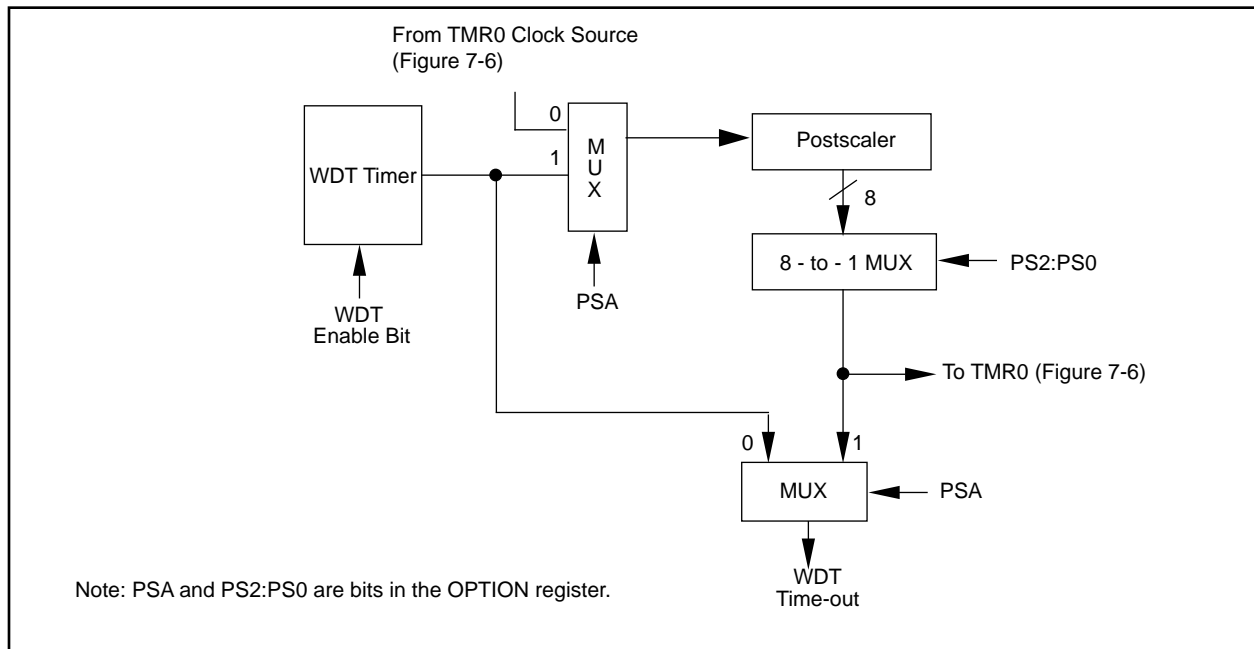


FIGURE 9-18: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	MPEEN	BODEN ⁽¹⁾	CP1	CP0	$\overline{\text{PWRTE}}$ ⁽¹⁾	WDTE	FOSC1	FOSC0
81h	OPTION	RBPUP	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 9-1 for details of the operation of these bits.

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BCF	Bit Clear f				
Syntax:	[<i>label</i>] BCF f,b				
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$				
Operation:	$0 \rightarrow (f)$				
Status Affected:	None				
Encoding:	<table><tr><td>01</td><td>00bb</td><td>bfff</td><td>ffff</td></tr></table>	01	00bb	bfff	ffff
01	00bb	bfff	ffff		
Description:	Bit 'b' in register 'f' is cleared.				
Words:	1				
Cycles:	1				
Example	<pre>BCF FLAG_REG, 7</pre> <p>Before Instruction FLAG_REG = 0xC7</p> <p>After Instruction FLAG_REG = 0x47</p>				

BSF		Bit Set f			
Syntax:	[<i>label</i>] BSF f,b				
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$				
Operation:	$1 \rightarrow (f)$				
Status Affected:	None				
Encoding:	01	01bb	bfff	ffff	
Description:	Bit 'b' in register 'f' is set.				
Words:	1				
Cycles:	1				
Example	BSF FLAG_REG, 7				
	Before Instruction				
	FLAG_REG = 0x0A				
	After Instruction				
	FLAG_REG = 0x8A				

BTFSC		Bit Test, Skip if Clear																		
Syntax:	[<i>label</i>] BTFSC f,b																			
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$																			
Operation:	skip if (f) = 0																			
Status Affected:	None																			
Encoding:	<table border="1"><tr><td>01</td><td>10bb</td><td>bfff</td><td>ffff</td></tr></table>					01	10bb	bfff	ffff											
01	10bb	bfff	ffff																	
Description:	<p>If bit 'b' in register 'f' is '0' then the next instruction is skipped.</p> <p>If bit 'b' is '0' then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2 cycle instruction.</p>																			
Words:	1																			
Cycles:	1(2)																			
Example	<table><tr><td>HERE</td><td>BTFSC</td><td>FLAG, 1</td></tr><tr><td>FALSE</td><td>GOTO</td><td>PROCESS_CODE</td></tr><tr><td>TRUE</td><td>.</td><td></td></tr><tr><td></td><td>.</td><td></td></tr><tr><td></td><td>.</td><td></td></tr></table> <p>Before Instruction</p> <p>PC = address HERE</p> <p>After Instruction</p> <p>if FLAG<1> = 0, PC = address TRUE</p> <p>if FLAG<1>=1, PC = address FALSE</p>					HERE	BTFSC	FLAG, 1	FALSE	GOTO	PROCESS_CODE	TRUE	.			.			.	
HERE	BTFSC	FLAG, 1																		
FALSE	GOTO	PROCESS_CODE																		
TRUE	.																			
	.																			
	.																			

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CLRWDT Clear Watchdog Timer

Syntax:	[<i>label</i>] CLRWDT			
Operands:	None			
Operation:	00h → WDT 0 → WDT prescaler, 1 → \overline{TO} 1 → \overline{PD}			
Status Affected:	\overline{TO} , \overline{PD}			
Encoding:	00	0000	0110	0100
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits \overline{TO} and \overline{PD} are set.			
Words:	1			
Cycles:	1			
Example	CLRWDT			

Before Instruction
WDT counter = ?

After Instruction
WDT counter = 0x00
WDT prescaler = 0
 \overline{TO} = 1
 \overline{PD} = 1

COMF Complement f

Syntax:	[<i>label</i>] COMF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	$(\bar{f}) \rightarrow (\text{dest})$			
Status Affected:	Z			
Encoding:	00	1001	dfff	ffff
Description:	The contents of register 'f' are complemented. If 'd' is 0 the result is stored in W. If 'd' is 1 the result is stored back in register 'f'.			
Words:	1			
Cycles:	1			
Example	COMF REG1, 0			

Before Instruction
REG1 = 0x13

After Instruction
REG1 = 0x13
W = 0xEC

DECF Decrement f

Syntax:	[<i>label</i>] DECF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(f) - 1 \rightarrow (dest)			
Status Affected:	Z			
Encoding:	00	0011	dfff	ffff
Description:	Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.			
Words:	1			
Cycles:	1			
Example	DECF CNT, 1			

Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ Decrement f, Skip if 0

Syntax:	[<i>label</i>] DECFSZ f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(f) - 1 \rightarrow (dest); skip if result = 0			
Status Affected:	None			
Encoding:	00	1011	dfff	ffff
Description:	<p>The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.</p> <p>If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.</p>			
Words:	1			

Before Instruction
PC = address HERE

After Instruction
CNT = CNT - 1
if CNT = 0,
PC = address CONTINUE
if CNT ≠ 0,
PC = address HERE+1

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FIGURE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING

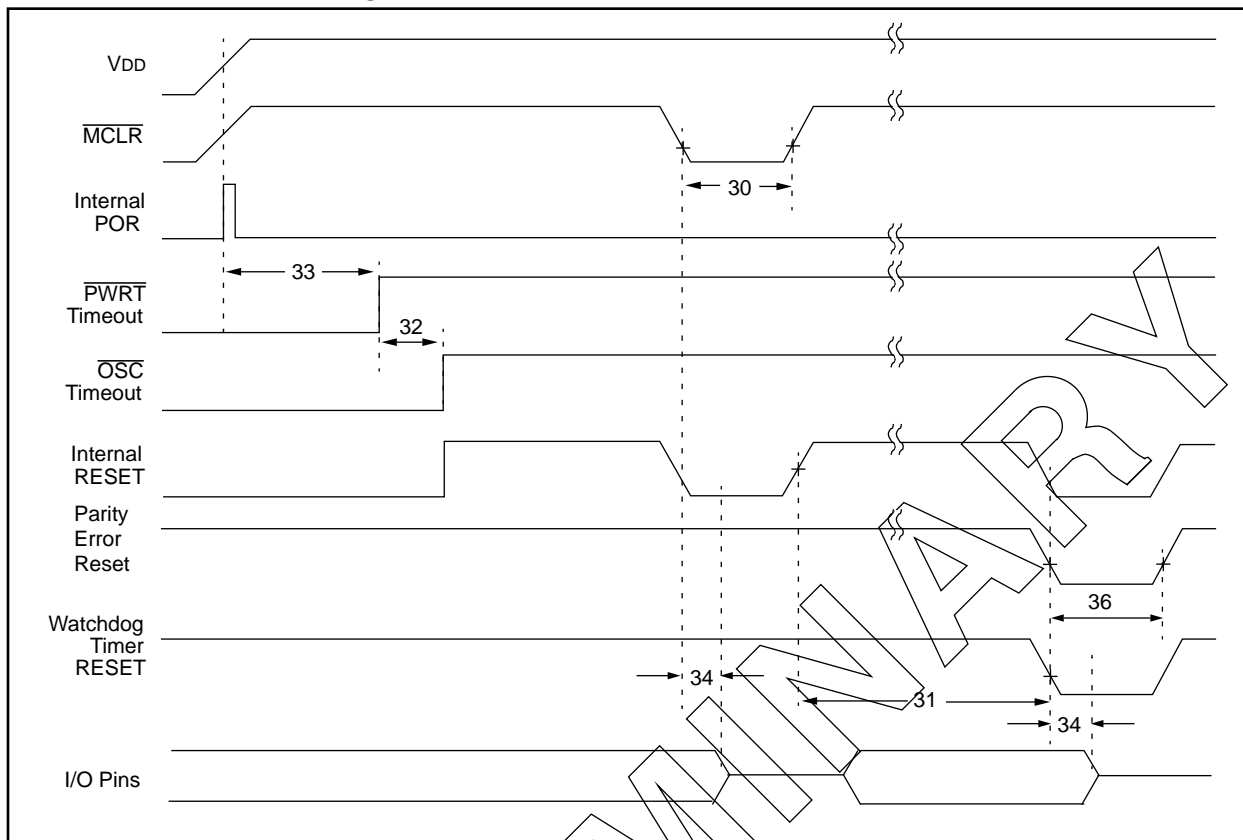


FIGURE 12-5: BROWN-OUT RESET TIMING

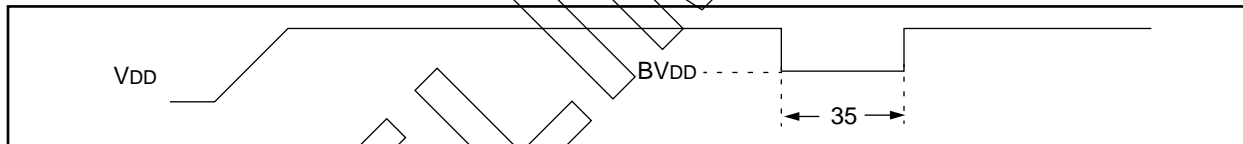


TABLE 12-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	μs	
35	TBOR	Brown-out Reset pulse width	100	—	—	μs	VDD ≤ BVDD (D005)
36	TPER	Parity Error Reset	—	TBD	—	μs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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APPENDIX C: WHAT'S NEW

New Data Sheet

APPENDIX D: WHAT'S CHANGED

New Data Sheet

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APPENDIX E: PIC16/17 MICROCONTROLLERS

E.1 PIC14000 Devices

PIC14000	Memory			Peripherals			Features		
	Clock	Maximum Frequency of Operation (MHz)	EPROM Program Memory (Kx14 words)	Data Memory (bytes)	Timer Module(s)	Serial Ports (SPI/I ² C, USART)	Slope A/D Converter (high-res) Channels	Interrupt Sources	I/O Pins
PIC14000	20	4K	192	TMR0 ADTMR	I ² C/ SMBus	14	11	22	2.7-6.0
								Yes	
								Internal Oscillator, Bandgap Reference, Temperature Sensor, Calibration Factors, Low Voltage Detector, SLEEP, HIBERNATE, Comparators with Programmable References (2)	
								Additional On-chip Features	
								In-Circuit Serial Programming	
								Voltage Range (Volts)	
								Packages	