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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	176 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc662t-04i-l

PIC16C64X & PIC16C66X

TABLE 1-1: PIC16C64X & PIC16C66X DEVICE FEATURES

	Clock			Memory			Peripherals				Features	
	Maximum Frequency of Operation (MHz)	Program Memory (bytes)	Data Memory (bytes)	Timer Module(s)	Comparator(s)	Internal Reference Voltage	Parallel Slave Port	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Brown-out Reset	Packages
PIC16C641	20	2K	128	TMR0	2	Yes	-	4	22	3.0-6.0	Yes	28-pin PDIP, SOIC, Windowed CDIP
PIC16C642	20	4K	176	TMR0	2	Yes	-	4	22	3.0-6.0	Yes	28-pin PDIP, SOIC, Windowed CDIP
PIC16C661	20	2K	128	TMR0	2	Yes	Yes	5	33	3.0-6.0	Yes	40-pin PDIP, Windowed CDIP; 44-pin PLCC, TQFP
PIC16C662	20	4K	176	TMR0	2	Yes	Yes	5	33	3.0-6.0	Yes	40-pin PDIP, Windowed CDIP; 44-pin PLCC, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.

All PIC16CXXX Family devices use serial programming with clock pin RB6 and data pin RB7.

PIC16C64X & PIC16C66X

NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C64X & PIC16C66X devices can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C64X & PIC16C66X use a Harvard architecture in which program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than an 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches, which require two cycles.

The PIC16C641 and PIC16C661 both address 2K x 14 on-chip program memory while the PIC16C642 and PIC16C662 address 4K x 14. All program memory is internal.

PIC16C64X & PIC16C66X devices can directly or indirectly address their register files or data memory. All special function registers including the program counter are mapped in the data memory. These devices have an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C64X & PIC16C66X simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16C64X & PIC16C66X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift, and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, bit in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

PIC16C64X & PIC16C66X

Name	DIP Pin #	QFP Pin #	PLCC Pin #	I/O/P Type	Buffer Type	Description
RD0/PSP0	19	38	21	I/O	ST/TTL ⁽³⁾	PORTD can be a bi-directional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD1/PSP1	20	39	22	I/O	ST/TTL ⁽³⁾	
RD2/PSP2	21	40	23	I/O	ST/TTL ⁽³⁾	
RD3/PSP3	22	41	24	I/O	ST/TTL ⁽³⁾	
RD4/PSP4	27	2	30	I/O	ST/TTL ⁽³⁾	
RD5/PSP5	28	3	31	I/O	ST/TTL ⁽³⁾	
RD6/PSP6	29	4	32	I/O	ST/TTL ⁽³⁾	
RD7/PSP7	30	5	33	I/O	ST/TTL ⁽³⁾	
RE0/ \overline{RD}	8	25	9	I/O	ST/TTL ⁽³⁾	PORTE is a bi-directional I/O port. RE0/ \overline{RD} read control for parallel slave port. RE1/ \overline{WR} write control for parallel slave port. RE2/ \overline{CS} select control for parallel slave port.
RE1/ \overline{WR}	9	26	10	I/O	ST/TTL ⁽³⁾	
RE2/ \overline{CS}	10	27	11	I/O	ST/TTL ⁽³⁾	
Vss	12,31	6,29	13,34	P	—	Ground reference for logic and I/O pins.
VDD	11,32	7,28	12,35	P	—	Positive supply for logic and I/O pins.
NC	—	12,13, 33,34	1,17 28,40	—	—	Not Connected.

Legend: O = output I/O = input/output P = power
 I = input — = not used ST = Schmitt Trigger input
 TTL = TTL input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 2: This buffer is a Schmitt Trigger input when used in serial programming mode.
 3: This buffer is a Schmitt Trigger input when configured as a general purpose I/O and a TTL input when used in the Parallel Slave Port Mode (for interfacing to a microprocessor port).

PIC16C64X & PIC16C66X

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3, and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-3.

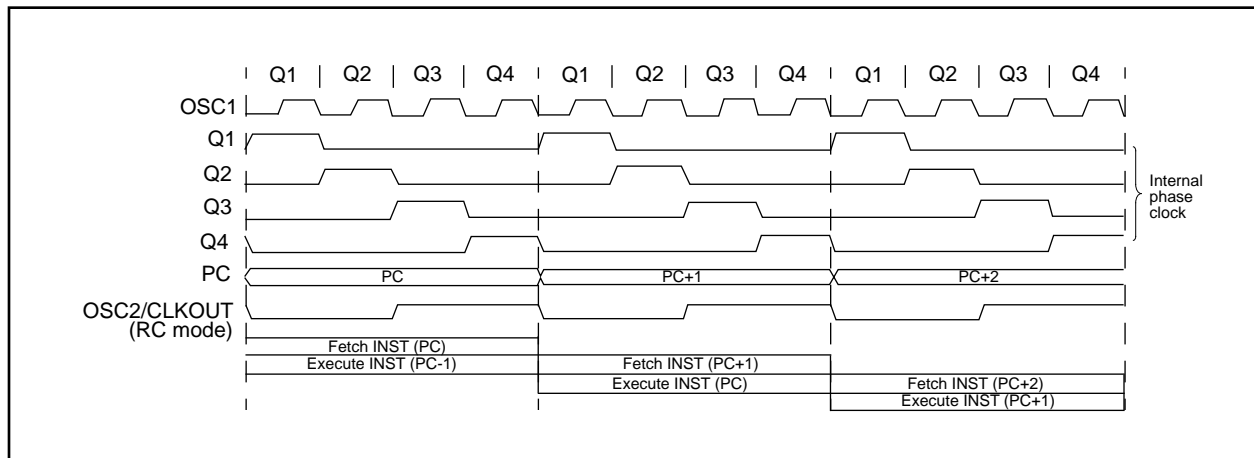
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3, and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

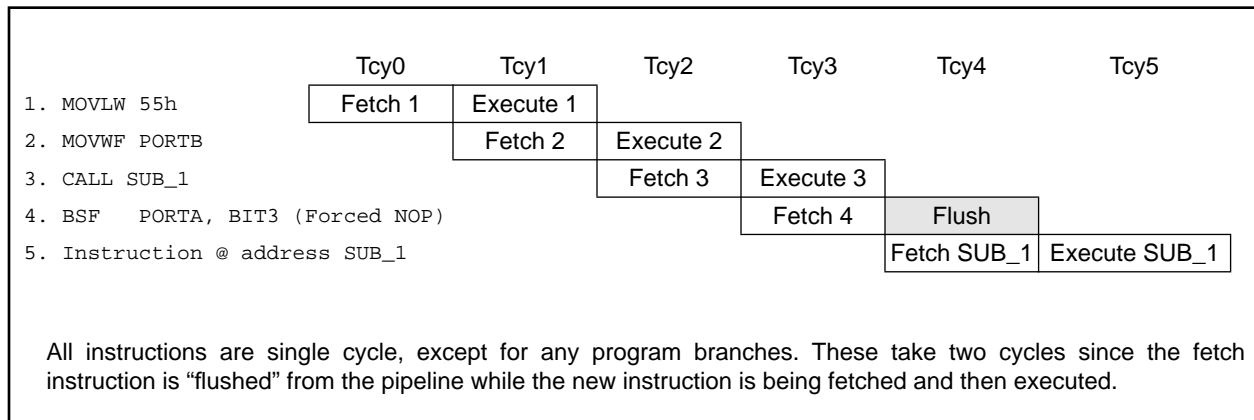
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-3: CLOCK/INSTRUCTION CYCLE



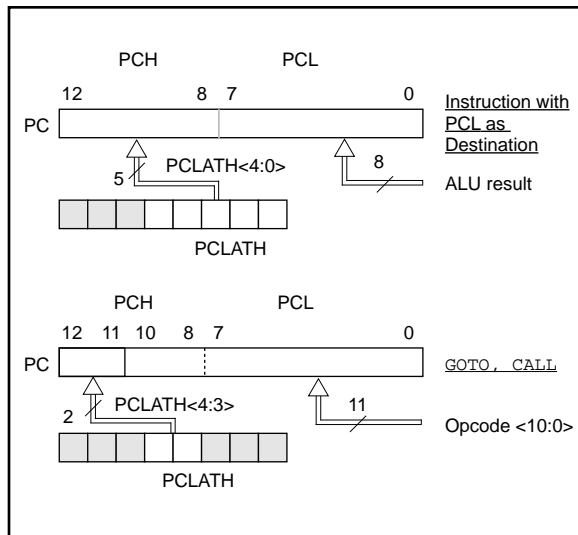
EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is readable and writable. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any reset, the PC is cleared. Figure 4-11 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 4-11: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note "Implementing a Table Read" (AN556).

4.3.2 STACK

PIC16C64X & PIC16C66X devices have an 8 level deep x 13-bit wide hardware stack (Figure 4-2). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no status bits to indicate stack overflow or stack underflow conditions.

Note 2: There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

4.4 Program Memory Paging

PIC16C642 and PIC16C662 devices have 4K of program memory, but the CALL and GOTO instructions only have an 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. To allow CALL and GOTO instructions to address the entire 4K program memory address range, there must be another bit to specify the program memory page. This paging bit comes from the PCLATH<3> bit (Figure 4-11). When doing a CALL or GOTO instruction, the user must ensure that this page select bit (PCLATH<3>) is programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<3> bit is not required for the return instructions (which POPs the address from the stack).

Note: The PIC16C64X & PIC16C66X ignore the PCLATH<4> bit, which is used for program memory pages 2 and 3 (1000h - 1FFFh). The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

5.0 I/O PORTS

The PIC16C641 and PIC16C642 have three ports, PORTA, PORTB, and PORTC. PIC16C661 and PIC16C662 devices have five ports, PORTA through PORTE. Some pins for these I/O ports are multiplexed with alternate functions for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

5.1 PORTA and TRISA Registers

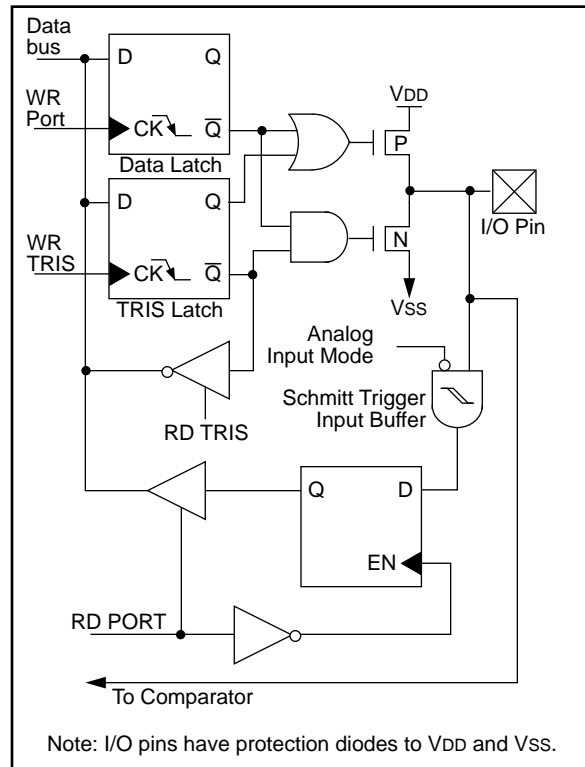
PORTA is a 6-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. Pin RA4 is multiplexed with the T0CKI clock input. All other RA port pins have Schmitt Trigger input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as input or output.

Setting a bit in the TRISA register puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISA register puts the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

The PORTA pins are multiplexed with comparator and voltage reference functions. The operation of these pins are selected by control bits in the CMCON (comparator control register) register and the VRCON (voltage reference control) register. When selected as comparator inputs, these pins will read as '0's.

FIGURE 5-1: BLOCK DIAGRAM OF RA1:RA0 PINS



Note: On reset, the TRISA register is set to all inputs. The digital inputs are disabled and the comparator inputs are forced to ground to reduce excess current consumption.

TRISA controls the direction of the RA pins, even when they are being used as comparator inputs. The user must make sure to keep the pins configured as inputs when using them as comparator inputs.

The RA2 pin will also function as the output for the voltage reference. When in this mode, the VREF pin is a very hi-impedance output. The user must set the TRISA<2> bit and use hi-impedance loads.

In one of the comparator modes defined by the CMCON register, pins RA3 and RA4 become outputs of the comparators. The TRISA<4:3> bits must be cleared to enable outputs to use this function.

EXAMPLE 5-1: INITIALIZING PORTA

```
CLRF    PORTA           ;Initialize PORTA by
                        ;clearing output latches

MOVLW   0x07            ;Turn comparators off,
MOVWF   CMCON           ;enable pins for I/O
BSF     STATUS, RP0     ;Select bank1
MOVLW   0x1F            ;Value to initialize
                        ;data direction
MOVWF   TRISA           ;Set RA<4:0> as inputs
                        ;TRISA<7:5> are clear
```


PIC16C64X & PIC16C66X

FIGURE 5-4: BLOCK DIAGRAM OF RA4 PIN

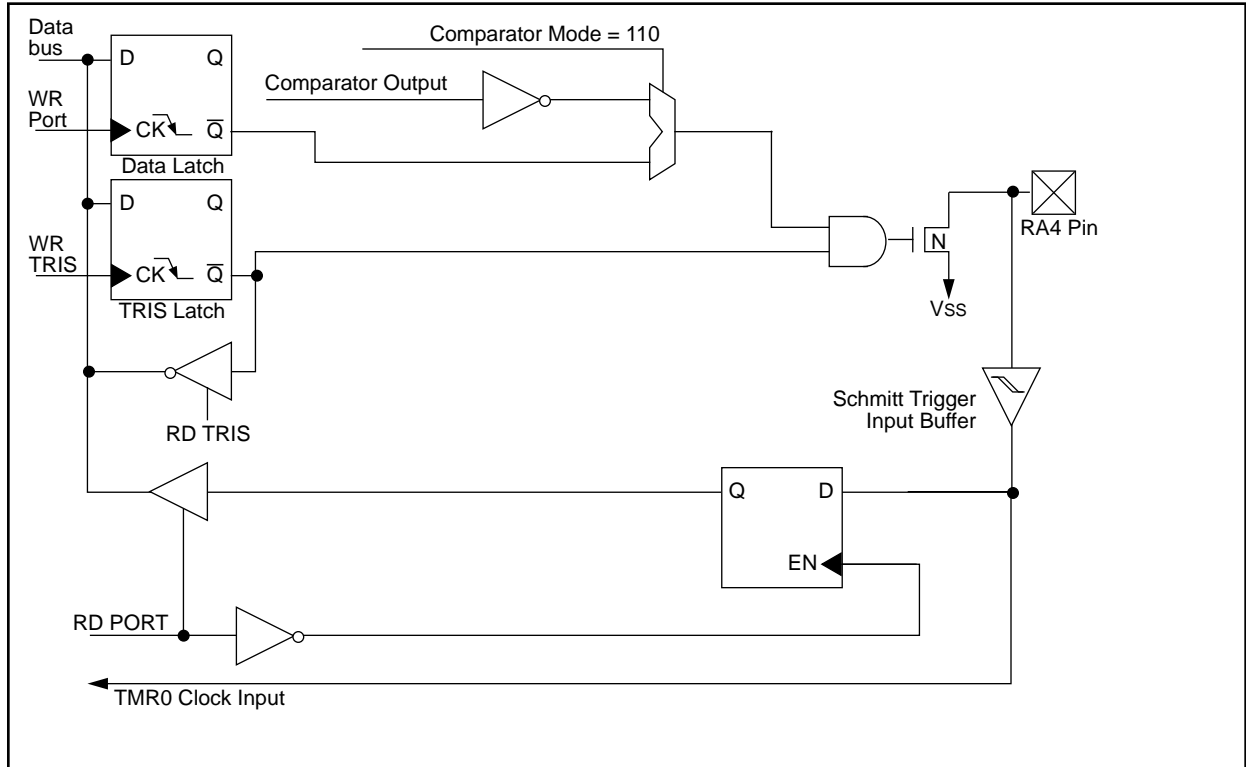


TABLE 5-1: PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function
RA0/AN0	bit0	ST	Input/output or comparator input.
RA1/AN1	bit1	ST	Input/output or comparator input.
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output.
RA3/AN3	bit3	ST	Input/output or comparator input/output.
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.
RA5	bit5	ST	Input/output.

Legend: ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx 0000	--uu 0000
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

PIC16C64X & PIC16C66X

5.3 PORTC and TRISC Registers

PORTC is an 8-bit bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC pins have Schmitt Trigger input buffers.

EXAMPLE 5-3: INITIALIZING PORTC

```
CLRF    PORTC      ; Initialize PORTC by
                  ; clearing output
                  ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                  ; initialize data
                  ; direction
MOVWF   TRISC       ; Set RC<3:0> as inputs
                  ; RC<5:4> as outputs
                  ; RC<7:6> as inputs
```

FIGURE 5-7: PORTC BLOCK DIAGRAM (IN I/O PORT MODE)

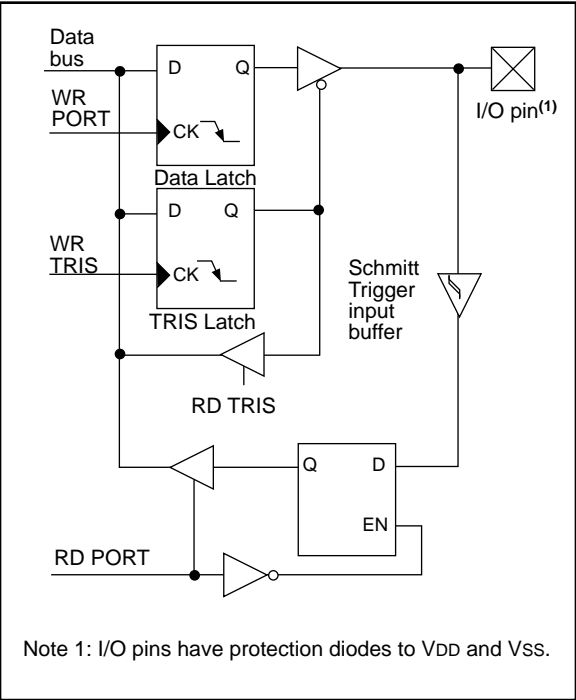


TABLE 5-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0	bit0	ST	Input/output
RC1	bit1	ST	Input/output
RC2	bit2	ST	Input/output
RC3	bit3	ST	Input/output
RC4	bit4	ST	Input/output
RC5	bit5	ST	Input/output
RC6	bit6	ST	Input/output
RC7	bit7	ST	Input/output

Legend: ST = Schmitt Trigger input

TABLE 5-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged.

PIC16C64X & PIC16C66X

5.4 PORTD and TRISD Registers (PIC16C661 and PIC16C662 only)

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 5-8: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)

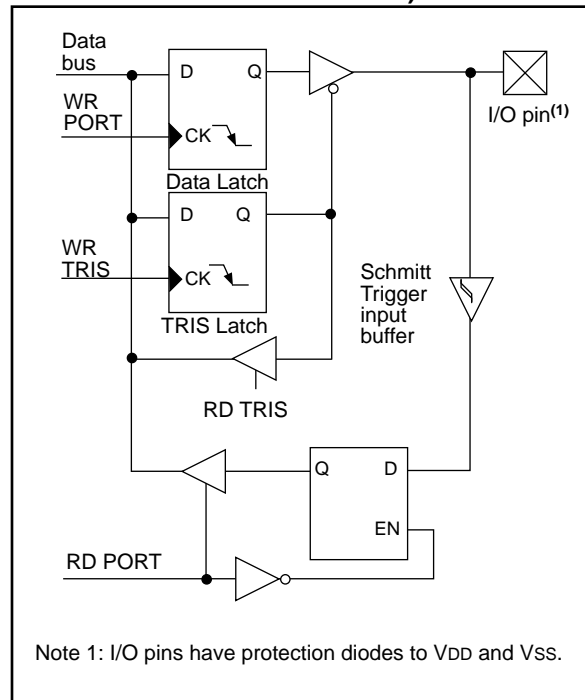


TABLE 5-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit0
RD1/PSP1	bit1	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit1
RD2/PSP2	bit2	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit2
RD3/PSP3	bit3	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit3
RD4/PSP4	bit4	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit4
RD5/PSP5	bit5	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit5
RD6/PSP6	bit6	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit6
RD7/PSP7	bit7	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit7

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port Mode.

TABLE 5-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTD.

PIC16C64X & PIC16C66X

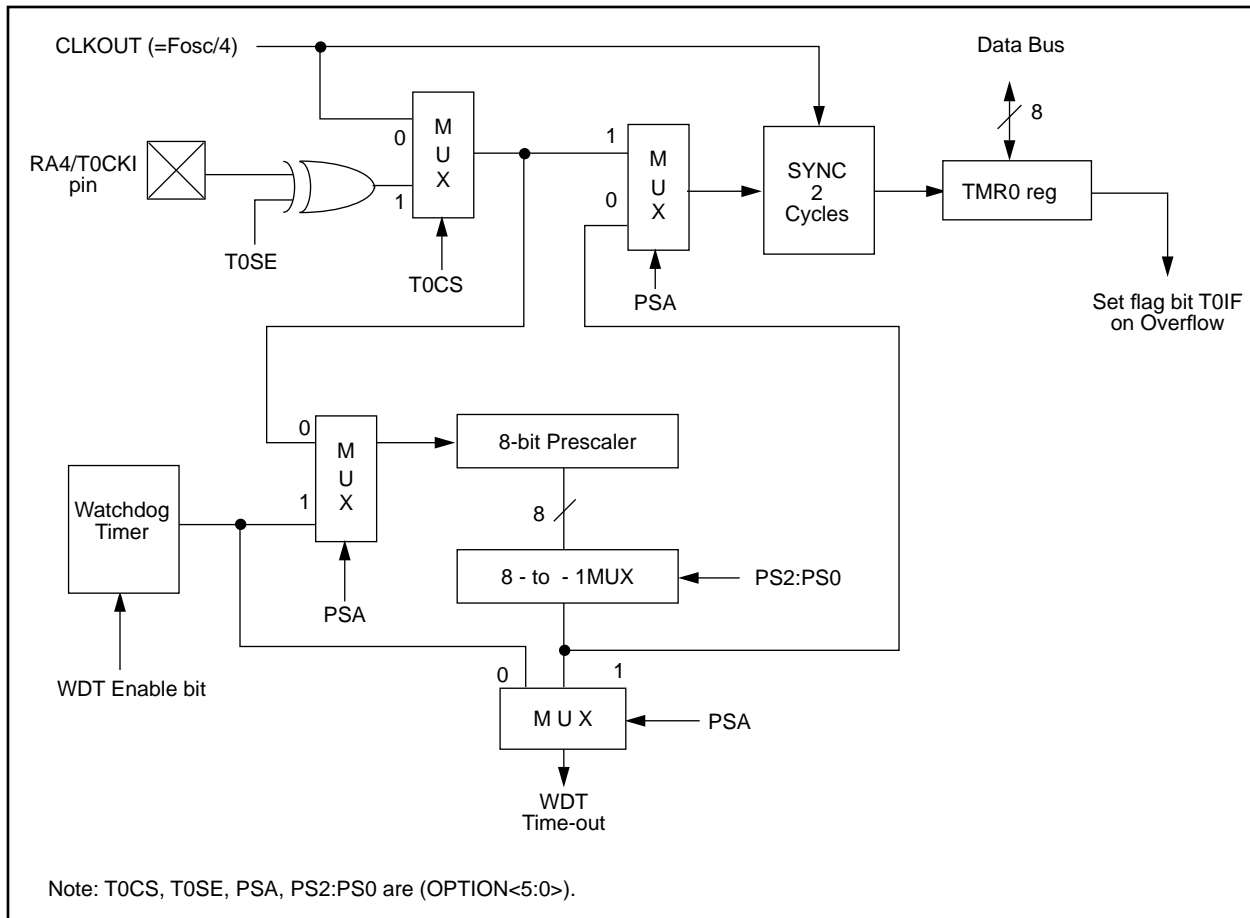
6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (Figure 6-6). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`) will clear the prescaler count. When assigned to Watchdog Timer, a `CLRWDT` instruction will clear the prescaler count along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



PIC16C64X & PIC16C66X

6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed “on the fly” during program execution.

Note: To avoid an unintended device RESET, the following instruction sequence (shown in Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This precaution must be followed even if the WDT is disabled.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF    STATUS, RP0    ;Bank 0
CLRF   TMR0           ;Clear TMR0 & Prescaler
BSF    STATUS, RP0    ;Bank 1
CLRWDT           ;Clears WDT
MOVLW  b'xxxxlxxx'    ;Select new prescale
MOVWF  OPTION_REG     ;value & WDT
BCF    STATUS, RP0    ;Bank 0
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT           ;Clear WDT and
                ;prescaler
BSF     STATUS, RP0 ;Bank 1
MOVLW   b'xxx0xxx' ;Select TMR0, new
                ;prescale value and
MOVWF   OPTION_REG ;clock source
BCF     STATUS, RP0 ;Bank 0
```

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

PIC16C64X & PIC16C66X

NOTES:

PIC16C64X & PIC16C66X

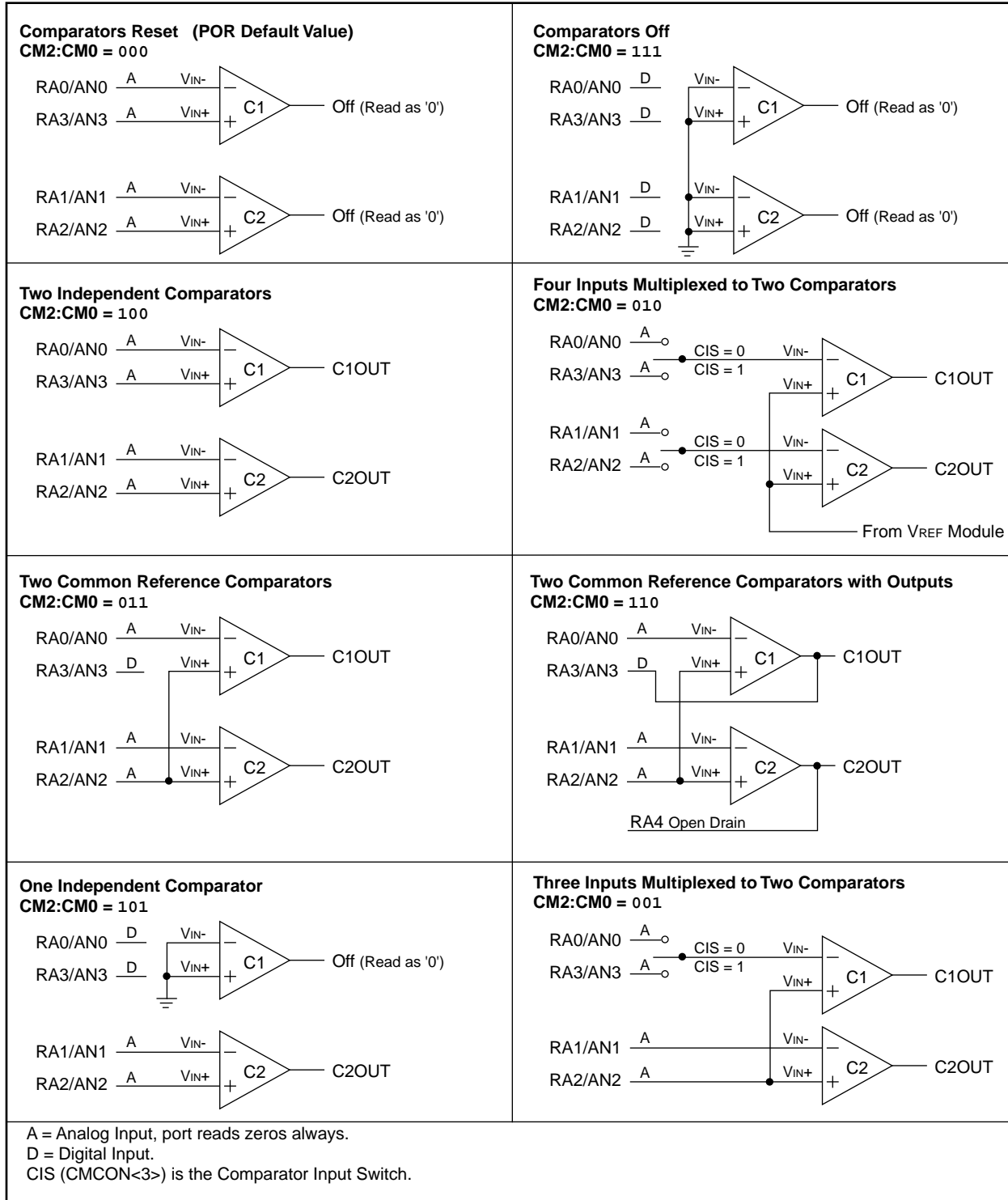
7.1 Comparator Configuration

There are eight modes of operation for the comparators. The CMCON register is used to select the mode. Figure 7-2 shows the eight possible modes. The TRISA register controls the data direction of the comparator pins for each mode. If the comparator

mode is changed, the comparator output level may not be valid for the specified mode change delay shown in Table 12-2.

Note: Comparator interrupts should be disabled during a comparator mode change otherwise a false interrupt may occur.

FIGURE 7-2: COMPARATOR I/O OPERATING MODES



PIC16C64X & PIC16C66X

TABLE 9-6: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset Brown-out Reset Parity Error Reset	MCLR Reset during: - normal operation - SLEEP or WDT Reset	Wake up from SLEEP through: - interrupt - WDT time-out
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1 ⁽²⁾
STATUS	03h	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--xx 0000	--xu 0000	--uu uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD ⁽⁴⁾	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE ⁽⁴⁾	09h	---- -xxx	---- -uuu	---- -uuu
CMCON	1Fh	00-- 0000	00-- 0000	uu-- uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
PIR1	0Ch	00-- ----	00-- ----	uu-- ---- ⁽¹⁾
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
TRISD ⁽⁴⁾	88h	1111 1111	1111 1111	uuuu uuuu
TRISE ⁽⁴⁾	89h	0000 -111	0000 -111	uuuu -uuu
PIE1	8Ch	00-- ----	00-- ----	uu-- ----
PCON	8Eh	u--- -qqq	u--- -uuu	u--- -uuu
VRCON	9Fh	000- 0000	000- 0000	uuu- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 9-5 for reset value for specific condition.

4: These registers are associated with the Parallel Slave Port and are not implemented on the PIC16C641/642.

11.0 DEVELOPMENT SUPPORT

11.1 Development Tools

The PIC16/17 microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB-SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy logic development system (fuzzyTECH®-MP)

11.2 PICMASTER: High Performance Universal In-Circuit Emulator with MPLAB IDE

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXX and PIC17CXX families. PICMASTER is supplied with the MPLAB™ Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

11.3 ICEPIC: Low-cost PIC16CXX In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT® through Pentium™ based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

11.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC16C5X, PIC16CXX, PIC17CXX and PIC14000 devices. It can also set configuration and code-protect bits in this mode.

11.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12C5XX, PIC14000, PIC16C5X, PIC16CXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket.

PIC16C64X & PIC16C66X

12.1 DC Characteristics: PIC16C641/642/661/662-04 (Commercial, Industrial, Automotive) PIC16C641/642/661/662-10 (Commercial, Industrial, Automotive) PIC16C641/642/661/662-20 (Commercial, Industrial, Automotive)

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ commercial, and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ automotive							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001 D001A	VDD	Supply Voltage	4.0 4.5	— —	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	VDR	RAM Data Retention Voltage ⁽¹⁾	1.5	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004*	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Reset Voltage	3.7 3.7	4.0 4.0	4.3 4.4	V V	BODEN configuration bit is clear Automotive
D010 D010A D013	IDD	Supply Current ⁽²⁾	— —	2.7 35	5 70	mA μA	XT and RC osc configuration FOSC = 4 MHz, VDD = 5.5V, WDT disabled ⁽⁴⁾ LP osc configuration, PIC16C64X & PIC16C66X-04 only FOSC = 32 kHz, VDD = 4.0V, WDT disabled HS osc configuration FOSC = 20 MHz, VDD = 5.5V, WDT disabled
D015 D016	ΔI_{BOR} ΔI_{COMP}	Module Differential Current ⁽⁵⁾ Brown-out Reset Current Comparator Current for each Comparator	— —	350 —	425 100	μA μA	BODEN bit is clear, VDD = 5.0V VDD = 4.0V
D017 D021	ΔI_{VREF} ΔI_{WDT}	VREF Current WDT Current	— —	— 6.0	300 20	μA μA	VDD = 4.0V VDD = 4.0V
D021	IPD	Power-down Current ⁽³⁾	— —	1.5 2.5	21 24	μA μA	VDD = 4.0V, WDT disabled Automotive

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated™, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{ext}$ (mA) with Rext in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

PIC16C64X & PIC16C66X

FIGURE 12-7: PARALLEL SLAVE PORT TIMING (PIC16C661 AND PIC16C662)

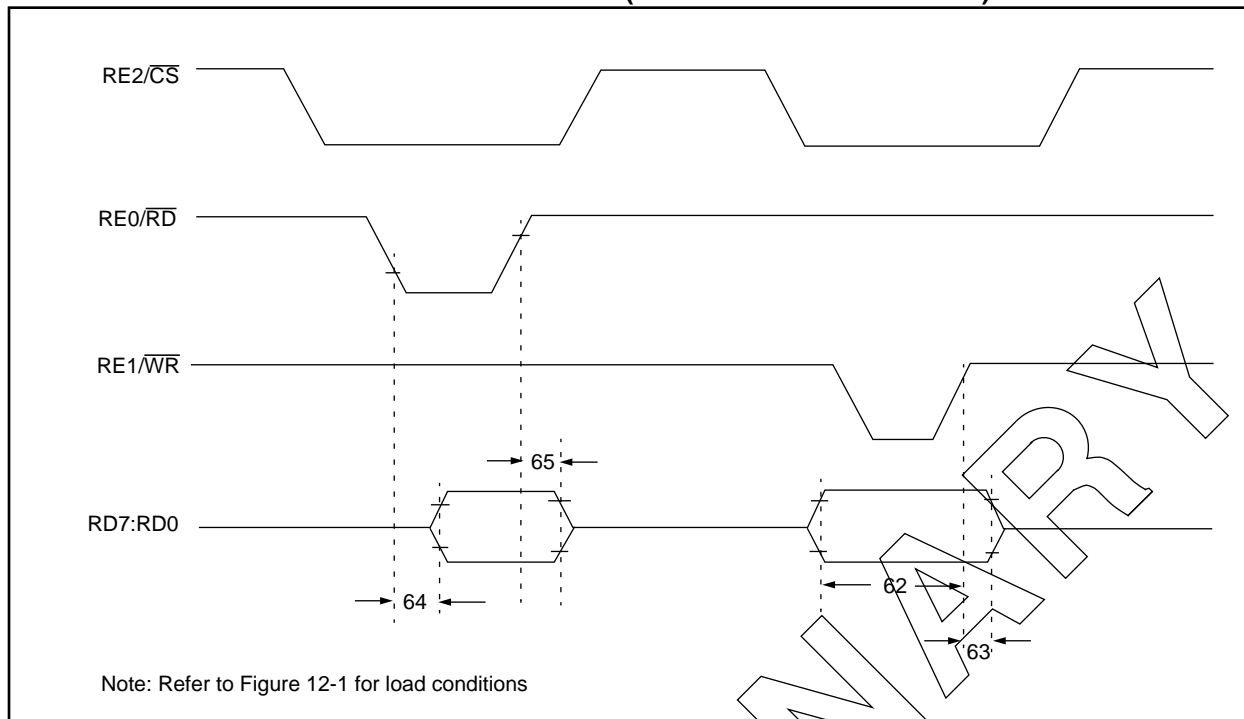


TABLE 12-8: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C661 AND PIC16C662)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before \overline{WR} ↑ or \overline{CS} ↑ (setup time)	20	—	—	ns	
63*	TwrH2dtI	\overline{WR} ↑ or \overline{CS} ↑ to data-in invalid (hold time)	20	—	—	ns	PIC16C66X
			35	—	—	ns	PIC16LC66X
64	TrdL2dtV	\overline{RD} ↓ and \overline{CS} ↓ to data-out valid	—	—	80	ns	
65	TrdH2dtI	\overline{RD} ↑ or \overline{CS} ↓ to data-out invalid	10	—	30	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

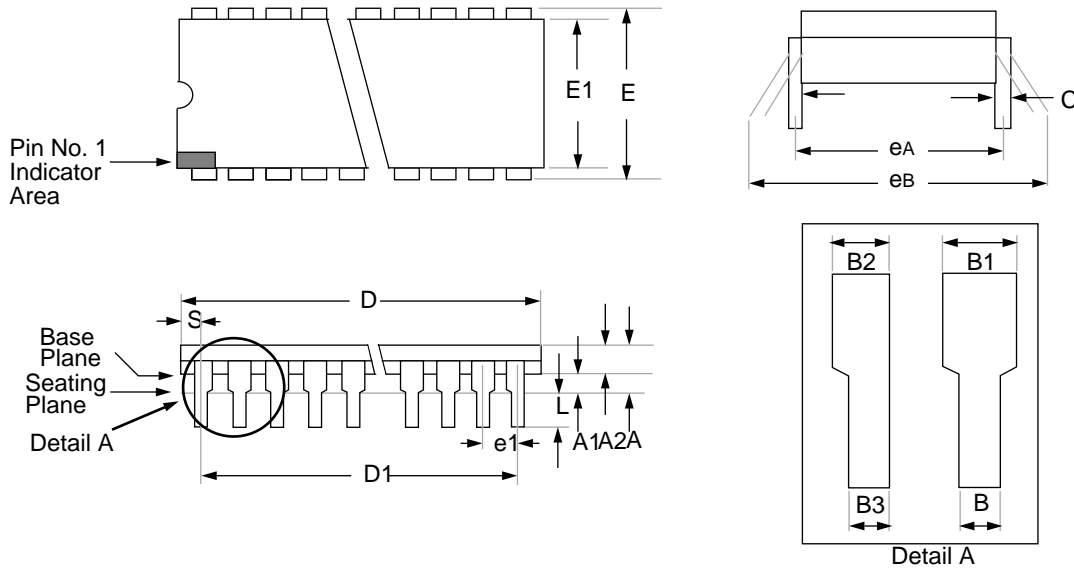
PIC16C64X & PIC16C66X

NOTES:

PIC16C64X & PIC16C66X

14.0 PACKAGING INFORMATION

Package Type: 28-Lead Skinny Plastic Dual In-Line (SP) - 300 mil



Package Group: Plastic Dual In-Line (PLA)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.632	4.572		0.143	0.180	
A1	0.381	—		0.015	—	
A2	3.175	3.556		0.125	0.140	
B	0.406	0.559		0.016	0.022	
B1	1.016	1.651	Typical	0.040	0.065	Typical
B2	0.762	1.016	4 places	0.030	0.040	4 places
B3	0.203	0.508	4 places	0.008	0.020	4 places
C	0.203	0.331	Typical	0.008	0.013	Typical
D	34.163	35.179		1.385	1.395	
D1	33.020	33.020	BSC	1.300	1.300	BSC
E	7.874	8.382		0.310	0.330	
E1	7.112	7.493		0.280	0.295	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.874	7.874	BSC	0.310	0.310	BSC
eB	8.128	9.906		0.320	0.390	
L	3.175	3.683		0.125	0.145	
S	0.584	1.220		0.023	0.048	