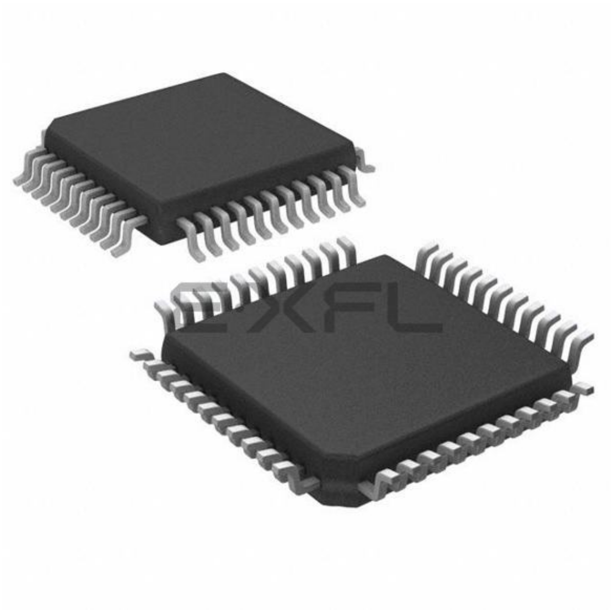


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	176 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc662t-04i-pq

Name	DIP Pin #	QFP Pin #	PLCC Pin #	I/O/P Type	Buffer Type	Description
						PORTD can be a bi-directional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	38	21	I/O	ST/TTL(3)	
RD1/PSP1	20	39	22	I/O	ST/TTL(3)	
RD2/PSP2	21	40	23	I/O	ST/TTL(3)	
RD3/PSP3	22	41	24	I/O	ST/TTL(3)	
RD4/PSP4	27	2	30	I/O	ST/TTL(3)	
RD5/PSP5	28	3	31	I/O	ST/TTL(3)	
RD6/PSP6	29	4	32	I/O	ST/TTL(3)	
RD7/PSP7	30	5	33	I/O	ST/TTL(3)	
						PORTE is a bi-directional I/O port.
RE0/$\overline{RD}$	8	25	9	I/O	ST/TTL(3)	RE0/$\overline{RD}$ read control for parallel slave port.
RE1/$\overline{WR}$	9	26	10	I/O	ST/TTL(3)	RE1/$\overline{WR}$ write control for parallel slave port.
RE2/$\overline{CS}$	10	27	11	I/O	ST/TTL(3)	RE2/$\overline{CS}$ select control for parallel slave port.
V_{SS}	12,31	6,29	13,34	P	—	Ground reference for logic and I/O pins.
V_{DD}	11,32	7,28	12,35	P	—	Positive supply for logic and I/O pins.
NC	—	12,13, 33,34	1,17 28,40	—	—	Not Connected.

Legend: O = output; I = input; TTL = TTL input; I/O = input/output; — = not used; P = power; ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured as a general purpose I/O and a TTL input when used in the Parallel Slave Port Mode (for interfacing to a microprocessor port).

4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

The PIC16C64X & PIC16C66X have a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16C641 and PIC16C661 only the first 2K x 14 (0000h - 07FFh) is physically implemented. For the PIC16C642 and PIC16C662 only the first 4K x 14 (0000h - 0FFh) is physically implemented. Accessing a location above the 2K or 4K boundary will cause a wrap-around. The reset vector is at 0000h and the interrupt vector is at 0004h (Figure 4-1 and Figure 4-2). See Section 4.4 for Program Memory paging.

FIGURE 4-1: PIC16C641/661 PROGRAM MEMORY MAP AND STACK

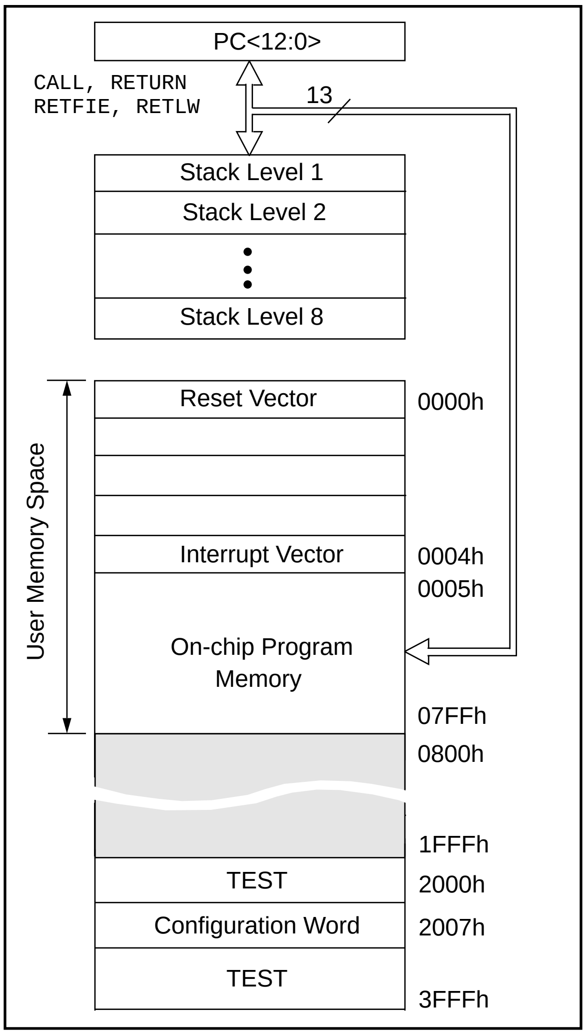
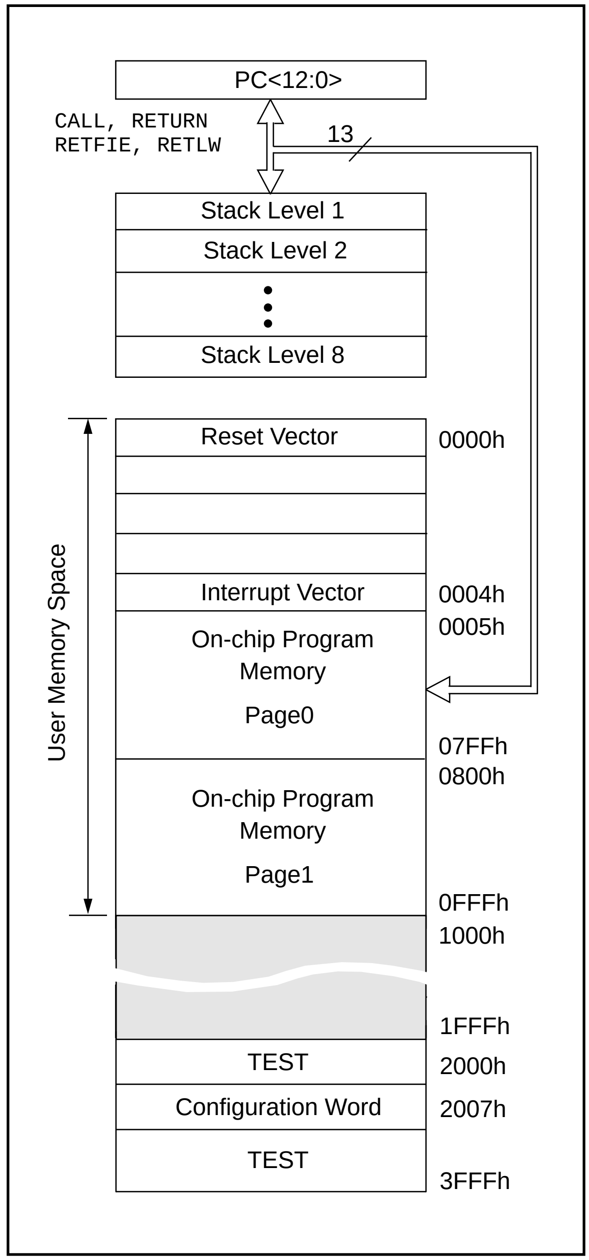


FIGURE 4-2: PIC16C642/662 PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

The data memory (Figure 4-4) is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected when bit RP0 (STATUS<5>) is cleared. Bank 1 is selected when the RP0 bit is set. The Special Function Registers are located in the first 32 locations of each Bank. Register locations A0h-EFh (Bank 1) are general purpose registers implemented as static RAM. Some special function registers are mapped in Bank 1.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 176 x 8 for the PIC16C642/662, and 128 x8 for the PIC16C641/661. Each is accessed either directly, or indirectly through the File Select Register FSR (Section 4.5).

FIGURE 4-3: PIC16C641/661 DATA MEMORY MAP

File Address	Bank 0	Bank 1	File Address
00h	INDF(1)	INDF(1)	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD(2)	TRISD(2)	88h
09h	PORTE(2)	TRISE(2)	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h–7Fh	General Purpose Register	General Purpose Register	A0h–BFh
			C0h–EFh
		Mapped in Page 0	F0h–FFh

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.
2: Not implemented on the PIC16C641.

5.5 PORTE and TRISE Register (PIC16C661 and PIC16C662 only)

PORTE has three pins RE0/$\overline{RD}$, RE1/$\overline{WR}$, and RE2/$\overline{CS}$, which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

I/O PORTE becomes control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). In this mode the input buffers are TTL.

Figure 5-9 shows the TRISE register, which also controls the parallel slave port operation.

FIGURE 5-9: TRISE REGISTER (ADDRESS 89h)

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **IBF:** Input Buffer Full Status bit
1 = A word has been received and waiting to be read by the CPU
0 = No word has been received

bit 6: **OBF**: Output Buffer Full Status bit
1 = The output buffer still holds a previously written word
0 = The output buffer has been read

bit 5: **IBOV**: Input Buffer Overflow Detect bit (in microprocessor mode)
1 = A write occurred when a previously input word has not been read (must be cleared in software)
0 = No overflow occurred

bit 4: **PSPMODE**: Parallel Slave Port Mode Select bit
1 = Parallel slave port mode
0 = General purpose I/O mode

bit 3: **Unimplemented**: Read as '0'

bit 2: **TRISE2**: Direction control bit for pin RE2/$\overline{CS}$
1 = Input
0 = Output

bit 1: **TRISE1**: Direction control bit for pin RE1/$\overline{WR}$
1 = Input
0 = Output

bit 0: **TRISE0**: Direction control bit for pin RE0/$\overline{RD}$
1 = Input
0 = Output

9.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST), Brown-out Reset (BOR), and Parity Error Reset (PER)

9.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.6V to 1.8V). To take advantage of the POR, just tie the $\overline{\text{MCLR}}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607 "*Power-up Trouble Shooting.*"

9.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) delay on power-up only, from POR or BOR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows VDD to rise to an acceptable level. A configuration bit, $\overline{\text{PWRTE}}$ can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Reset is enabled.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variations. See DC parameters for details.

9.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP, and HS modes and only on Power-on Reset or wake-up from SLEEP.

9.4.4 BROWN-OUT RESET (BOR)

PIC16C64X & PIC16C66X devices have on-chip Brown-out Reset circuitry. A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V (Parameter D005 in ES section) for greater than parameter 35 in Table 12-6, the brown-out situation will reset the chip. A reset is not guaranteed to occur if VDD falls below 4.0V for less than parameter 35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in reset an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms time delay. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 9-8 shows typical Brown-out situations.

FIGURE 9-8: BROWN-OUT SITUATIONS

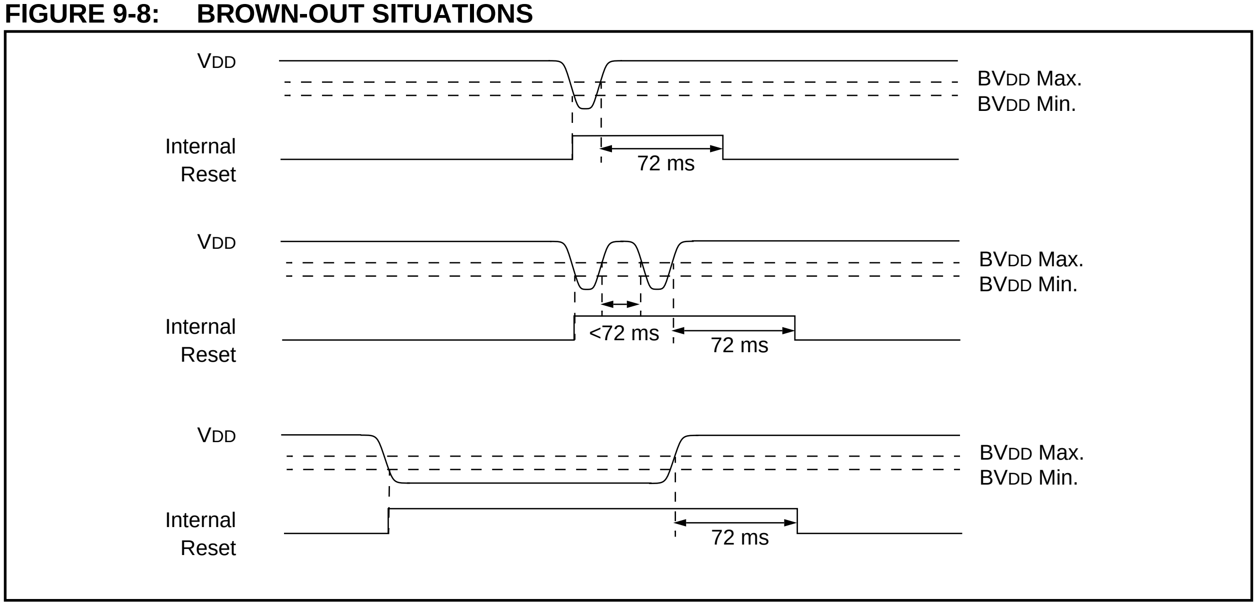


TABLE 9-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{PER}$	$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	
1	0	x	1	1	Power-on Reset
x	0	x	0	x	Illegal, $\overline{TO}$ is set on POR
x	0	x	x	0	Illegal, $\overline{PD}$ is set on POR
1	1	0	1	1	Brown-out Reset
1	1	1	0	1	WDT Reset
1	1	1	0	0	WDT Wake-up
1	1	1	u	u	$\overline{MCLR}$ reset during normal operation
1	1	1	1	0	$\overline{MCLR}$ reset during SLEEP
0	1	1	1	1	Parity Error Reset
0	0	x	x	x	Illegal, $\overline{PER}$ is set on POR
0	x	0	x	x	Illegal, $\overline{PER}$ is set on BOR

TABLE 9-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	u--- -10x
$\overline{MCLR}$ reset during normal operation	000h	000u uuuu	u--- -uuu
$\overline{MCLR}$ reset during SLEEP	000h	0001 0uuu	u--- -uuu
WDT reset	000h	0000 1uuu	u--- -uuu
WDT Wake-up	PC + 1	uuu0 0uuu	u--- -uuu
Brown-out Reset	000h	0001 1uuu	u--- -uu0
Parity Error Reset	000h	0001 1uuu	1--- -0uu
Interrupt Wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	u--- -uuu

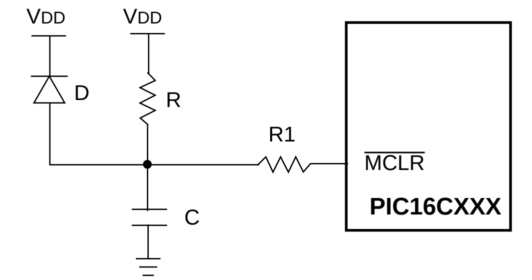
Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as ‘0’.
Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 9-6: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset Brown-out Reset Parity Error Reset	MCLR Reset during: - normal operation - SLEEP or WDT Reset	Wake up from SLEEP through: - interrupt - WDT time-out
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1(2)
STATUS	03h	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--xx 0000	--xu 0000	--uu uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD(4)	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE(4)	09h	---- -xxx	---- -uuu	---- -uuu
CMCON	1Fh	00-- 0000	00-- 0000	uu-- uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu(1)
PIR1	0Ch	00-- ----	00-- ----	uu-- ----(1)
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
TRISD(4)	88h	1111 1111	1111 1111	uuuu uuuu
TRISE(4)	89h	0000 -111	0000 -111	uuuu -uuu
PIE1	8Ch	00-- ----	00-- ----	uu-- ----
PCON	8Eh	u--- -qqq	u--- -uuu	u--- -uuu
VRCON	9Fh	000- 0000	000- 0000	uuu- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as ‘0’,q = value depends on condition.
Note 1: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).
2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3: See Table 9-5 for reset value for specific condition.
4: These registers are associated with the Parallel Slave Port and are not implemented on the PIC16C641/642.

FIGURE 9-12: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

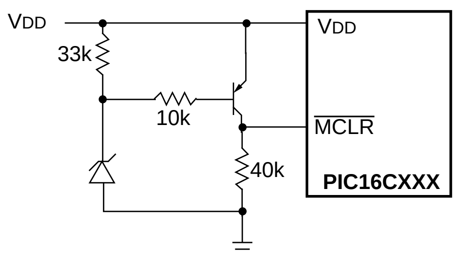


Note 1: External power-on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{\text{MCLR}}$ from external capacitor C in the event of $\overline{\text{MCLR}}$/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 9-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1

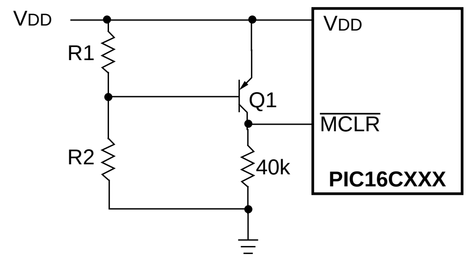


Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

2: Internal Brown-out Reset circuitry should be disabled when using this circuit.

3: Resistors should be adjusted for the characteristics of the transistor.

FIGURE 9-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7\text{ V}$$

2: Internal Brown-out Reset circuitry should be disabled when using this circuit.

3: Resistors should be adjusted for the characteristics of the transistor.

9.5.1 RB0/INT INTERRUPT

The external interrupt on the RB0/INT pin is edge triggered: either rising if bit INTEDG (OPTION<6>) is set, or falling, if bit INTEDG is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be enabled/disabled by setting/clearing enable bit INTE (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The RB0/INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.8 for details on SLEEP and Figure 9-19 for timing of wake-up from SLEEP through RB0/INT interrupt.

9.5.2 TMR0 INTERRUPT

An overflow (FFh $\rightarrow$ 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 6.0.

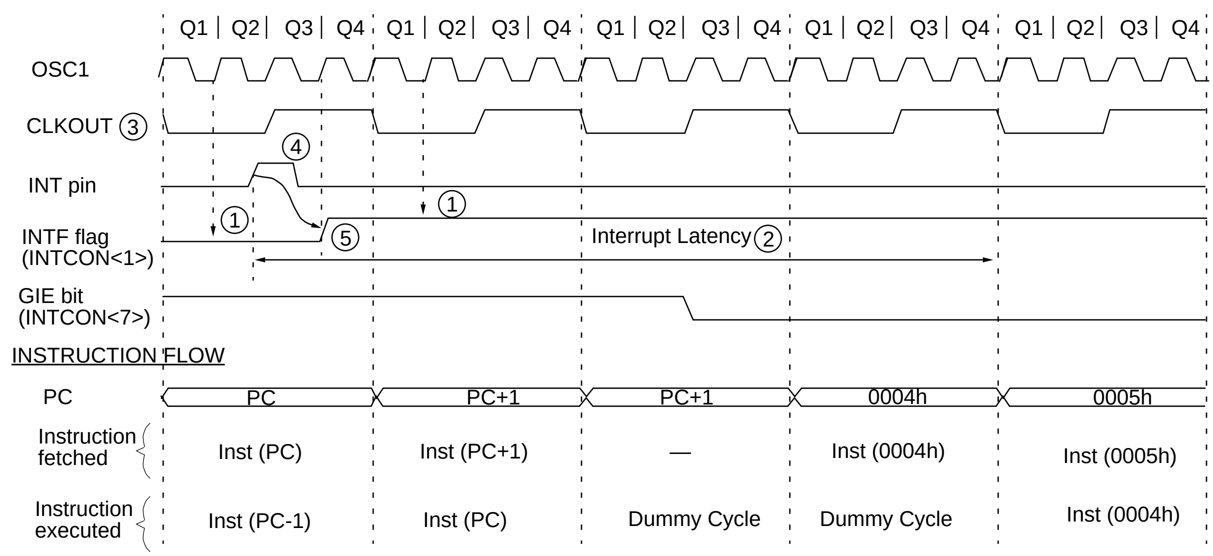
9.5.3 PORTB INTERRUPT

An input change on any bit of PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>). For operation of PORTB (Section 5.2).

9.5.4 COMPARATOR INTERRUPT

See Section 7.6 for complete description of the comparator interrupt.

FIGURE 9-16: RB0/INT PIN INTERRUPT TIMING



Note
1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.
Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

BCF — Bit Clear f

Syntax: [*label*] BCF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

01	00bb	bfff	ffff

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example

```
BCF     FLAG_REG, 7
```

Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

BSF — Bit Set f

Syntax: [*label*] BSF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 1 → (f<b>)

Status Affected: None

Encoding:

01	01bb	bfff	ffff

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example

```
BSF     FLAG_REG,   7
```

Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

BTFSC — Bit Test, Skip if Clear

Syntax: [*label*] BTFSC f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

01	10bb	bfff	ffff

Description: If bit 'b' in register 'f' is '0' then the next instruction is skipped.
If bit 'b' is '0' then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example

```
HERE    BTFSC  FLAG,1
FALSE   GOTO   PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address HERE
After Instruction
if FLAG<1> = 0,
PC = address TRUE
if FLAG<1>=1,
PC = address FALSE

NOP — No Operation

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

00	0000	0xx0	0000

Description: No operation.

Words: 1

Cycles: 1

Example

```
NOP
```

OPTION — Load Option Register

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

00	0000	0110	0010

Description: The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.

Words: 1

Cycles: 1

Example

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

RETFIE — Return from Interrupt

Syntax: [*label*] RETFIE

Operands: None

Operation: TOS → PC,
1 → GIE

Status Affected: None

Encoding:

00	0000	0000	1001

Description: Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.

Words: 1

Cycles: 2

Example

```
RETFIE
```

After Interrupt
PC = TOS
GIE = 1

RETLW — Return with Literal in W

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

11	01xx	kkkk	kkkk

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Example

```
        CALL TABLE    ;W contains table
                      ;offset value
        •             ;W now has table value
        •
        •
TABLE   ADDWF PC      ;W = offset
        RETLW k1      ;Begin table
        RETLW k2      ;
        •
        •
        •
        RETLW kn      ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k8

11.0 DEVELOPMENT SUPPORT

11.1 Development Tools

The PIC16/17 microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB-SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy logic development system (fuzzyTECH®–MP)

11.2 PICMASTER: High Performance Universal In-Circuit Emulator with MPLAB IDE

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXX and PIC17CXX families. PICMASTER is supplied with the MPLAB™ Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

11.3 ICEPIC: Low-cost PIC16CXX In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT® through Pentium™ based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

11.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable V_{DD} and V_{PP} supplies which allows it to verify programmed memory at V_{DD} min and V_{DD} max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC16C5X, PIC16CXX, PIC17CXX and PIC14000 devices. It can also set configuration and code-protect bits in this mode.

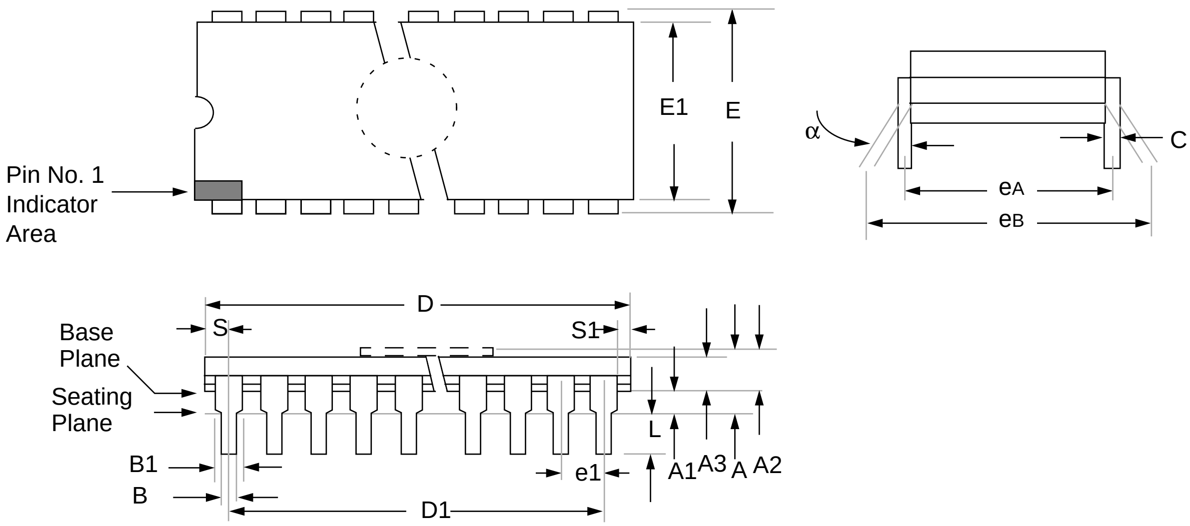
11.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12C5XX, PIC14000, PIC16C5X, PIC16CXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket.

NOTES:

Package Type: 40-Lead Ceramic Dual In-Line with Window (JW) - (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	**BSC**	1.900	1.900	**BSC**
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**BSC**	0.100	0.100	**BSC**
eA	14.986	16.002	**Typical**	0.590	0.630	**Typical**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

E.5 PIC16C7X Family of Devices

	Clock	Memory		Peripherals							Features			
	Maximum Frequency of Operation (MHz)	EPROM Program Memory (x14 words)	Data Memory (bytes)	Timer Module(s)	Capture/Compare/PWM Module(s)	Serial Port(s) (SPI/I^{2}C, USART)	Parallel Slave Port	A/D Converter (8-bit) Channels	Interrupt Sources	I/O Pins	Voltage Range (Volts)	In-Circuit Serial Programming	Brown-out Reset	Packages
PIC16C710	20	512	36	TMR0	—	—	—	4	4	13	2.5-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C71	20	1K	36	TMR0	—	—	—	4	4	13	2.5-6.0	Yes	—	18-pin DIP, SOIC
PIC16C711	20	1K	68	TMR0	—	—	—	4	4	13	2.5-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C72	20	2K	128	TMR0, TMR1, TMR2	1	SPI/I^{2}C	—	5	8	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC, SSOP
PIC16C73	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I^{2}C, USART	—	5	11	22	2.5-6.0	Yes	—	28-pin SDIP, SOIC
PIC16C73A	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I^{2}C, USART	—	5	11	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC
PIC16C74	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I^{2}C, USART	Yes	8	12	33	2.5-6.0	Yes	—	40-pin DIP; 44-pin PLCC, MQFP
PIC16C74A	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I^{2}C, USART	Yes	8	12	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC16C7X Family devices use serial programming with clock pin RB6 and data pin RB7.

E.6 PIC16C8X Family of Devices

	Clock	Memory					Peripherals			Features	
	Maximum Frequency of Operation (MHz)	Program Memory: Flash	Program Memory: EEPROM	Program Memory: ROM	Data Memory (bytes)	Data EEPROM (bytes)	Timer Module(s)	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Packages
PIC16C84	10	—	1K	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16F84[(1)]	10	1K	—	—	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16CR84[(1)]	10	—	—	1K	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16F83[(1)]	10	512	—	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16CR83[(1)]	10	—	—	512	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC

All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.

All PIC16C8X family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

E.7 PIC16C9XX Family Of Devices

	Clock	Memory		Peripherals						Features						
	Maximum Frequency of Operation (MHz)	EPROM Program Memory	Data Memory (bytes)	Timer Module(s)	Capture/Compare/PWM Module(s)	Serial Port(s) (SPI/I^2C, USART)	Parallel Slave Port	A/D Converter (8-bit) Channels	LCD Module	Interrupt Sources	I/O Pins	Input Pins	Voltage Range (Volts)	In-Circuit Serial Programming	Brown-out Reset	Packages
PIC16C923	8	4K	176	TMR0, TMR1, TMR2	1	SPI/I^2C	—	—	4 Com 32 Seg	8	25	27	3.0-6.0	Yes	—	64-pin SDIP[1], TQFP, 68-pin PLCC, DIE
PIC16C924	8	4K	176	TMR0, TMR1, TMR2	1	SPI/I^2C	—	5	4 Com 32 Seg	9	25	27	3.0-6.0	Yes	—	64-pin SDIP[1], TQFP, 68-pin PLCC, DIE

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
All PIC16CXX Family devices use serial programming with clock pin RB6 and data pin RB7.
Note 1: Please contact your local Microchip representative for availability of this package.

INDEX

NOTES:

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.