What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	100K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205zct6tr

3.4 Embedded Flash memory

The STM32F20x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbyte available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 3.6 Embedded SRAM

All STM32F20x products embed:

- Up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states
- 4 Kbytes of backup SRAM.

    The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. Multi-AHB matrix

ai15963c
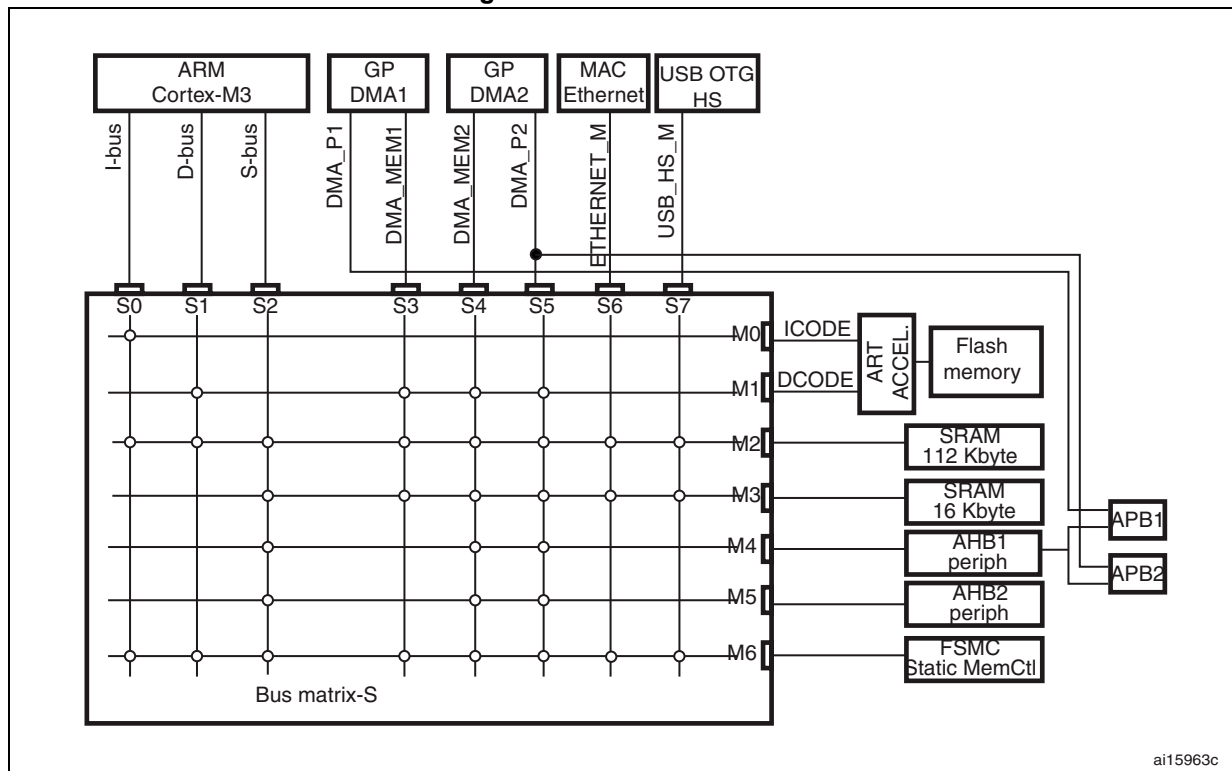
3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.26 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F207xx devices.

The STM32F207xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F207xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F207xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F207xx.

The STM32F207xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F20x and STM32F21x reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.27 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one

3.30 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 kHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

3.31 Digital camera interface (DCMI)

The camera interface is not available in STM32F205xx devices.

STM32F207xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain up to 27 Mbyte/s at 27 MHz or 48 Mbyte/s at 48 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw Bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.32 True random number generator (RNG)

All STM32F2xxx products embed a true RNG that delivers 32-bit random numbers produced by an integrated analog circuit.

3.33 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

To provide fast I/O handling, the GPIOs are on the fast AHB1 bus with a clock up to 120 MHz that leads to a maximum I/O toggling speed of 60 MHz.

3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.38 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F20x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
54	C7	83	116	144	D12	PD2	I/O	FT	-	TIM3_ETR,UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
-	-	84	117	145	D11	PD3	I/O	FT	-	FSMC_CLK,USART2_CTS, EVENTOUT	-
-	-	85	118	146	D10	PD4	I/O	FT	-	FSMC_NOE, USART2_RTS, EVENTOUT	-
-	-	86	119	147	C11	PD5	I/O	FT	-	FSMC_NWE,USART2_TX, EVENTOUT	-
-	-	-	120	148	D8	V_{SS}	S	-	-	-	-
-	-	-	121	149	C8	V_{DD}	S	-	-	-	-
-	-	87	122	150	B11	PD6	I/O	FT	-	FSMC_NWAIT, USART2_RX, EVENTOUT	-
-	-	88	123	151	A11	PD7	I/O	FT	-	USART2_CK,FSMC_NE1, FSMC_NCE2, EVENTOUT	-
-	-	-	124	152	C10	PG9	I/O	FT	-	USART6_RX, FSMC_NE2,FSMC_NCE3, EVENTOUT	-
-	-	-	125	153	B10	PG10	I/O	FT	-	FSMC_NCE4_1, FSMC_NE3, EVENTOUT	-
-	-	-	126	154	B9	PG11	I/O	FT	-	FSMC_NCE4_2, ETH_MII_TX_EN , ETH _RMII_TX_EN, EVENTOUT	-
-	-	-	127	155	B8	PG12	I/O	FT	-	FSMC_NE4, USART6_RTS, EVENTOUT	-
-	-	-	128	156	A8	PG13	I/O	FT	-	FSMC_A24, USART6_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EVENTOUT	-
-	-	-	129	157	A7	PG14	I/O	FT	-	FSMC_A25, USART6_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EVENTOUT	-
-	-	-	130	158	D7	V_{SS}	S	-	-	-	-

Table 10. Alternate function mapping (continued)

Port		AF0 SYS	AF1 TIM1/2	AF2 TIM3/4/5	AF3 TIM8/9/10/11	AF4 I2C1/I2C2/I2C3	AF5 SPI1/SPI2/I2S2	AF6 SPI3/I2S3	AF7 USART1/2/3	AF8 UART4/5/USART6	AF9 CAN1/CAN2/TIM12/13/14	AF10 OTG_FS/OTG_HS	AF11 ETH	AF12 FSMC/SDIO/OTG_HS	AF13 DCMI	AF014	AF15
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL		-	-	-	-	-	-	FSMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FSMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A5	-	-	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	-	-	-	-	-	-	-	FSMC_NIORD	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	-	-	-	-	-	-	-	FSMC_NREG	-	-	EVENTOUT
	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	-	-	FSMC_NIOWR	-	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	FSMC_CD	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INTR	-	-	EVENTOUT
	PF11	-	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A9	-	-	EVENTOUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A10	-	-	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A12	-	-	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A13	-	-	EVENTOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A14	-	-	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A15	-	-	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INT2	-	-	EVENTOUT
	PG7	-	-	-	-	-	-	-	-	USART6_CK	-	-	-	FSMC_INT3	-	-	EVENTOUT
	PG8	-	-	-	-	-	-	-	-	USART6_RTS	-	-	ETH _PPS_OUT	-	-	-	EVENTOUT
	PG9	-	-	-	-	-	-	-	-	USART6_RX	-	-	-	FSMC_NE2/ FSMC_NCE3	-	-	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NCE4_1/ FSMC_NE3	-	-	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_TX_EN ETH _RMII_TX_EN	FSMC_NCE4_2	-	-	EVENTOUT
	PG12	-	-	-	-	-	-	-	-	USART6_RTS	-	-	-	FSMC_NE4	-	-	EVENTOUT
	PG13	-	-	-	-	-	-	-	-	UART6_CTS	-	-	ETH _MII_TXD0 ETH _RMII_TXD0	FSMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	-	-	-	-	USART6_TX	-	-	ETH _MII_TXD1 ETH _RMII_TXD1	FSMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	-	DCMI_D13	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.8 V $\leq V_{DD} \leq$ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 17*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 18*.

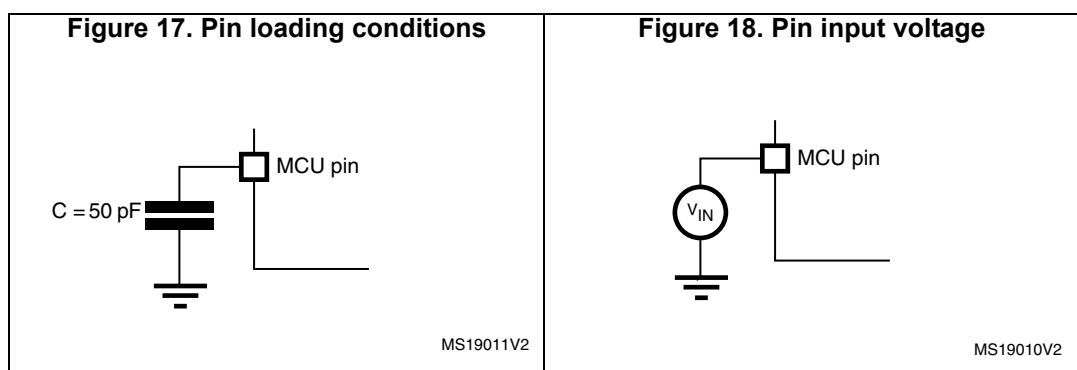| Figure 17. Pin loading conditions	Figure 18. Pin input voltage

MS19011V2

MS19010V2

Table 15. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency ($f_{Flashmax}$)	Number of wait states at maximum CPU frequency (f_{CPUmax}= 120 MHz)[1]	I/O operation	FSMC_CLK frequency for synchronous accesses	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V[2]	Conversion time up to 1 Msps	16 MHz with no Flash memory wait state	7[3]	– Degraded speed performance – No I/O compensation	Up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1 Msps	18 MHz with no Flash memory wait state	6[3]	– Degraded speed performance – No I/O compensation	Up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2 Msps	24 MHz with no Flash memory wait state	4[3]	– Degraded speed performance – I/O compensation works	Up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V[4]	Conversion time up to 2 Msps	30 MHz with no Flash memory wait state	3[3]	– Full-speed operation – I/O compensation works	– Up to 60 MHz when V_{DD} = 3.0 to 3.6 V – Up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 21*).

2. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.

4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

**Figure 21. Number of wait states versus f$_{CPU}$ and V$_{DD}$ range**
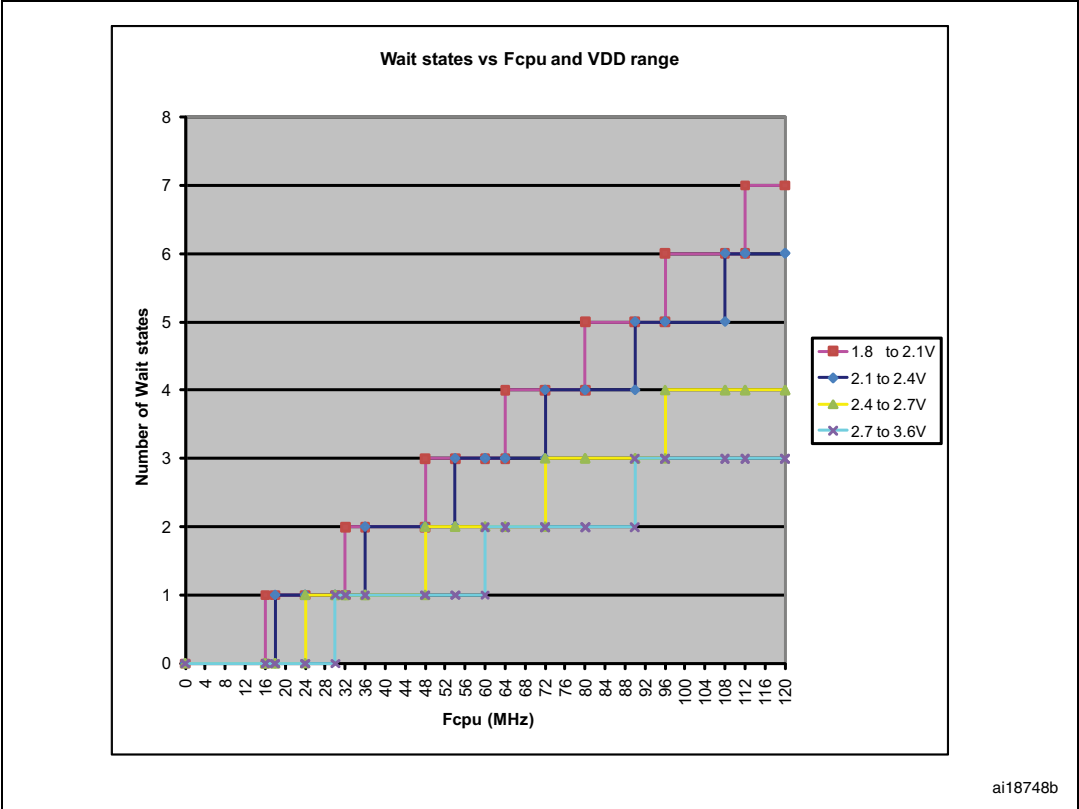
1. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range and IRROFF is set to V$_{DD}$.

6.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor to the VCAP1/VCAP2 pins. C$_{EXT}$ is specified in *Table 16*.

Figure 22. External capacitor C$_{EXT}$
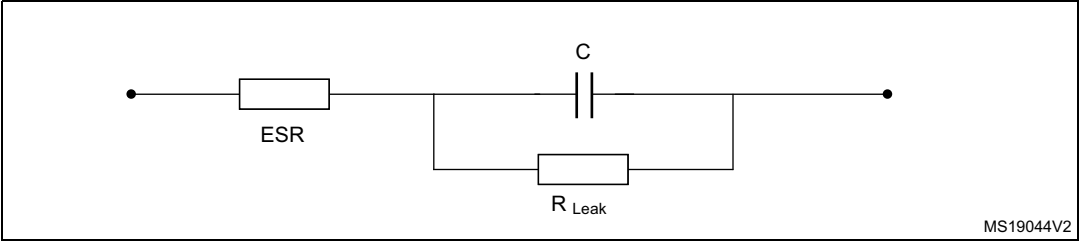
1. Legend: ESR is the equivalent series resistance.

Table 16. VCAP1/VCAP2 operating conditions[1]

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V$_{CAP}$ capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

Table 34. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter[3]	Cycle-to-cycle jitter	System clock 120 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
$I_{DD(PLL)}$[4]	PLL power consumption on VDD	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$[4]	PLL power consumption on VDDA	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.

2. Guaranteed by design, not tested in production.

3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.

4. Guaranteed by characterization results, not tested in production.

Table 35. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock[1]	-	0.95[2]	1	2.10[2]	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock	-	-	-	216	MHz
f_{VCO_OUT}	PLLI2S VCO output	-	192	-	432	MHz
t_{LOCK}	PLLI2S lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 42: EMI characteristics*). It is available only on the main PLL.

Table 36. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max[1]	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	2^{15}-1	-

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126 md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.0002\%(peak)$$

Table 39. Flash memory programming with V$_{PP}$

Symbol	Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
t$_{prog}$	Double word programming	T$_A$ = 0 to +40 °C V$_{DD}$ = 3.3 V V$_{PP}$ = 8.5 V	-	16	100[2]	µs
t$_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
t$_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
t$_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t$_{ME}$	Mass erase time		-	6.9	-	s
V$_{prog}$	Programming voltage	-	2.7	-	3.6	V
V$_{PP}$	V$_{PP}$ voltage range	-	7	-	9	V
I$_{PP}$	Minimum current sunk on the V$_{PP}$ pin	-	10	-	-	mA
t$_{VPP}$[3]	Cumulative time during which V$_{PP}$ is applied	-	-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V$_{PP}$ should only be connected during programming/erasing.

Table 40. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value Min[1]	Unit
N$_{END}$	Endurance	T$_A$ = –40 to +85 °C (6 suffix versions) T$_A$ = –40 to +105 °C (7 suffix versions)	10	kcycles
t$_{RET}$	Data retention	1 kcycle[2] at T$_A$ = 85 °C	30	Years
		1 kcycle[2] at T$_A$ = 105 °C	10	
		10 kcycles[2] at T$_A$ = 55 °C	20	

1. Guaranteed by characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V$_{DD}$ and V$_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 14: General operating conditions*.

All I/Os are CMOS and TTL compliant.

Table 46. I/O static characteristics

| Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa and NRST I/O input low level voltage	$1.7\ V \leq V_{DD} \leq 3.6\ V$	-	-	$0.35V_{DD}-0.04^{(1)}$	V
					$0.3V_{DD}^{(2)}$	
	BOOT0 I/O input low level voltage	$1.75\ V \leq V_{DD} \leq 3.6\ V$, $-40\ °C \leq T_A \leq 105\ °C$	-	-	$0.1V_{DD}+0.1^{(1)}$	
		$1.7\ V \leq V_{DD} \leq 3.6\ V$, $0\ °C \leq T_A \leq 105\ °C$	-	-		
V_{IH}	FT, TTa and NRST I/O input high level voltage[5]	$1.7\ V \leq V_{DD} \leq 3.6\ V$	$0.45V_{DD}+0.3^{(1)}$	-	-	V
			$0.7V_{DD}^{(2)}$			
	BOOT0 I/O input high level voltage	$1.75\ V \leq V_{DD} \leq 3.6\ V$, $-40\ °C \leq T_A \leq 105\ °C$	$0.17V_{DD}+0.7^{(1)}$	-	-	
		$1.7\ V \leq V_{DD} \leq 3.6\ V$, $0\ °C \leq T_A \leq 105\ °C$		-	-	
V_{HYS}	FT, TTa and NRST I/O input hysteresis	$1.7\ V \leq V_{DD} \leq 3.6\ V$	$0.45V_{DD}+0.3^{(1)}$	-	-	V
	BOOT0 I/O input hysteresis	$1.75\ V \leq V_{DD} \leq 3.6\ V$, $-40\ °C \leq T_A \leq 105\ °C$	$10\%V_{DDIO}^{(1)(3)}$	-	-	
		$1.7\ V \leq V_{DD} \leq 3.6\ V$, $0\ °C \leq T_A \leq 105\ °C$	$100^{(1)}$	-	-	
I_{lkg}	I/O input leakage current [4]	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	μA
	I/O FT input leakage current [5]	$V_{IN} = 5\ V$	-	-	3	

Figure 55. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})
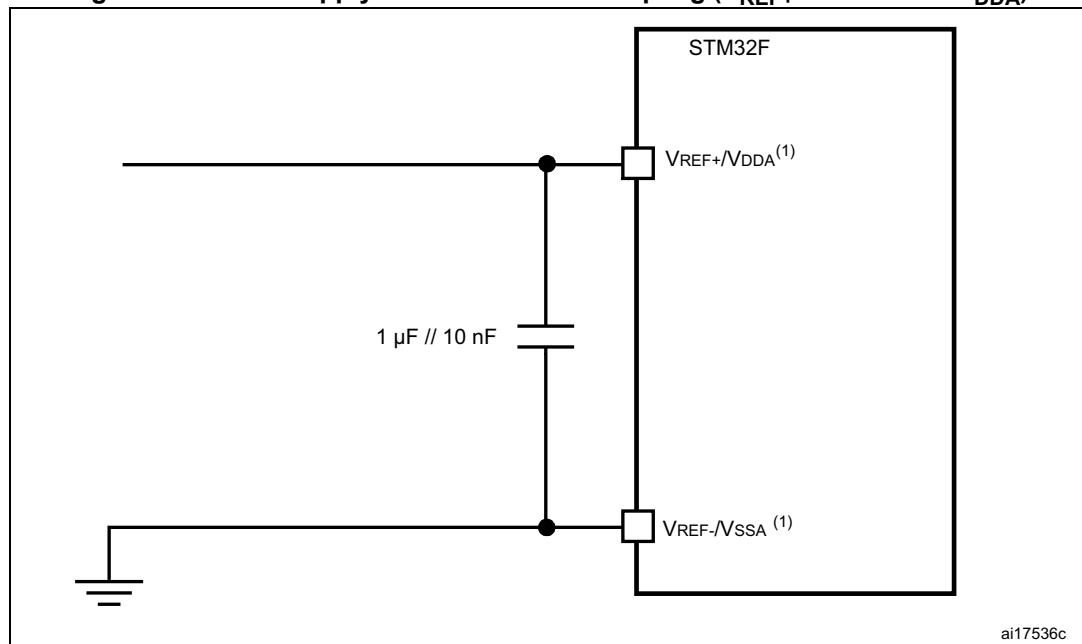
1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.21 DAC electrical characteristics

Table 68. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.8[1]	-	3.6	V	-
V_{REF+}	Reference supply voltage	1.8[1]	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}[2]	Resistive load with buffer ON	5	-	-	kΩ	-
R_O[2]	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}[2]	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min[2]	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.8 V
DAC_OUT max[2]	Higher DAC_OUT voltage with buffer ON	-	-	$V_{DDA} - 0.2$	V	

Figure 57. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms
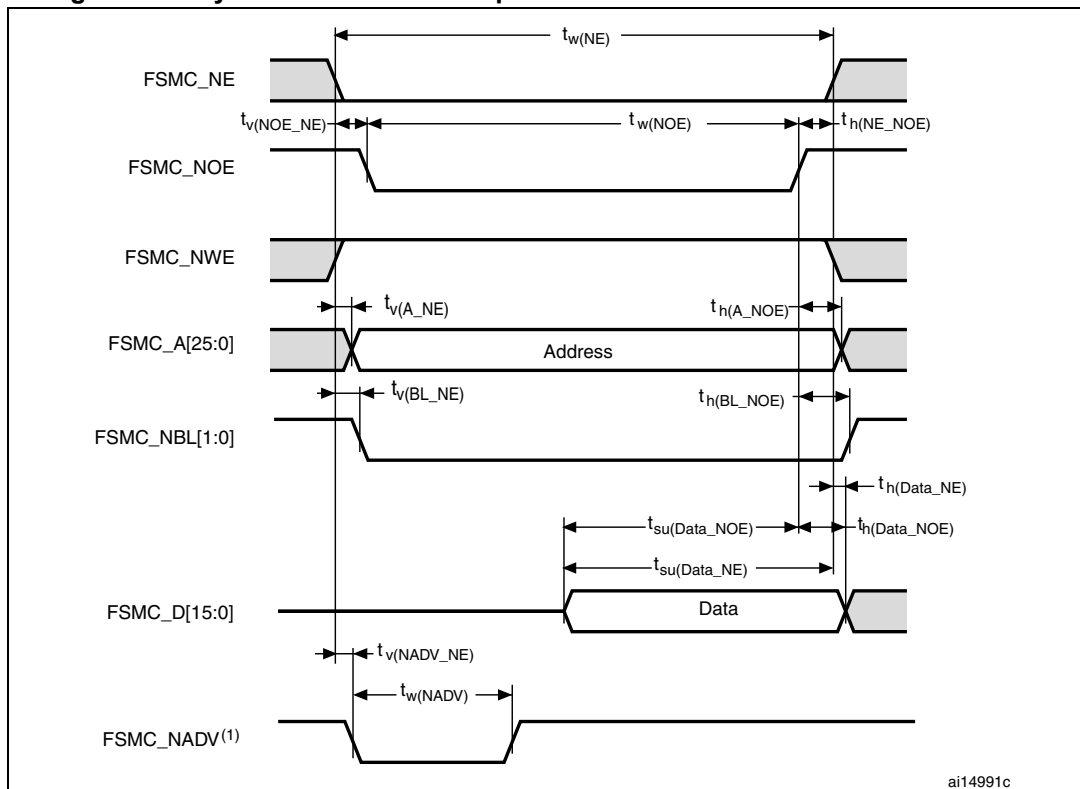
1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	2.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$2T_{HCLK} - 1$	$2T_{HCLK} + 0.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	4	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$T_{HCLK} + 0.5$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$T_{HCLK} + 2.5$	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	2.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK} - 0.5$	ns

1. C_L = 30 pF.

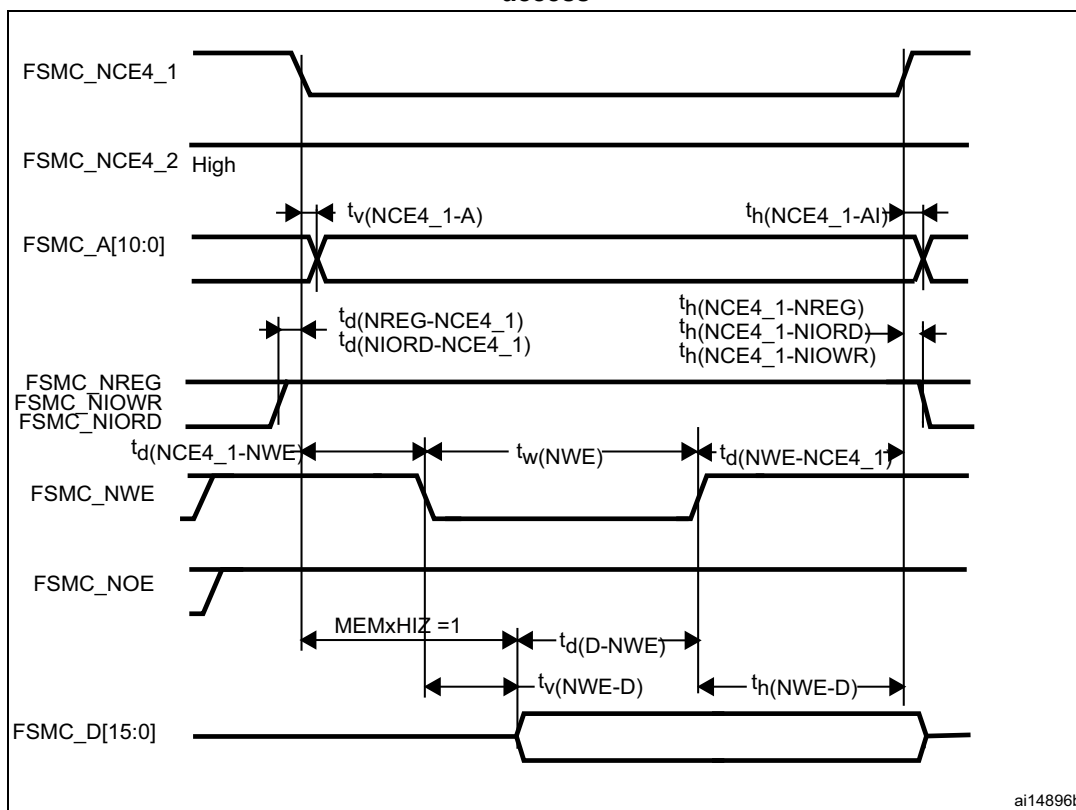2. Guaranteed by characterization results, not tested in production.

Figure 65. PC Card/CompactFlash controller waveforms for common memory read access
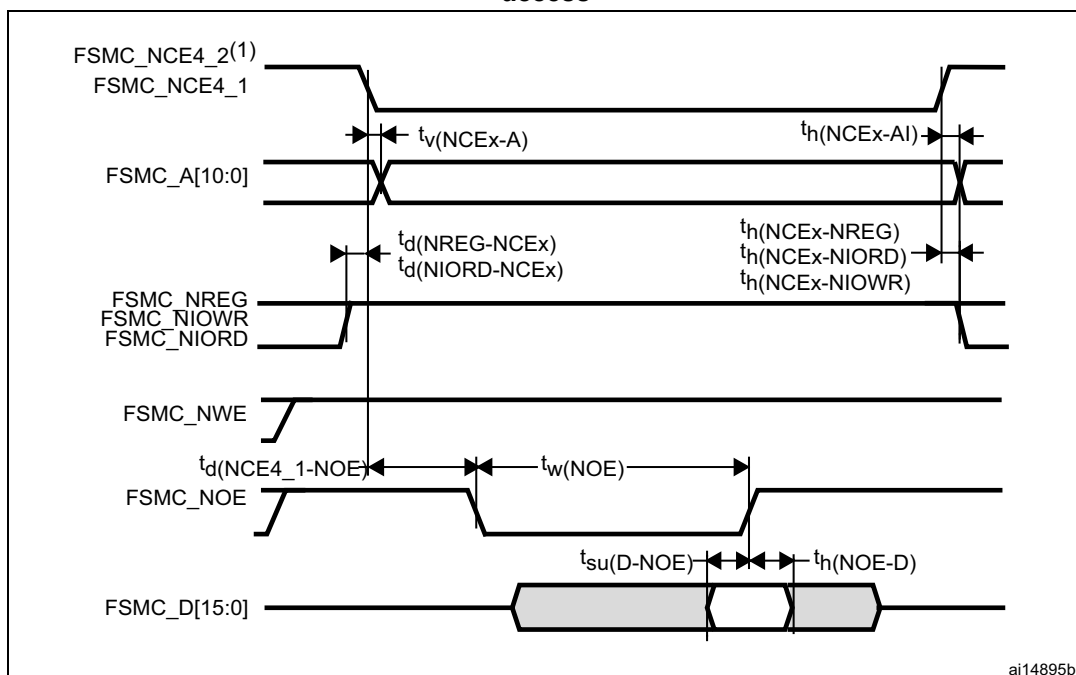
1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 66. PC Card/CompactFlash controller waveforms for common memory write access

Table 81. Switching characteristics for PC Card/CF read and write cycles in I/O space[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK} - 0.5$	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK} - 1$	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK} - 3$	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK} + 1.5$	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}$	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK} + 1$	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	$5T_{HCLK} - 0.5$	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK} + 1$	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. C_L = 30 pF.

2. Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 71 through *Figure 74* represent synchronous waveforms, together with *Table 82* and *Table 83* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

8 Ordering information

Table 96. Ordering information scheme

Example: STM32 F   205 R   E   T   6   V   xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

205 = STM32F20x, connectivity

207= STM32F20x, connectivity, camera interface, Ethernet

Pin count

R = 64 pins or 66 pins[(1)]

V = 100 pins

Z = 144 pins

I = 176 pins

Flash memory size

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

E = 512 Kbytes of Flash memory

F = 768 Kbytes of Flash memory

G = 1024 Kbytes of Flash memory

Package

T = LQFP

H = UFBGA

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Software option

Internal code or Blank

Options

xxx = programmed parts

TR = tape and reel

1.   The 66 pins is available on WLCSP package only.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, contact your nearest ST sales office.

Table 97. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	10	Changed minimum supply voltage from 1.65 to 1.8 V.
		Updated number of AHB buses in *Section 2: Description* and *Section 3.12: Clocks and startup*.
		Removed Figure 4. Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package.
		Updated *Note 2* below *Figure 4: STM32F20x block diagram*.
		Changed System memory to System memory + OTP in *Figure 16: Memory map*.
		Added *Note 1* below *Table 16: VCAP1/VCAP2 operating conditions*.
		Updated V_{DDA} and V_{REF+} decoupling capacitor in *Figure 19: Power supply scheme* and updated *Note 3*.
		Changed simplex mode into half-duplex mode in *Section 3.24: Inter-integrated sound (I2S)*.
		Replaced DAC1_OUT and DAC2_OUT by DAC_OUT1 and DAC_OUT2, respectively.Changed TIM2_CH1/TIM2_ETR into TIM2_CH1_ETR for PA0 and PA5 in *Table 10: Alternate function mapping*.
		Updated note applying to I_{DD} (external clock and all peripheral disabled) in *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*. Updated *Note 3* below *Table 22: Typical and maximum current consumption in Sleep mode*.
		Removed f_{HSE_ext} typical value in *Table 28: High-speed external user clock characteristics*.
		Updated master I2S clock jitter conditions and values in *Table 35: PLLI2S (audio PLL) characteristics*.
		Updated equations in *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*.
		Swapped TTL and CMOS port conditions for V_{OL} and V_{OH} in *Table 47: Output voltage characteristics*.
		Updated $V_{IL(NRST)}$ and $V_{IH(NRST)}$ in *Table 49: NRST pin characteristics*.
		Updated *Table 54: SPI characteristics* and *Table 55: I2S characteristics*. Removed note 1 related to measurement points below *Figure 43: SPI timing diagram - slave mode and CPHA = 1*, *Figure 44: SPI timing diagram - master mode*, and *Figure 45: I2S slave timing diagram (Philips protocol)(1)*.
		Updated t_{HC} in *Table 61: ULPI timing*.
		Updated *Figure 49: Ethernet SMI timing diagram*, *Table 63: Dynamics characteristics: Ethernet MAC signals for SMI* and *Table 65: Dynamics characteristics: Ethernet MAC signals for MII*.
		Update f_{TRIG} in *Table 66: ADC characteristics*.
		Updated I_{DDA} description in *Table 68: DAC characteristics*.
		Updated note below *Figure 54: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 55: Power supply and reference decoupling (VREF+ connected to VDDA)*.