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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207vct6tr

1 Introduction

This datasheet provides the description of the STM32F205xx and STM32F207xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F205xx and STM32F207xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F20x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART and UART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC.

3.9 Flexible static memory controller (FSMC)

The FSMC is embedded in all STM32F20x devices. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- Maximum frequency (f_{HCLK}) for external access is 60 MHz

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.10 Nested vectored interrupt controller (NVIC)

The STM32F20x devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M3.

The NVIC main features are the following:

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.20 Timers and watchdogs

The STM32F20x devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 5 compares the features of the advanced-control, general-purpose and basic timers.

Table 5. Timer feature comparison

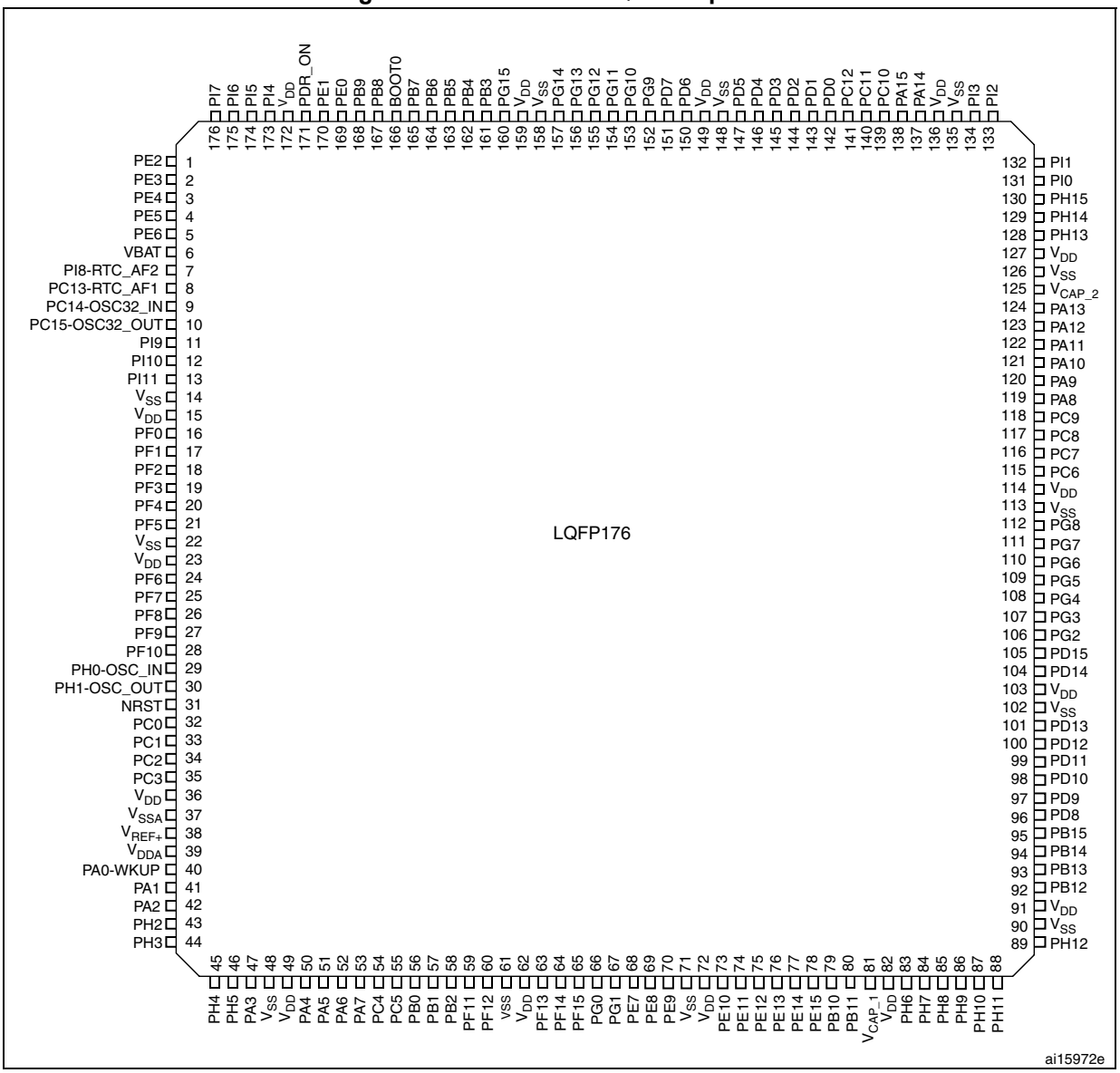
Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock	Max timer clock
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	60 MHz	120 MHz
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	30 MHz	60 MHz
General purpose	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	60 MHz	120 MHz
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	60 MHz	120 MHz
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	30 MHz	60 MHz
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	30 MHz	60 MHz

3.20.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

Figure 14. STM32F20x LQFP176 pinout



1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	131	159	C7	V_{DD}	S	-	-	-	-
-	-	-	132	160	B7	PG15	I/O	FT	-	USART6_CTS, DCMI_D13, EVENTOUT	-
55	A4	89	133	161	A10	PB3 (JTDO/TRACESWO)	I/O	FT	-	JTDO/ TRACESWO, SPI3_SCK, I2S3_SCK, TIM2_CH2, SPI1_SCK, EVENTOUT	-
56	B4	90	134	162	A9	PB4	I/O	FT	-	NJTRST, SPI3_MISO, TIM3_CH1, SPI1_MISO, EVENTOUT	-
57	A5	91	135	163	A6	PB5	I/O	FT	-	I2C1_SMBA, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, TIM3_CH2, SPI1_MOSI, SPI3_MOSI, DCMI_D10, I2S3_SD, EVENTOUT	-
58	B5	92	136	164	B6	PB6	I/O	FT	-	I2C1_SCL,, TIM4_CH1, CAN2_TX, DCMI_D5,USART1_TX, EVENTOUT	-
59	A6	93	137	165	B5	PB7	I/O	FT	-	I2C1_SDA, FSMC_NL(6), DCMI_VSYNC, USART1_RX, TIM4_CH2, EVENTOUT	-
60	B6	94	138	166	D6	BOOT0	I	B	-	-	V_{PP}
61	B7	95	139	167	A5	PB8	I/O	FT	-	TIM4_CH3,SDIO_D4, TIM10_CH1, DCMI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-
62	A7	96	140	168	B4	PB9	I/O	FT	-	SPI2_NSS, I2S2_WS, TIM4_CH4, TIM11_CH1, SDIO_D5, DCMI_D7, I2C1_SDA, CAN1_TX, EVENTOUT	-
-	-	97	141	169	A4	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, DCMI_D2, EVENTOUT	-

Table 12. Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	120	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	120	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	25	
$I_{INJ(PIN)}$ (2)	Injected current on five-volt tolerant I/O(3)	–5/+0	
	Injected current on any other pin(4)	±5	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	30	
f_{PCLK2}	Internal APB2 clock frequency	-	0	60	

Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled(3)	120 MHz	61	81	93	mA
			90 MHz	48	68	80	
			60 MHz	33	53	65	
			30 MHz	18	38	50	
			25 MHz	14	34	46	
			16 MHz(4)	10	30	42	
			8 MHz	6	26	38	
			4 MHz	4	24	36	
			2 MHz	3	23	35	
		External clock(2), all peripherals disabled	120 MHz	33	54	66	
			90 MHz	27	47	59	
			60 MHz	19	39	51	
			30 MHz	11	31	43	
			25 MHz	8	28	41	
			16 MHz(4)	6	26	38	
			8 MHz	4	24	36	
			4 MHz	3	23	35	
			2 MHz	2	23	34	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

Table 35. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12.288 MHz N=432, R=5 on 1000 samples		-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design, not tested in production.
3. Value given with main PLL running.
4. Guaranteed by characterization results, not tested in production.

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 42: EMI characteristics*). It is available only on the main PLL.

Table 36. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15}-1$	-

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.0002\%(peak)$$

Figure 44. SPI timing diagram - master mode

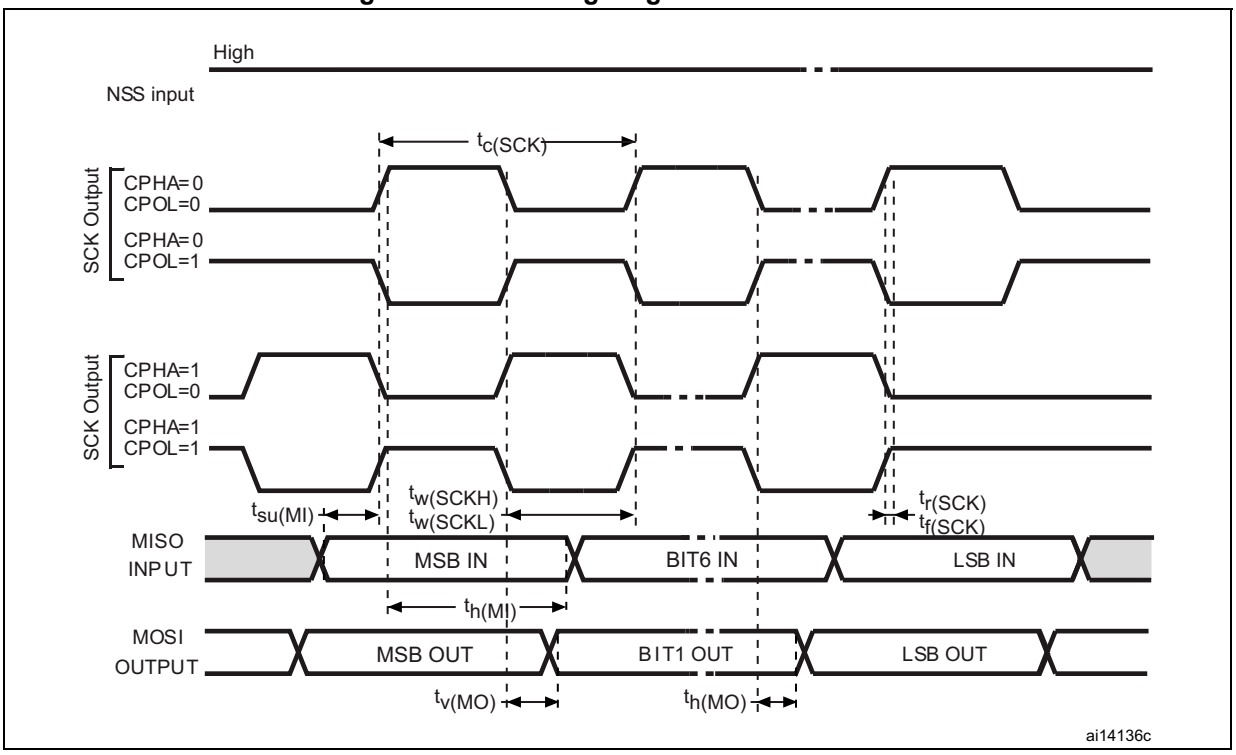


Table 65 gives the list of Ethernet MAC signals for MII and *Figure 50* shows the corresponding timing diagram.

Figure 51. Ethernet MII timing diagram

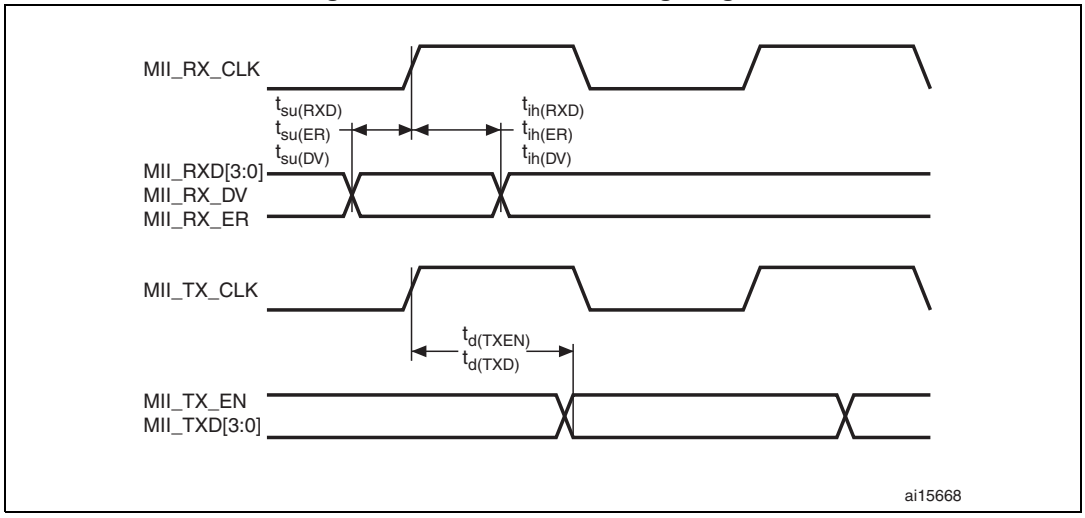


Table 65. Dynamics characteristics: Ethernet MAC signals for MII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	7.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1	-	-	ns
$t_{su(DV)}$	Data valid setup time	4	-	-	ns
$t_{ih(DV)}$	Data valid hold time	0	-	-	ns
$t_{su(ER)}$	Error setup time	3.5	-	-	ns
$t_{ih(ER)}$	Error hold time	0	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	-	11	14	ns
$t_{d(TXD)}$	Transmit data valid delay time	-	11	14	ns

CAN (controller area network) interface

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANTX and CANRX).

6.3.23 V_{BAT} monitoring characteristics

Table 70. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} (1 mV accuracy)	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.24 Embedded reference voltage

The parameters given in *Table 71* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 71. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

6.3.25 FSMC characteristics

Asynchronous waveforms and timings

Figure 57 through *Figure 60* represent asynchronous waveforms and *Table 72* through *Table 75* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 1
- DataSetupTime = 1
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 59. Asynchronous multiplexed PSRAM/NOR read waveforms

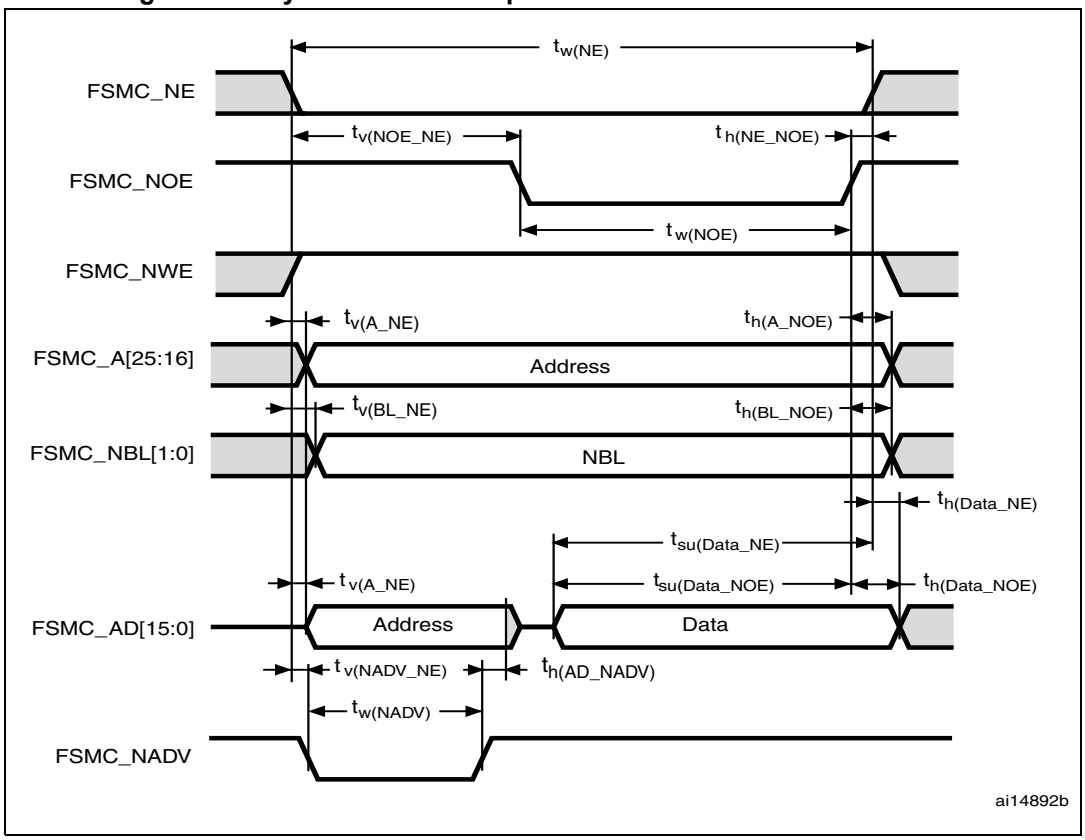
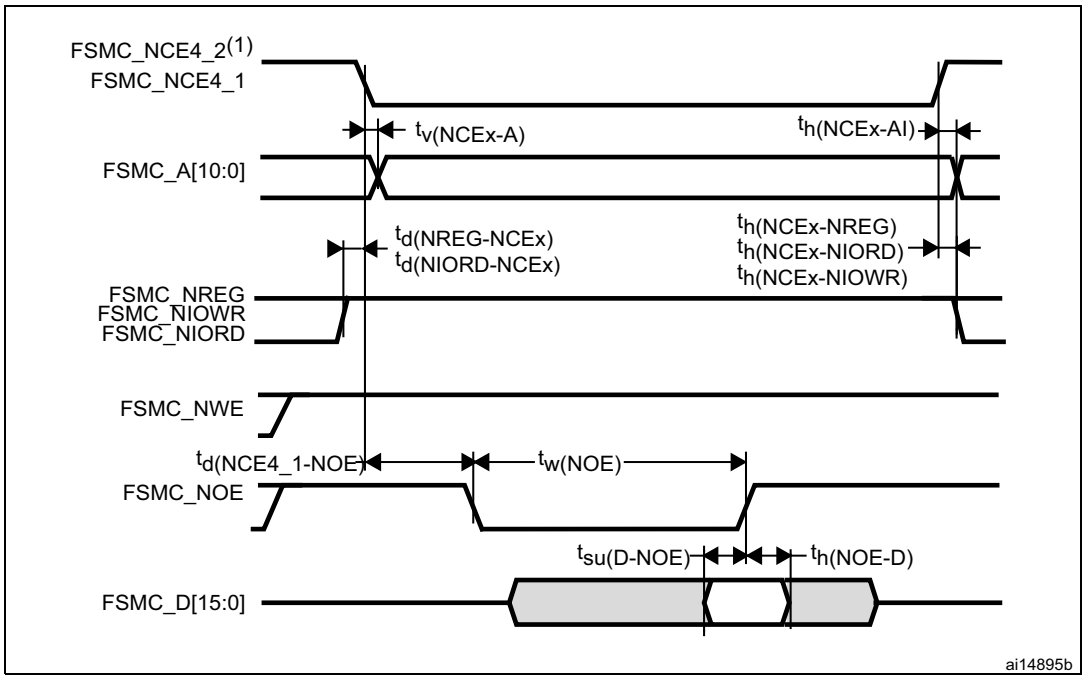


Table 74. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK}$-1	$3T_{HCLK}$+1	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$2T_{HCLK}$	$2T_{HCLK}$+0.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	T_{HCLK}-1	T_{HCLK}+1	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	2	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK}– 1.5	T_{HCLK}	ns
$t_{h(AD\_NADV)}$	FSMC_AD(adress) valid hold time after FSMC_NADV high)	T_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	T_{HCLK}	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	T_{HCLK}+ 2	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	T_{HCLK}+ 3	-	ns

Figure 65. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 66. PC Card/CompactFlash controller waveforms for common memory write access

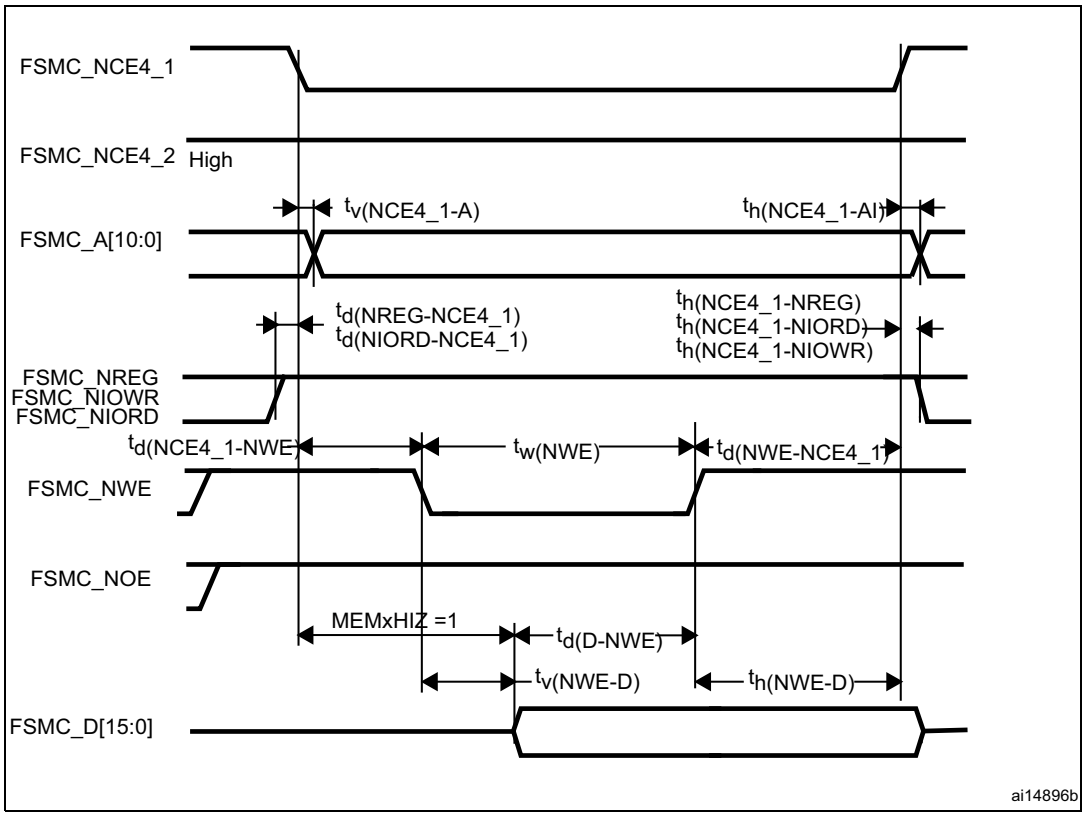


Figure 70. PC Card/CompactFlash controller waveforms for I/O space write access

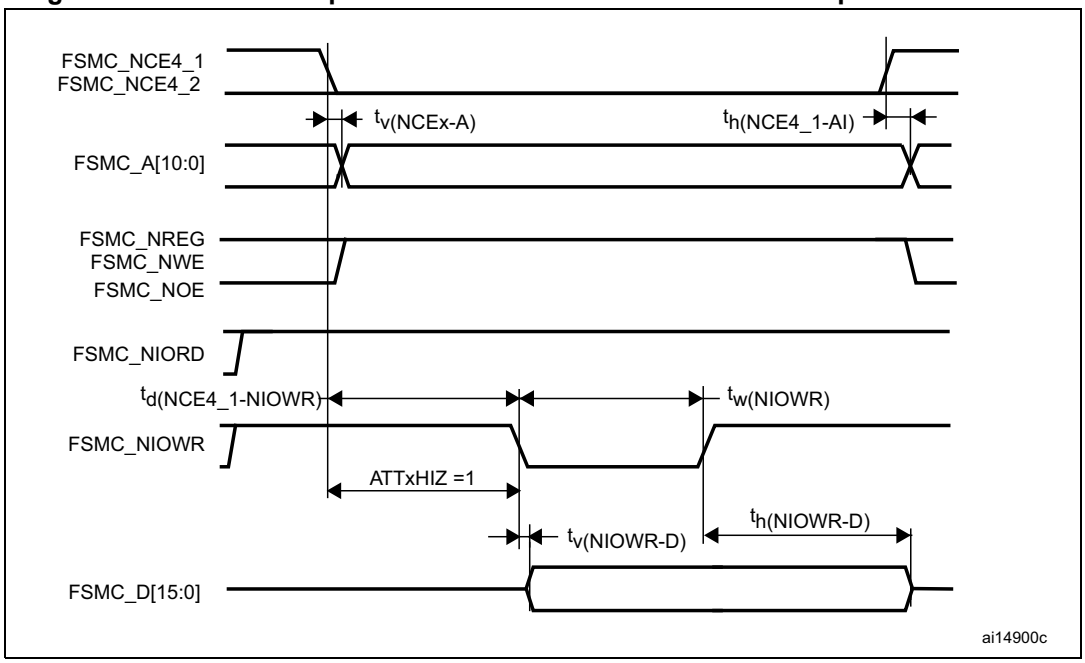


Table 80. Switching characteristics for PC Card/CF read and write cycles in attribute/common space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FSMC_Ncex low to FSMC_Ay valid	-	0	ns
$t_{h(NCEx\_AI)}$	FSMC_NCEx high to FSMC_Ax invalid	4	-	ns
$t_{d(NREG-NCEx)}$	FSMC_NCEx low to FSMC_NREG valid	-	3.5	ns
$t_{h(NCEx-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid	T_{HCLK}+ 4	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5T_{HCLK}$+ 1	ns
$t_{d(NCEx-NOE)}$	FSMC_NCEx low to FSMC_NOE low	-	$5T_{HCLK}$	ns
$t_{w(NOE)}$	FSMC_NOE low width	$8T_{HCLK}$– 0.5	$8T_{HCLK}$+ 1	ns
$t_{d(NOE\_NCEx)}$	FSMC_NOE high to FSMC_NCEx high	$5T_{HCLK}$+ 2.5	-	ns
$t_{su\ (D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	4	-	ns
$t_{h\ (N0E-D)}$	FSMC_N0E high to FSMC_D[15:0] invalid	2	-	ns
$t_{w(NWE)}$	FSMC_NWE low width	$8T_{HCLK}$- 1	$8T_{HCLK}$+ 4	ns
$t_{d(NWE\_NCEx)}$	FSMC_NWE high to FSMC_NCEx high	$5T_{HCLK}$+ 1.5	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	5HCLK+ 1	ns
$t_{v\ (NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h\ (NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$8T_{HCLK}$	-	ns
$t_{d\ (D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	$13T_{HCLK}$	-	ns

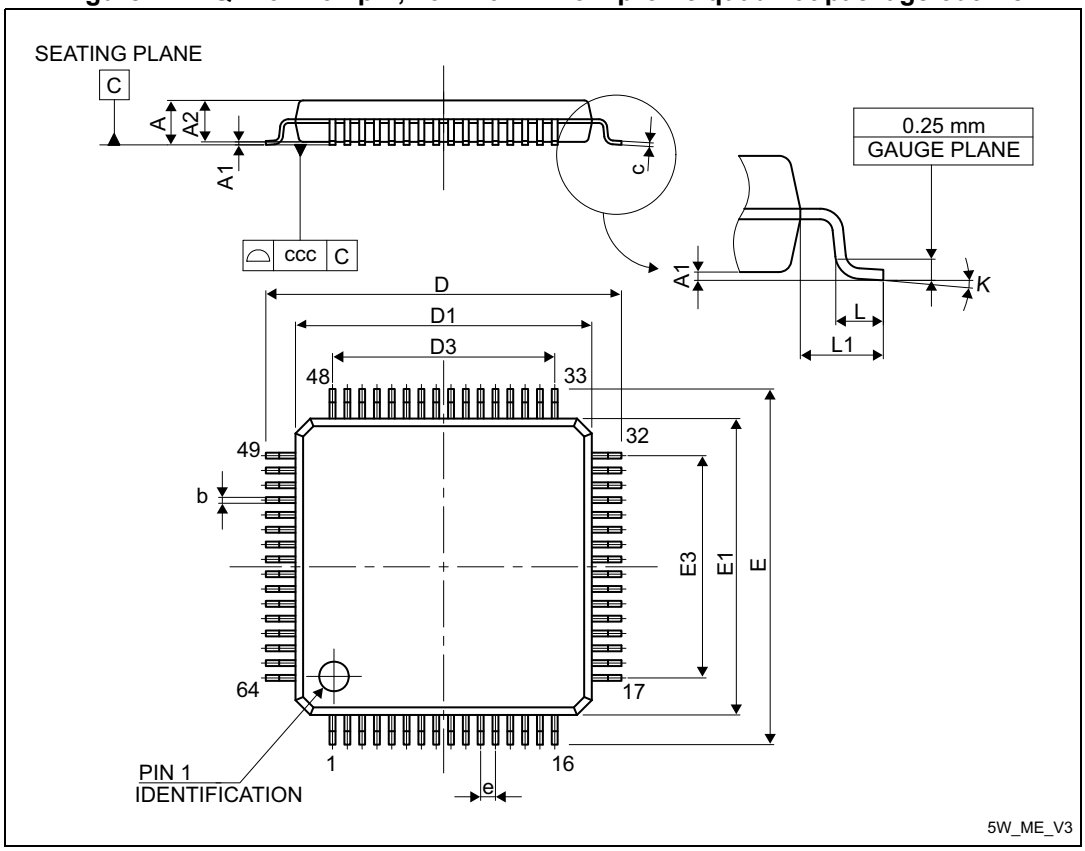
1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP64 package information

Figure 77. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

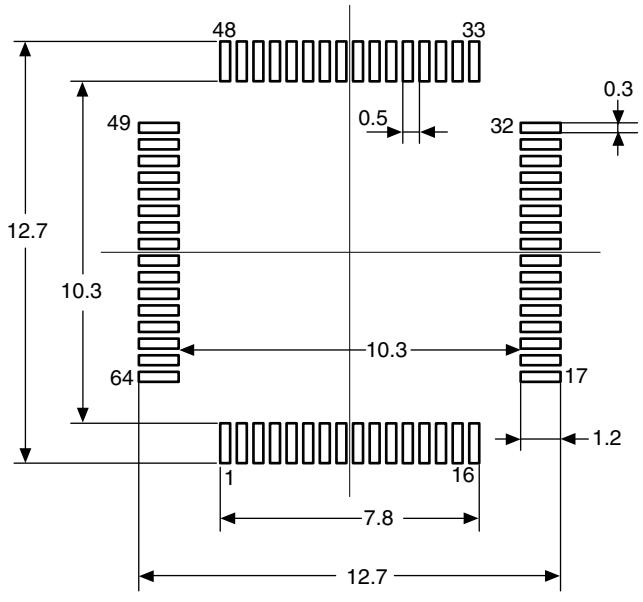
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106

Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 78. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

8 Ordering information

Table 96. Ordering information scheme

Example: STM32 F 205 R E T 6 V xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

205 = STM32F20x, connectivity

207= STM32F20x, connectivity, camera interface, Ethernet

Pin count

R = 64 pins or 66 pins(1)

V = 100 pins

Z = 144 pins

I = 176 pins

Flash memory size

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

E = 512 Kbytes of Flash memory

F = 768 Kbytes of Flash memory

G = 1024 Kbytes of Flash memory

Package

T = LQFP

H = UFBGA

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Software option

Internal code or Blank

Options

xxx = programmed parts

TR = tape and reel

1. The 66 pins is available on WLCSP package only.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, contact your nearest ST sales office.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6	Changed datasheet status to “Full Datasheet”. Introduced concept of SRAM1 and SRAM2. LQFP176 package now in production and offered only for 256 Kbyte and 1 Mbyte devices. Availability of WLCSP64+2 package limited to 512 Kbyte and 1 Mbyte devices. Updated *Figure 3: Compatible board design between STM32F10x and STM32F2xx for LQFP144 package* and *Figure 2: Compatible board design between STM32F10x and STM32F2xx for LQFP100 package*. Added camera interface for STM32F207Vx devices in *Table 2: STM32F205xx features and peripheral counts*. Removed 16 MHz internal RC oscillator accuracy in *Section 3.12: Clocks and startup*. Updated *Section 3.16: Voltage regulator*. Modified I^2S sampling frequency range in *Section 3.12: Clocks and startup*, *Section 3.24: Inter-integrated sound (I2S)*, and *Section 3.30: Audio PLL (PLLI2S)*. Updated *Section 3.17: Real-time clock (RTC), backup SRAM and backup registers* and description of TIM2 and TIM5 in *Section 3.20.2: General-purpose timers (TIMx)*. Modified maximum baud rate (oversampling by 16) for USART1 in *Table 6: USART feature comparison*. Updated note related to RFU pin below *Figure 12: STM32F20x LQFP100 pinout*, *Figure 13: STM32F20x LQFP144 pinout*, *Figure 14: STM32F20x LQFP176 pinout*, *Figure 15: STM32F20x UFBGA176 ballout*, and *Table 8: STM32F20x pin and ball definitions*. In *Table 8: STM32F20x pin and ball definitions*,:changed I2S2_CK and I2S3_CK to I2S2_SCK and I2S3_SCK, respectively; added PA15 and TT (3.6 V tolerant I/O). Added RTC_50Hz as PB15 alternate function in *Table 8: STM32F20x pin and ball definitions* and *Table 10: Alternate function mapping*. Removed ETH _RMII_TX_CLK for PC3/AF11 in *Table 10: Alternate function mapping*. Updated *Table 11: Voltage characteristics* and *Table 12: Current characteristics*. T_{STG} updated to –65 to +150 in *Table 13: Thermal characteristics*. Added CEXT, ESL, and ESR in *Table 14: General operating conditions* as well as *Section 6.3.2: VCAP1/VCAP2 external capacitor*. Modified *Note 4* in *Table 15: Limitations depending on the operating power supply range*. Updated *Table 17: Operating conditions at power-up / power-down (regulator ON)*, and *Table 18: Operating conditions at power-up / power-down (regulator OFF)*. Added OSC_OUT pin in *Figure 17: Pin loading conditions*. and *Figure 18: Pin input voltage*. Updated *Figure 19: Power supply scheme* to add IRROFF and REGOFF pins and modified notes. Updated V_{PVD}, V_{BOR1}, V_{BOR2}, V_{BOR3}, $T_{RSTTEMPO}$ typical value, and I_{RUSH}, added E_{RUSH} and *Note 2* in *Table 19: Embedded reset and power control block characteristics*.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Changed $t_{w(SCKH)}$ to $t_{w(SCLH)}$, $t_{w(SCKL)}$ to $t_{w(SCLL)}$, $t_{r(SCK)}$ to $t_{r(SCL)}$, and $t_{f(SCK)}$ to $t_{f(SCL)}$ in *Table 52: I2C characteristics* and in *Figure 41: I2C bus AC waveforms and measurement circuit*. Added *Table 57: USB OTG FS DC electrical characteristics* and updated *Table 58: USB OTG FS electrical characteristics*. Updated V_{DD} minimum value in *Table 62: Ethernet DC electrical characteristics*. Updated *Table 66: ADC characteristics* and R_{AIN} equation. Updated R_{AIN} equation. Updated *Table 68: DAC characteristics*. Updated t_{START} in *Table 69: Temperature sensor characteristics*. Updated R typical value in *Table 70: VBAT monitoring characteristics*. Updated *Table 71: Embedded internal reference voltage*. Modified FSMC_NOE waveform in *Figure 57: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms*. Shifted end of FSMC_NEx/NADV/addresses/NWE/NOE/NWAIT of a half FSMC_CLK period, changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, and $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and updated data latency from 1 to 0 in *Figure 61: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 62: Synchronous multiplexed PSRAM write timings*, *Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings*, and *Figure 64: Synchronous non-multiplexed PSRAM write timings*, Changed $t_{d(CLKH-NExH)}$) to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and modified $t_{w(CLK)}$ minimum value in *Table 76*, *Table 77*, *Table 78*, and *Table 79*. Updated note 2 in *Table 72*, *Table 73*, *Table 74*, *Table 75*, *Table 76*, *Table 77*, *Table 78*, and *Table 79*. Modified $t_{h(NIOWR-D)}$ in *Figure 70: PC Card/CompactFlash controller waveforms for I/O space write access*. Modified FSMC_NCEx signal in *Figure 71: NAND controller waveforms for read access*, *Figure 72: NAND controller waveforms for write access*, *Figure 73: NAND controller waveforms for common memory read access*, and *Figure 74: NAND controller waveforms for common memory write access* Specified Full speed (FS) mode for *Figure 89: USB OTG HS peripheral-only connection in FS mode* and *Figure 90: USB OTG HS host-only connection in FS mode*.