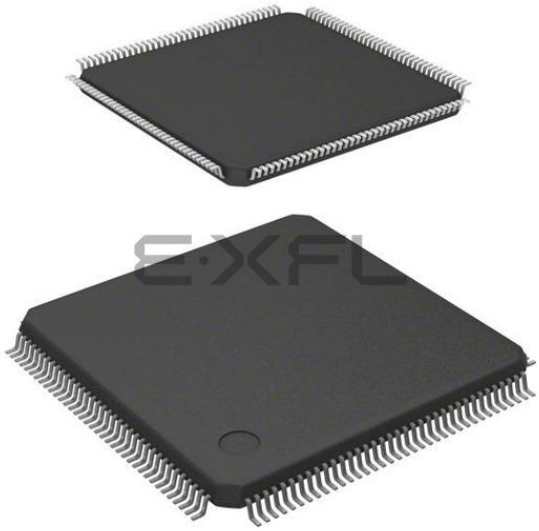

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207zct7tr

Contents

3.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

3.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In particular, the ethernet and USB OTG FS peripherals can be clocked by the system clock.

Several prescalers and PLLs allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 120 MHz and the maximum frequency the high-speed APB domains is 60 MHz. The maximum allowed frequency of the low-speed APB domain is 30 MHz.

The devices embed a dedicate PLL (PLLI2S) that allow them to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

3.14 Power supply schemes

- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode
- LPR is used in Stop modes

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost).

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to *Figure 19: Power supply scheme* and *Table 16: VCAP1/VCAP2 operating conditions*.

All packages have the regulator ON feature.

3.16.2 Regulator OFF

This feature is available only on packages featuring the REGOFF pin. The regulator is disabled by holding REGOFF high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP_1} and V_{CAP_2} pins.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 19: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

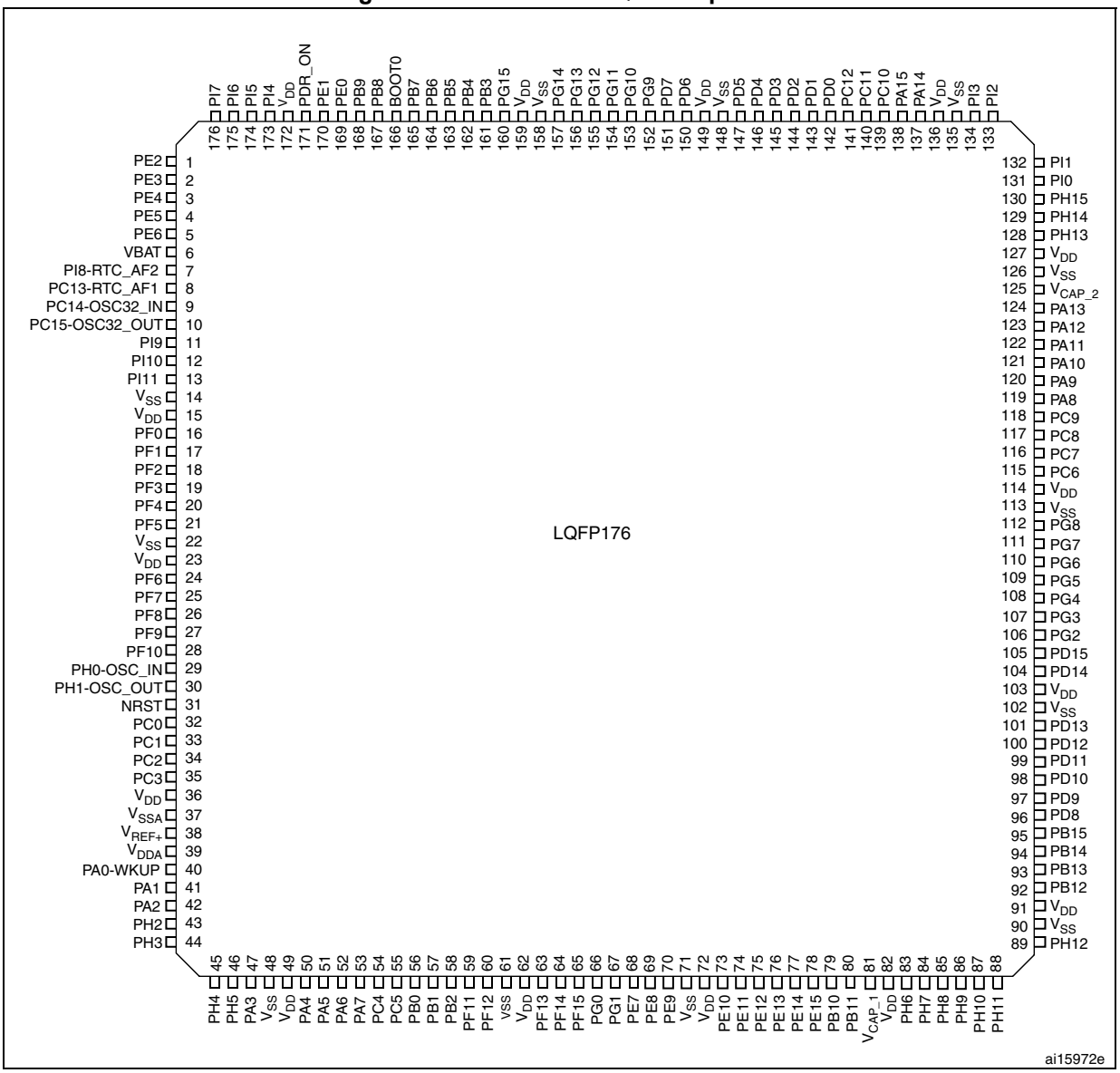
- PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used at power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection at reset or pre-reset is required.

Regulator OFF/internal reset ON

On WLCSP64+2 package, this mode is activated by connecting REGOFF pin to V_{DD} and IRROFF pin to V_{SS}. On UFBGA176 package, only REGOFF must be connected to V_{DD} (IRROFF not available). In this mode, V_{DD}/V_{DDA} minimum value is 1.8 V.

The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD}.

Figure 14. STM32F20x LQFP176 pinout



1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 15. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency ($f_{Flashmax}$)	Number of wait states at maximum CPU frequency (f_{CPUmax}= 120 MHz)(1)	I/O operation	FSMC_CLK frequency for synchronous accesses	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V(2)	Conversion time up to 1 Msps	16 MHz with no Flash memory wait state	7(3)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1 Msps	18 MHz with no Flash memory wait state	6(3)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2 Msps	24 MHz with no Flash memory wait state	4(3)	– Degraded speed performance – I/O compensation works	Up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(4)	Conversion time up to 2 Msps	30 MHz with no Flash memory wait state	3(3)	– Full-speed operation – I/O compensation works	– Up to 60 MHz when V_{DD} = 3.0 to 3.6 V – Up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 21*).
2. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

Figure 25. Typical current consumption vs. temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals ON

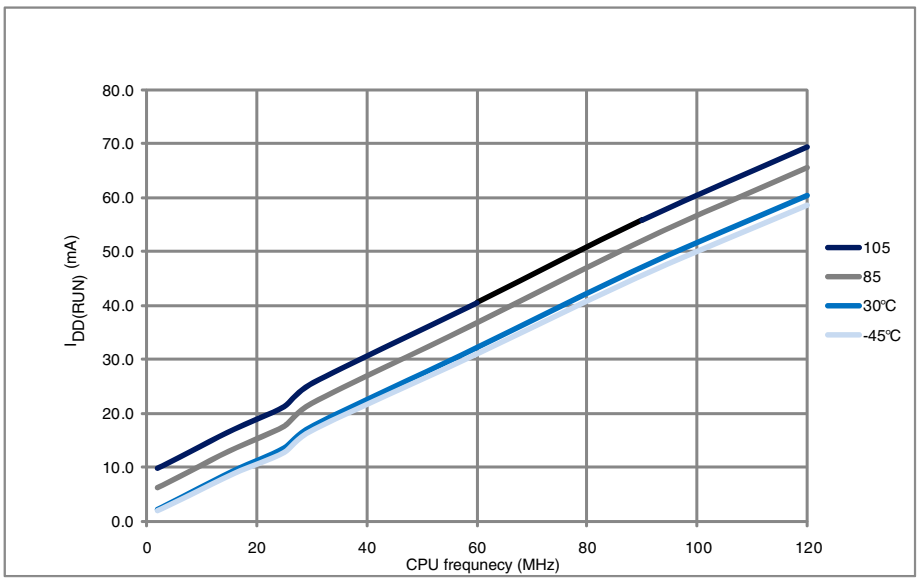


Figure 26. Typical current consumption vs. temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals OFF

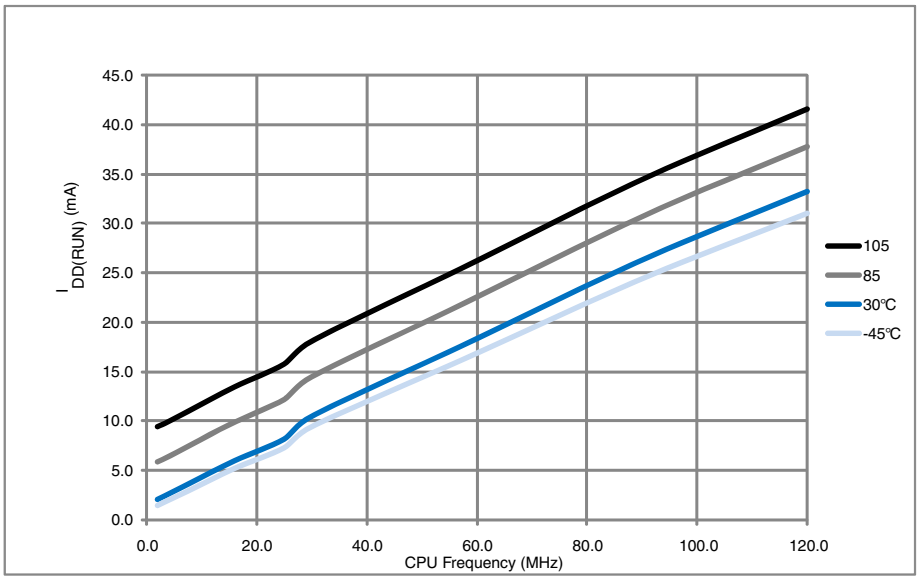


Table 26. Peripheral current consumption (continued)

Peripheral[1]		Typical consumption at 25 °C	Unit
APB2	SDIO	0.69	mA
	TIM1	1.06	
	TIM8	1.03	
	TIM9	0.58	
	TIM10	0.37	
	TIM11	0.39	
	ADC1[4]	2.13	
	ADC2[4]	2.04	
	ADC3[4]	2.12	
	SPI1	1.20	
	USART1	0.38	
	USART6	0.37	

1. External clock is 25 MHz (HSE oscillator with 25 MHz crystal) and PLL is on.
2. EN1 bit is set in DAC_CR register.
3. EN2 bit is set in DAC_CR register.
4. $f_{ADC} = f_{PCLK2}/2$, ADON bit set in ADC_CR2 register.

6.3.7 Wakeup time from low-power mode

The wakeup times given in *Table 27* is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Min[1]	Typ[1]	Max[1]	Unit
$t_{WUSLEEP}$[2]	Wakeup from Sleep mode	-	1	-	µs
t_{WUSTOP}[2]	Wakeup from Stop mode (regulator in Run mode)	-	13	-	µs
	Wakeup from Stop mode (regulator in low-power mode)	-	17	40	
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Deep power down mode)	-	110	-	
$t_{WUSTDBY}$[2][3]	Wakeup from Standby mode	260	375	480	µs

1. Guaranteed by characterization results, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and –45 °C, respectively.

Figure 49. Ethernet SMI timing diagram

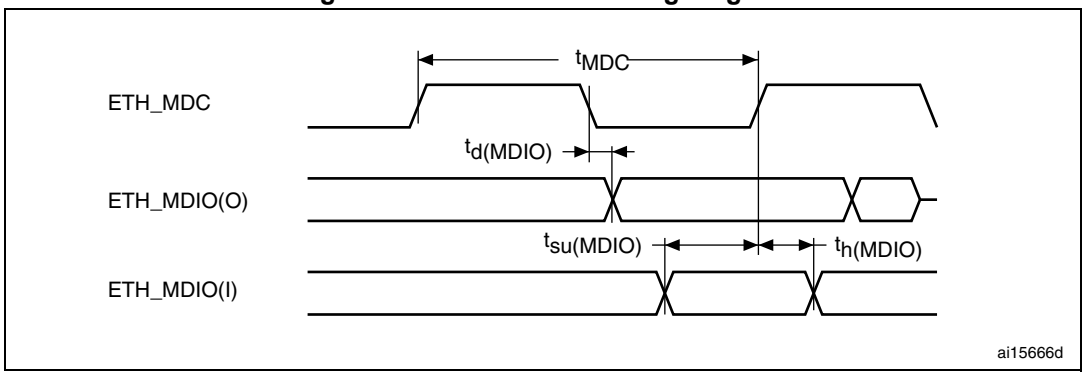


Table 63. Dynamics characteristics: Ethernet MAC signals for SMI

Symbol	Rating	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (2.38 MHz)	411	420	425	ns
$t_{d(MDIO)}$	MDIO write data valid time	6	10	13	ns
$t_{su(MDIO)}$	Read data setup time	12	-	-	ns
$t_{h(MDIO)}$	Read data hold time	0	-	-	ns

Table 64 gives the list of Ethernet MAC signals for the RMII and *Figure 50* shows the corresponding timing diagram.

Figure 50. Ethernet RMII timing diagram

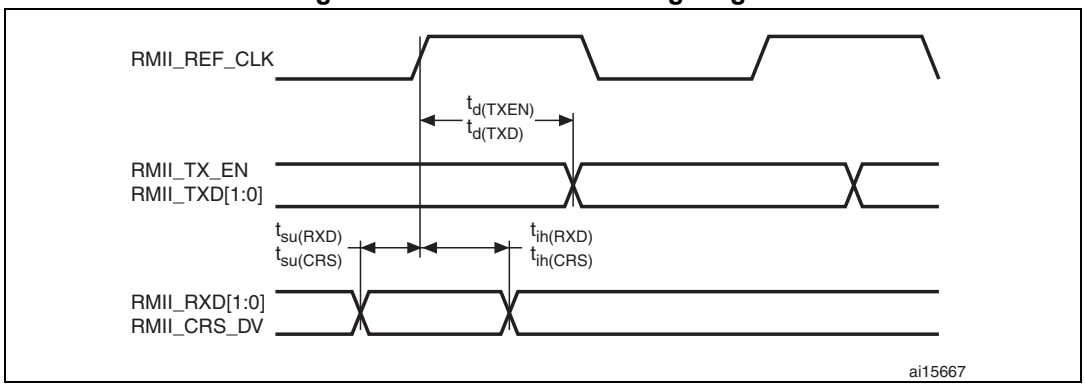


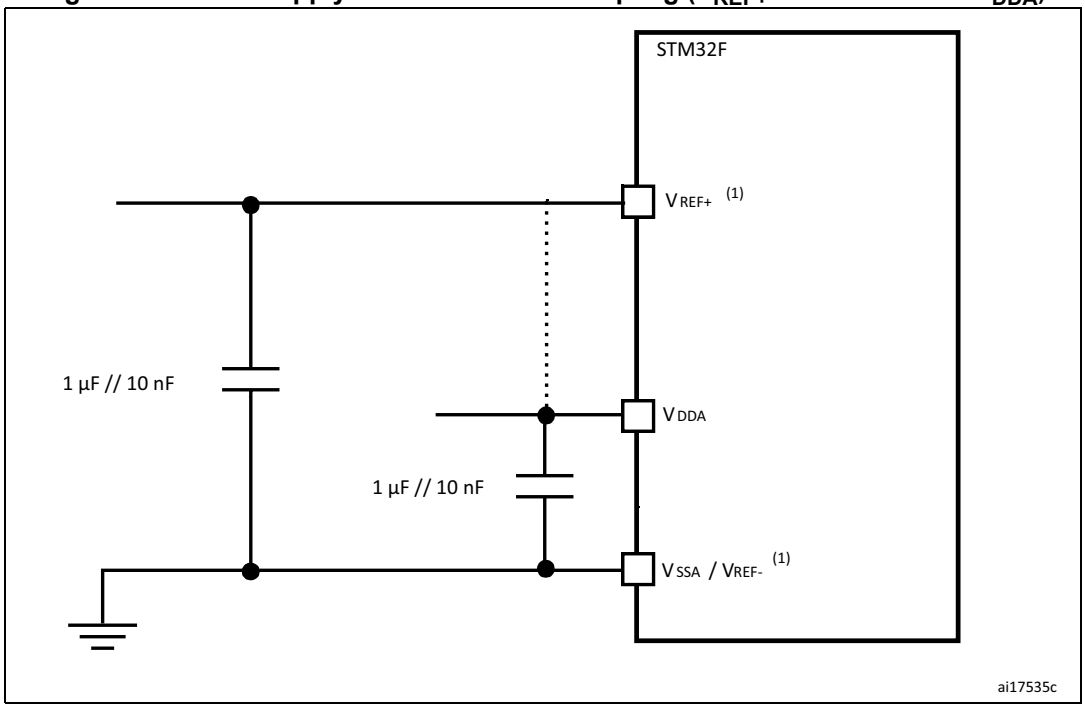
Table 64. Dynamics characteristics: Ethernet MAC signals for RMII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1.5	-	-	
$t_{su(CRS)}$	Carrier sense set-up time	0	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	9	11	13	
$t_{d(TXD)}$	Transmit data valid delay time	9	11.5	14	

General PCB design guidelines

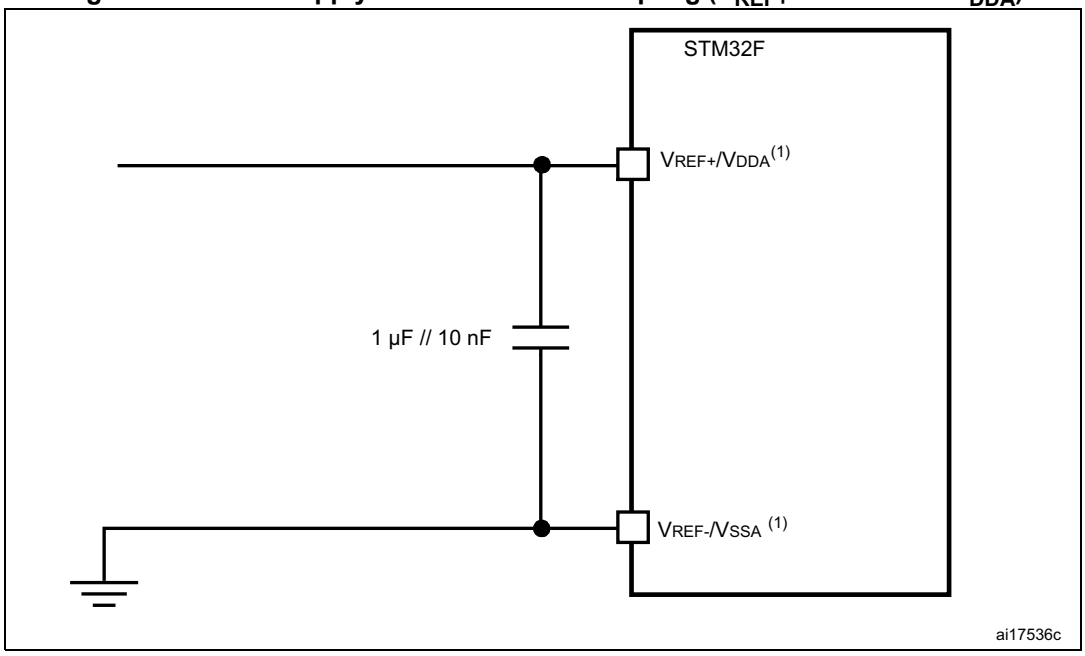
Power supply decoupling should be performed as shown in *Figure 54* or *Figure 55*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 54. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Figure 55. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.21 DAC electrical characteristics

Table 68. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.8(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage	1.8(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.8 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	

Figure 59. Asynchronous multiplexed PSRAM/NOR read waveforms

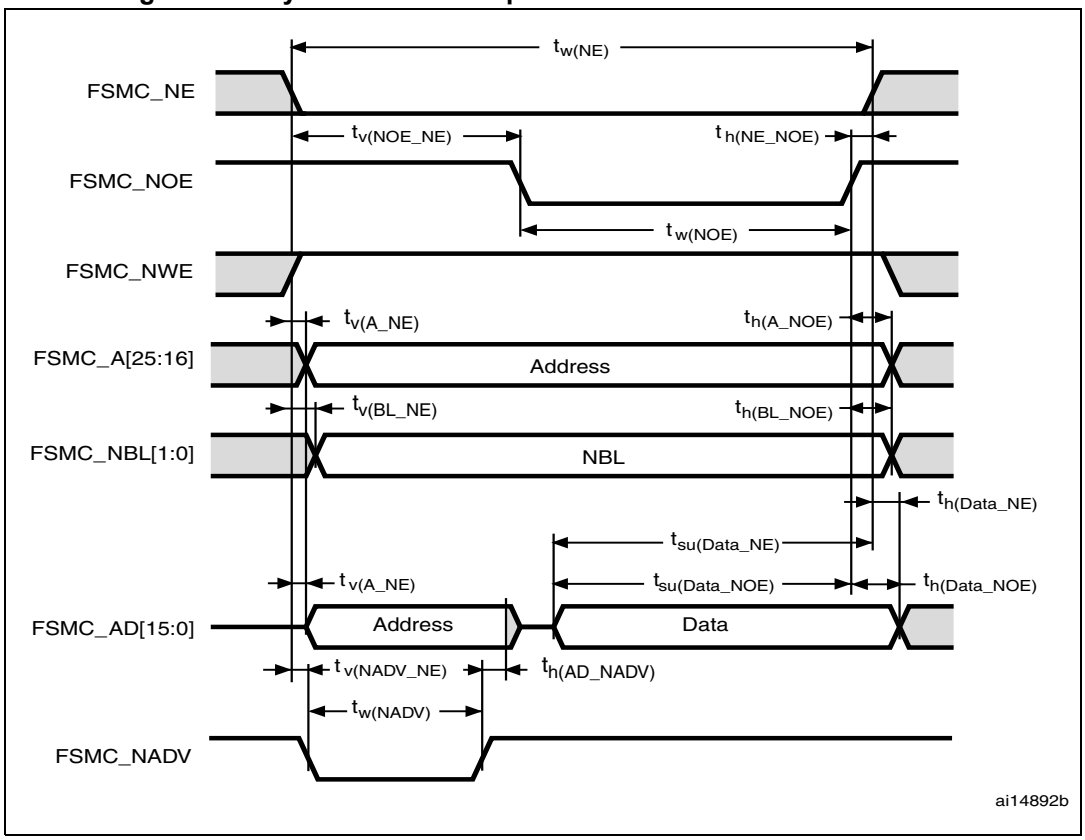


Table 74. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK}$-1	$3T_{HCLK}$+1	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$2T_{HCLK}$	$2T_{HCLK}$+0.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	T_{HCLK}-1	T_{HCLK}+1	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	2	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK}– 1.5	T_{HCLK}	ns
$t_{h(AD\_NADV)}$	FSMC_AD(adress) valid hold time after FSMC_NADV high)	T_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	T_{HCLK}	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	T_{HCLK}+ 2	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	T_{HCLK}+ 3	-	ns

Figure 71. NAND controller waveforms for read access

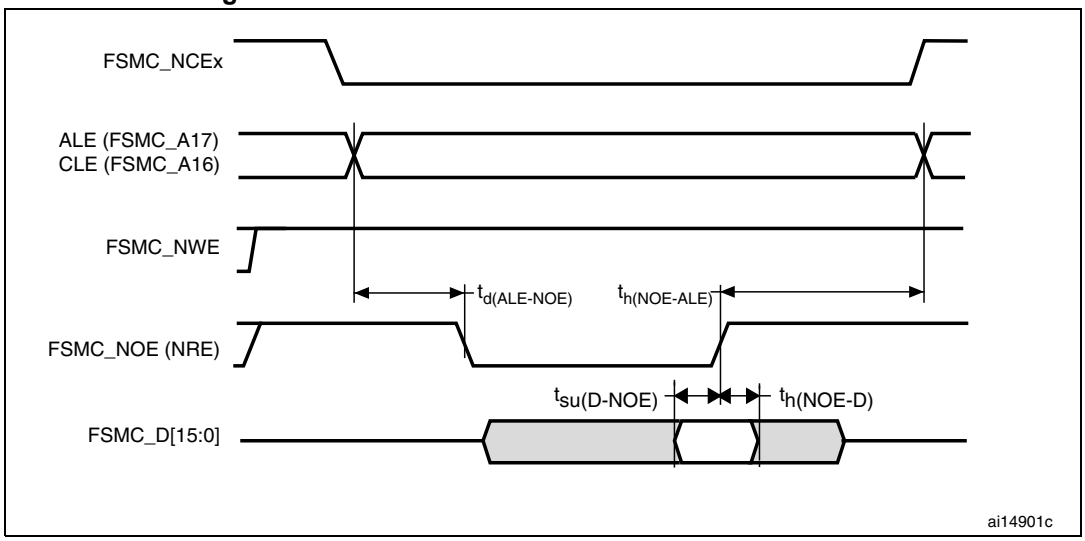


Figure 72. NAND controller waveforms for write access

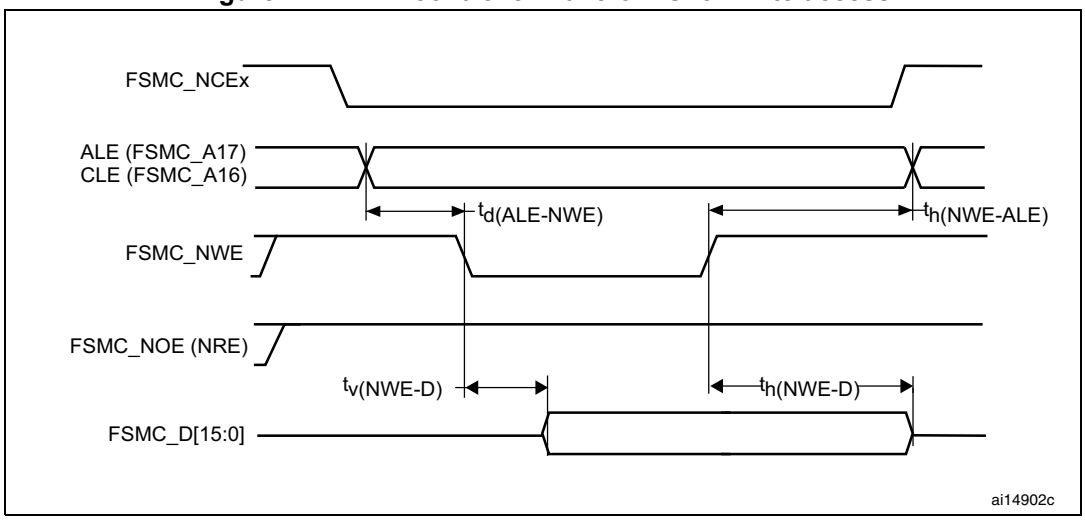
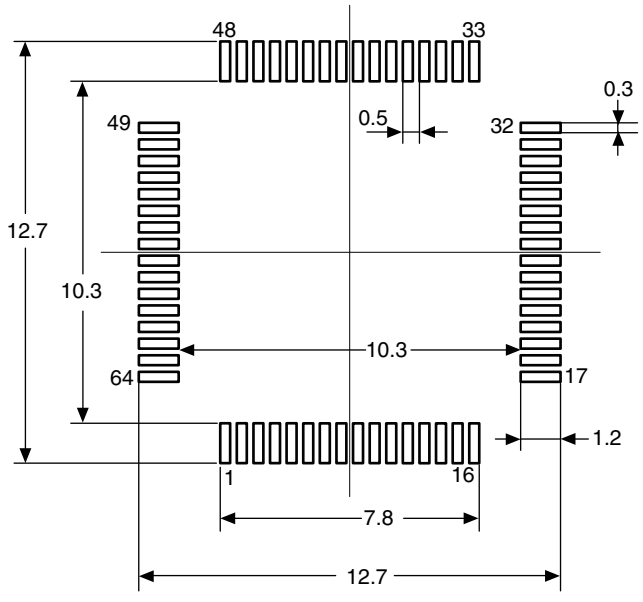


Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 78. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



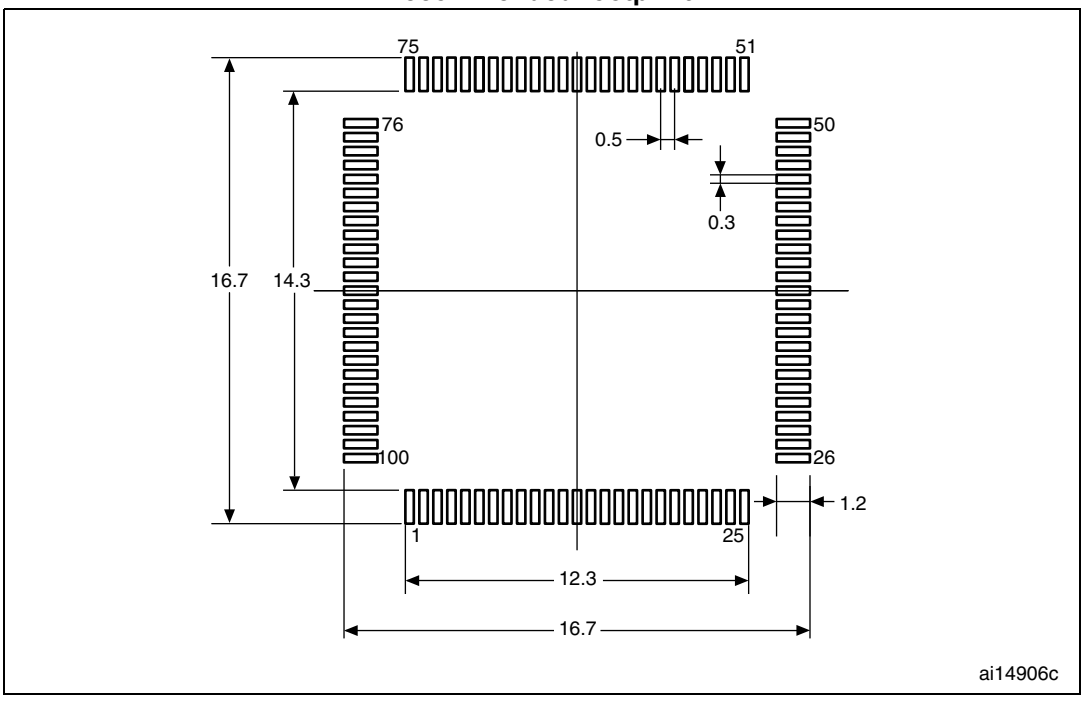
1. Dimensions are expressed in millimeters.

Table 90. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

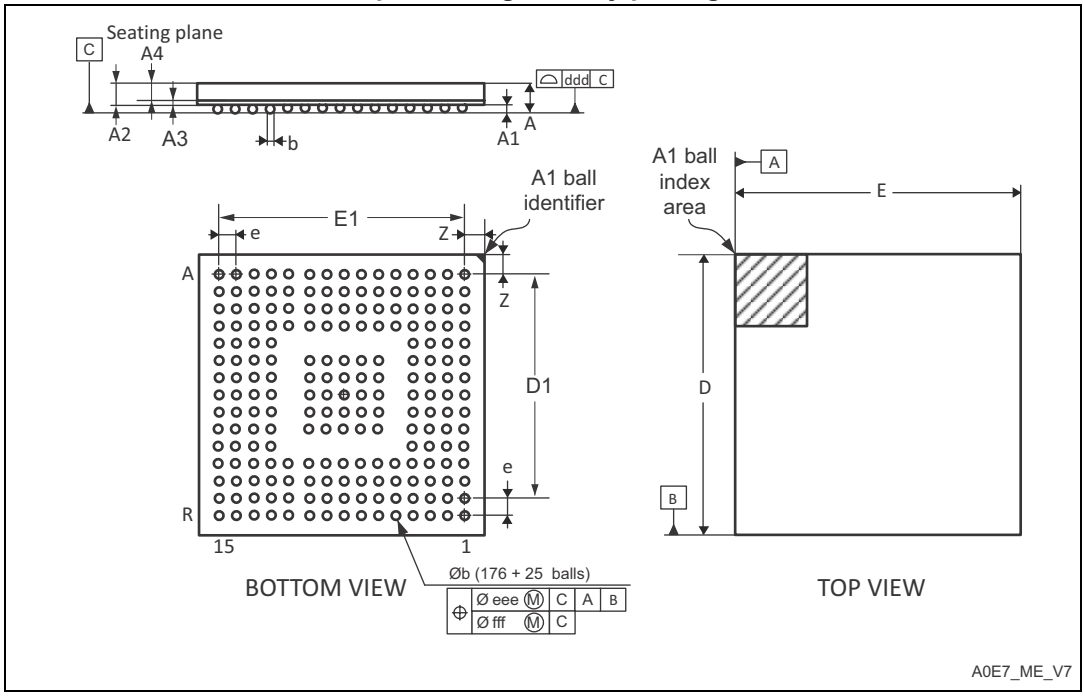
Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

7.6 UFBGA176+25 package information

Figure 89. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 93. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Updated *Typical and maximum current consumption* conditions, as well as *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)* and *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*. Added *Figure 23*, *Figure 24*, *Figure 25*, and *Figure 26*. Updated *Table 22: Typical and maximum current consumption in Sleep mode*, and added *Figure 27* and *Figure 28*. Updated *Table 23: Typical and maximum current consumptions in Stop mode*. Added *Figure 29: Typical current consumption vs. temperature in Stop mode*. Updated *Table 24: Typical and maximum current consumptions in Standby mode* and *Table 25: Typical and maximum current consumptions in VBAT mode*. Updated *On-chip peripheral current consumption* conditions and *Table 26: Peripheral current consumption*. Updated $t_{WUSTDBY}$ and t_{WUSTOP}, and added *Note 3* in *Table 27: Low-power mode wakeup timings*. Maximum f_{HSE_ext} and minimum $t_{w(HSE)}$ values updated in *Table 28: High-speed external user clock characteristics*. Updated C and g_m in *Table 30: HSE 4-26 MHz oscillator characteristics*. Updated R_F, I_2, g_m, and $t_{su(LSE)}$ in *Table 31: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Added *Note 1* and updated ACC_{HSI}, $IDD_{(HSI}$, and $t_{su(HSI)}$ in *Table 32: HSI oscillator characteristics*. Added *Figure 34: ACCHSI versus temperature*. Updated f_{LSI}, $t_{su(LSI)}$ and $IDD_{(LSI)}$ in *Table 33: LSI oscillator characteristics*. Added *Figure 35: ACCLSI versus temperature* *Table 34: Main PLL characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLL)}$ and $IDD_{A(PLL)}$, added *Note 2* for f_{PLL_IN} minimum and maximum values. *Table 35: PLLI2S (audio PLL) characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLLI2S)}$ and $IDD_{A(PLLI2S)}$, added *Note 2* for f_{PLLI2S_IN} minimum and maximum values. Added *Note 1* in *Table 36: SSCG parameters constraint*. Updated *Table 37: Flash memory characteristics*. Modified *Table 38: Flash memory programming* and added *Note 2* for t_{prog}. Updated t_{prog} and added *Note 1* in *Table 39: Flash memory programming with VPP*. Modified *Figure 40: Recommended NRST pin protection*. Updated *Table 42: EMI characteristics* and EMI monitoring conditions in *Section : Electromagnetic Interference (EMI)*. Added *Note 2* related to $V_{ESD(HBM)}$in *Table 43: ESD absolute maximum ratings*. Updated *Table 48: I/O AC characteristics*. Added *Section 6.3.15: I/O current injection characteristics*. Modified maximum frequency values and conditions in *Table 48: I/O AC characteristics*. Updated $t_{res(TIM)}$ in *Table 50: Characteristics of TIMx connected to the APB1 domain*. Modified $t_{res(TIM)}$ and f_{EXT} *Table 51: Characteristics of TIMx connected to the APB2 domain*.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Changed $t_{w(SCKH)}$ to $t_{w(SCLH)}$, $t_{w(SCKL)}$ to $t_{w(SCLL)}$, $t_{r(SCK)}$ to $t_{r(SCL)}$, and $t_{f(SCK)}$ to $t_{f(SCL)}$ in *Table 52: I2C characteristics* and in *Figure 41: I2C bus AC waveforms and measurement circuit*. Added *Table 57: USB OTG FS DC electrical characteristics* and updated *Table 58: USB OTG FS electrical characteristics*. Updated V_{DD} minimum value in *Table 62: Ethernet DC electrical characteristics*. Updated *Table 66: ADC characteristics* and R_{AIN} equation. Updated R_{AIN} equation. Updated *Table 68: DAC characteristics*. Updated t_{START} in *Table 69: Temperature sensor characteristics*. Updated R typical value in *Table 70: VBAT monitoring characteristics*. Updated *Table 71: Embedded internal reference voltage*. Modified FSMC_NOE waveform in *Figure 57: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms*. Shifted end of FSMC_NEx/NADV/addresses/NWE/NOE/NWAIT of a half FSMC_CLK period, changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, and $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and updated data latency from 1 to 0 in *Figure 61: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 62: Synchronous multiplexed PSRAM write timings*, *Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings*, and *Figure 64: Synchronous non-multiplexed PSRAM write timings*, Changed $t_{d(CLKH-NExH)}$) to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and modified $t_{w(CLK)}$ minimum value in *Table 76*, *Table 77*, *Table 78*, and *Table 79*. Updated note 2 in *Table 72*, *Table 73*, *Table 74*, *Table 75*, *Table 76*, *Table 77*, *Table 78*, and *Table 79*. Modified $t_{h(NIOWR-D)}$ in *Figure 70: PC Card/CompactFlash controller waveforms for I/O space write access*. Modified FSMC_NCEx signal in *Figure 71: NAND controller waveforms for read access*, *Figure 72: NAND controller waveforms for write access*, *Figure 73: NAND controller waveforms for common memory read access*, and *Figure 74: NAND controller waveforms for common memory write access* Specified Full speed (FS) mode for *Figure 89: USB OTG HS peripheral-only connection in FS mode* and *Figure 90: USB OTG HS host-only connection in FS mode*.