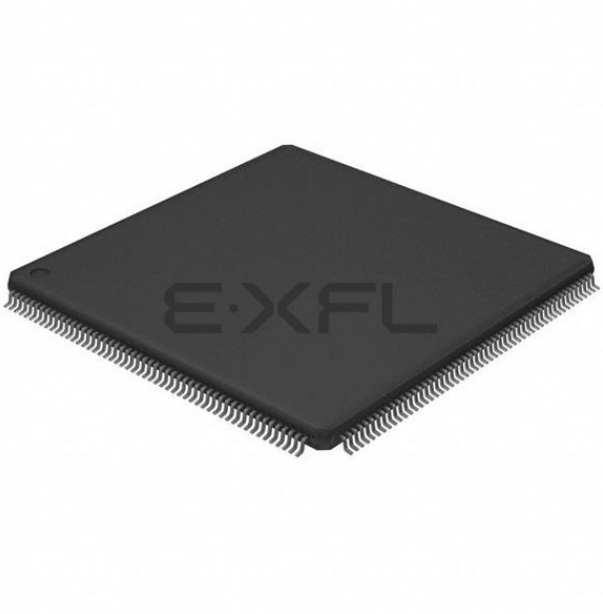


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	160
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	98K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2470fbd208-551

- Each peripheral has its own clock divider for further power saving. These dividers help reduce active power by 20 % to 30 %.
- Brownout detect with separate thresholds for interrupt and forced reset.
- On-chip power-on reset.
- On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Boundary scan for simplified board testing.
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace module supports real-time trace.

3. Applications

- Industrial control
- Medical systems
- Portable electronics
- Point-of-Sale (POS) equipment

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2470FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC2470FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					External bus	Ethernet	USB OTG/ OHCI/ device + 4 kB FIFO	CAN channels	SD/ MMC	GP DMA	ADC channels	DAC channels	Temp range
		Local bus	Ethernet buffer	GP/USB	RTC	Total									
LPC2470FBD208	n/a	64	16	16	2	98	Full 32-bit	MII/RMII	yes	2	yes	yes	8	1	−40 °C to +85 °C
LPC2470FET208	n/a	64	16	16	2	98	Full 32-bit	MII/RMII	yes	2	yes	yes	8	1	−40 °C to +85 °C

6. Pinning information

6.1 Pinning

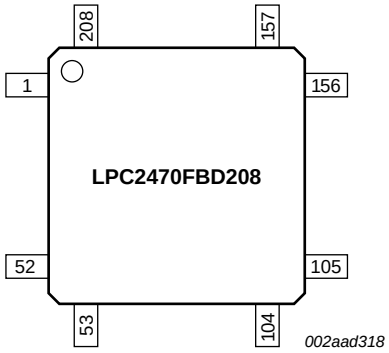


Fig 2. LPC2470 pinning LQFP208 package

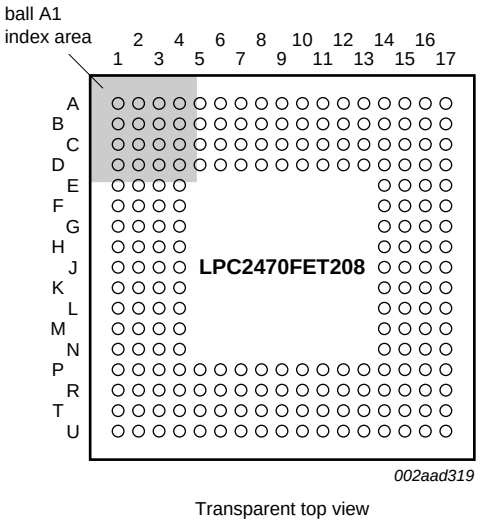


Fig 3. LPC2470 pinning TFBGA208 package

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	P3[27]/D27/ CAP1[0]/PWM1[4]	2	V_{SSIO}	3	P1[0]/ENET_TXD0	4	P4[31]/$\overline{CS1}$
5	P1[4]/ENET_TX_EN	6	P1[9]/ENET_RXD0	7	P1[14]/ENET_RX_ER	8	P1[15]/ ENET_REF_CLK/ ENET_RX_CLK
9	P1[17]/ENET_MDIO	10	P1[3]/ENET_TXD3/ MCICMD/PWM0[2]	11	P4[15]/A15	12	V_{SSIO}

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
13	P3[20]/D20/ PWM0[5]/DSR1	14	P1[11]/ENET_RXD2/ MCIDAT2/PWM0[6]	15	P0[8]/I2STX_WS/ LCDVD[16]/MISO1/ MAT2[2]	16	P1[12]/ENET_RXD3/ MCIDAT3/PCAP0[0]
17	P1[5]/ENET_TX_ER/ MCIPWR/PWM0[3]		-		-		-
Row B							
1	P3[2]/D2	2	P3[10]/D10	3	P3[1]/D1	4	P3[0]/D0
5	P1[1]/ENET_TXD1	6	V_{SSIO}	7	P4[30]/$\overline{CS0}$	8	P4[24]/$\overline{OE}$
9	P4[25]/$\overline{WE}$	10	P4[29]/$\overline{BLS3}$/MAT2[1]/ LCDVD[7]/LCDVD[11]/ LCDVD[3]/RXD3	11	P1[6]/ENET_TX_CLK/ MCIDAT0/PWM0[4]	12	P0[4]/I2SRX_CLK/ LCDVD[0]/RD2/CAP2[0]
13	$V_{DD(3V3)}$	14	P3[19]/D19/ PWM0[4]/DCD1	15	P4[14]/A14	16	P4[13]/A13
17	P2[0]/PWM1[1]/TXD1/ TRACECLK/LCDPWR		-		-		-
Row C							
1	P3[13]/D13	2	TDI	3	RTCK	4	P0[2]/TXD0
5	P3[9]/D9	6	P3[22]/D22/ PCAP0[0]/RI1	7	P1[8]/ENET_CRS_DV/ ENET_CRS	8	P1[10]/ENET_RXD1
9	$V_{DD(3V3)}$	10	P3[21]/D21/ PWM0[6]/DTR1	11	P4[28]/$\overline{BLS2}$/MAT2[0]/ LCDVD[6]/LCDVD[10]/ LCDVD[2]/TXD3	12	P0[5]/I2SRX_WS/ LCDVD[1]/TD2/CAP2[1]
13	P0[7]/I2STX_CLK/ LCDVD[9]/SCK1/ MAT2[1]	14	P0[9]/I2STX_SDA/ LCDVD[17]/MOSI1/ MAT2[3]	15	P3[18]/D18/ PWM0[3]/CTS1	16	P4[12]/A12
17	$V_{DD(3V3)}$		-		-		-
Row D							
1	$\overline{TRST}$	2	P3[28]/D28/ CAP1[1]/PWM1[5]	3	TDO	4	P3[12]/D12
5	P3[11]/D11	6	P0[3]/RXD0	7	$V_{DD(3V3)}$	8	P3[8]/D8
9	P1[2]/ENET_TXD2/ MCICLK/PWM0[1]	10	P1[16]/ENET_MDC	11	$V_{DD(DCDC)(3V3)}$	12	V_{SSCORE}
13	P0[6]/I2SRX_SDA/ LCDVD[8]/SSEL1/ MAT2[0]	14	P1[7]/ENET_COL/ MCIDAT1/PWM0[5]	15	P2[2]/PWM1[3]/CTS1/ PIPESTAT1/LCDDCLK	16	P1[13]/ENET_RX_DV
17	P2[4]/PWM1[5]/ DSR1/TRACESYNC/ LCDENAB/LCDM		-		-		-
Row E							
1	P0[26]/AD0[3]/ AOUT/RXD3	2	TCK	3	TMS	4	P3[3]/D3
14	P2[1]/PWM1[2]/RXD1/ PIPESTAT0/LCDLE	15	V_{SSIO}	16	P2[3]/PWM1[4]/DCD1/ PIPESTAT2/LCDFP	17	P2[6]/PCAP1[0]/RI1/ TRACEPKT1/ LCDVD[0]/LCDVD[4]
Row F							
1	P0[25]/AD0[2]/ I2SRX_SDA/TXD3	2	P3[4]/D4	3	P3[29]/D29/ MAT1[0]/PWM1[6]	4	DBGEN

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Ball	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0[0]/RD1/TXD3/ SDA1	94[1]	U15[1]	I/O	**P0[0] —** General purpose digital input/output pin.
			I	**RD1 —** CAN1 receiver input.
			O	**TXD3 —** Transmitter output for UART3.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[1]/TD1/RXD3/ SCL1	96[1]	T14[1]	I/O	**P0[1] —** General purpose digital input/output pin.
			O	**TD1 —** CAN1 transmitter output.
			I	**RXD3 —** Receiver input for UART3.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[2]/TXD0	202[1]	C4[1]	I/O	**P0[2] —** General purpose digital input/output pin.
			O	**TXD0 —** Transmitter output for UART0.
P0[3]/RXD0	204[1]	D6[1]	I/O	**P0[3] —** General purpose digital input/output pin.
			I	**RXD0 —** Receiver input for UART0.
P0[4]/I2SRX_CLK/ LCDVD[0]/RD2/ CAP2[0]	168[1]	B12[1]	I/O	**P0[4] —** General purpose digital input/output pin.
			I/O	**I2SRX_CLK —** I^2S Receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.[2]
			O	**LCDVD[0] —** LCD data.[2]
			I	**RD2 —** CAN2 receiver input.
			I	**CAP2[0] —** Capture input for Timer 2, channel 0.
P0[5]/I2SRX_WS/ LCDVD[1]/TD2/ CAP2[1]	166[1]	C12[1]	I/O	**P0[5] —** General purpose digital input/output pin.
			I/O	**I2SRX_WS —** I^2S Receive word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.[2]
			O	**LCDVD[1] —** LCD data.[2]
			O	**TD2 —** CAN2 transmitter output.
			I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/I2SRX_SDA/ LCDVD[8]/ SSEL1/MAT2[0]	164[1]	D13[1]	I/O	**P0[6] —** General purpose digital input/output pin.
			I/O	**I2SRX_SDA —** I^2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.[2]
			O	**LCDVD[8] —** LCD data.[2]
			I/O	**SSEL1 —** Slave Select for SSP1.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P0[7]/I2STX_CLK/ LCDVD[9]/SCK1/ MAT2[1]	162[1]	C13[1]	I/O	**P0[7] —** General purpose digital input/output pin.
			I/O	**I2STX_CLK —** I^2S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.[2]
			O	**LCDVD[9] —** LCD data.[2]
			I/O	**SCK1 —** Serial Clock for SSP1.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/I2STX_WS/ LCDVD[16]/ MISO1/MAT2[2]	160[1]	A15[1]	I/O	**P0[8] —** General purpose digital input/output pin.
			I/O	**I2STX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.[2]
			O	**LCDVD[16] —** LCD data.[2]
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/I2STX_SDA/ LCDVD[17]/ MOSI1/MAT2[3]	158[1]	C14[1]	I/O	**P0[9] —** General purpose digital input/output pin.
			I/O	**I2STX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.[2]
			O	**LCDVD[17] —** LCD data.[2]
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
			O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	98[1]	T15[1]	I/O	**P0[10] —** General purpose digital input/output pin.
			O	**TXD2 —** Transmitter output for UART2.
			I/O	**SDA2 —** I^2C2 data input/output (this is not an open-drain pin).
			O	**MAT3[0] —** Match output for Timer 3, channel 0.
P0[11]/RXD2/ SCL2/MAT3[1]	100[1]	R14[1]	I/O	**P0[11] —** General purpose digital input/output pin.
			I	**RXD2 —** Receiver input for UART2.
			I/O	**SCL2 —** I^2C2 clock input/output (this is not an open-drain pin).
			O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[12]/ USB_PPWR2/ MISO1/AD0[6]	41[3]	R1[3]	I/O	**P0[12] —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			I	**AD0[6] —** A/D converter 0, input 6.
P0[13]/ USB_UP_LED2/ MOSI1/AD0[7]	45[3]	R2[3]	I/O	**P0[13] —** General purpose digital input/output pin.
			O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus.
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
			I	**AD0[7] —** A/D converter 0, input 7.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[24]/ USB_RX_DM1/ LCDVD[10]/ LCDVD[14]/ PWM1[5]/MOSI0	78[1]	T9[1]	I/O	**P1[24] —** General purpose digital input/output pin.
			I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).[7]
			O	**LCDVD[10]/LCDVD[14] —** LCD data.[7]
			O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
			I/O	**MOSI0 —** Master Out Slave in for SSP0.
P1[25]/$\overline{\text{USB\_LS1}}$/ LCDVD[11]/ $\overline{\text{LCDVD[15]}}$/ $\overline{\text{USB\_HSTEN1}}$/ MAT1[1]	80[1]	T10[1]	I/O	**P1[25] —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_LS1}}$ —** Low Speed status for USB port 1 (OTG transceiver).[7]
			O	**LCDVD[11]/$\overline{\text{LCDVD[15]}}$ —** LCD data.[7]
			O	**$\overline{\text{USB\_HSTEN1}}$ —** Host Enabled status for USB port 1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
$\overline{\text{P1[26]}}$/ $\overline{\text{USB\_SSPND1}}$/ LCDVD[12]/ LCDVD[20]/ PWM1[6]/CAP0[0]	82[1]	R10[1]	I/O	**$\overline{\text{P1[26]}}$ —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_SSPND1}}$ —** USB port 1 Bus Suspend status (OTG transceiver).[7]
			O	**LCDVD[12]/LCDVD[20] —** LCD data.[7]
			O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[27]/$\overline{\text{USB\_INT1}}$/ LCDVD[13]/ $\overline{\text{LCDVD[21]}}$/ $\overline{\text{USB\_OVRCR1}}$/ CAP0[1]	88[1]	T12[1]	I/O	**P1[27] —** General purpose digital input/output pin.
			I	**$\overline{\text{USB\_INT1}}$ —** USB port 1 OTG transceiver interrupt (OTG transceiver).[7]
			O	**LCDVD[13]/LCDVD[21] —** LCD data.[7]
			I	**$\overline{\text{USB\_OVRCR1}}$ —** USB port 1 Over-Current status.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P1[28]/USB_SCL1/ LCDVD[14]/ LCDVD[22]/ PCAP1[0]/MAT0[0]	90[1]	T13[1]	I/O	**P1[28] —** General purpose digital input/output pin.
			I/O	**USB_SCL1 —** USB port 1 I^2C serial clock (OTG transceiver).[7]
			O	**LCDVD[14]/LCDVD[22] —** LCD data.[7]
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/USB_SDA1/ LCDVD[15]/ LCDVD[23]/ PCAP1[1]/MAT0[1]	92[1]	U14[1]	I/O	**P1[29] —** General purpose digital input/output pin.
			I/O	**USB_SDA1 —** USB port 1 I^2C serial data (OTG transceiver).[7]
			O	**LCDVD[15]/LCDVD[23] —** LCD data.[7]
			I	**PCAP1[1] —** Capture input for PWM1, channel 1.
			O	**MAT0[1] —** Match output for Timer 0, channel 0.
P1[30]/ USB_PWRD2/ V_{BUS}/AD0[4]	42[3]	P2[3]	I/O	**P1[30] —** General purpose digital input/output pin.
			I	**USB_PWRD2 —** Power Status for USB port 2.
			I	**V_{BUS} —** Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
			I	**AD0[4] —** A/D converter 0, input 4.
$\overline{\text{P1[31]}}$/ $\overline{\text{USB\_OVRCR2}}$/ SCK1/AD0[5]	40[3]	P1[3]	I/O	**$\overline{\text{P1[31]}}$ —** General purpose digital input/output pin.
			I	**$\overline{\text{USB\_OVRCR2}}$ —** Over-Current status for USB port 2.
			I/O	**SCK1 —** Serial Clock for SSP1.
			I	**AD0[5] —** A/D converter 0, input 5.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P2[14]/$\overline{\text{CS2}}$/ CAP2[0]/SDA1	91[9]	R12[9]	I/O	**P2[14] —** General purpose digital input/output pin.
			O	**$\overline{\text{CS2}}$ —** LOW active Chip Select 2 signal.
			I	**CAP2[0] —** Capture input for Timer 2, channel 0.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P2[15]/$\overline{\text{CS3}}$/ CAP2[1]/SCL1	99[9]	P13[9]	I/O	**P2[15] —** General purpose digital input/output pin.
			O	**$\overline{\text{CS3}}$ —** LOW active Chip Select 3 signal.
			I	**CAP2[1] —** Capture input for Timer 2, channel 1.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P2[16]/$\overline{\text{CAS}}$	87[1]	R11[1]	I/O	**P2[16] —** General purpose digital input/output pin.
			O	**$\overline{\text{CAS}}$ —** LOW active SDRAM Column Address Strobe.
P2[17]/$\overline{\text{RAS}}$	95[1]	R13[1]	I/O	**P2[17] —** General purpose digital input/output pin.
			O	**$\overline{\text{RAS}}$ —** LOW active SDRAM Row Address Strobe.
P2[18]/ CLKOUT0	59[1]	U3[1]	I/O	**P2[18] —** General purpose digital input/output pin.
			O	**CLKOUT0 —** SDRAM clock 0.
P2[19]/ CLKOUT1	67[1]	R7[1]	I/O	**P2[19] —** General purpose digital input/output pin.
			O	**CLKOUT1 —** SDRAM clock 1.
P2[20]/$\overline{\text{DYCS0}}$	73[1]	T8[1]	I/O	**P2[20] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS0}}$ —** SDRAM chip select 0.
P2[21]/$\overline{\text{DYCS1}}$	81[1]	U11[1]	I/O	**P2[21] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS1}}$ —** SDRAM chip select 1.
P2[22]/$\overline{\text{DYCS2}}$/ CAP3[0]/SCK0	85[1]	U12[1]	I/O	**P2[22] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS2}}$ —** SDRAM chip select 2.
			I	**CAP3[0] —** Capture input for Timer 3, channel 0.
			I/O	**SCK0 —** Serial clock for SSP0.
P2[23]/$\overline{\text{DYCS3}}$/ CAP3[1]/SSEL0	64[1]	U5[1]	I/O	**P2[23] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS3}}$ —** SDRAM chip select 3.
			I	**CAP3[1] —** Capture input for Timer 3, channel 1.
			I/O	**SSEL0 —** Slave Select for SSP0.
P2[24]/ CKEOUT0	53[1]	P5[1]	I/O	**P2[24] —** General purpose digital input/output pin.
			O	**CKEOUT0 —** SDRAM clock enable 0.
P2[25]/ CKEOUT1	54[1]	R4[1]	I/O	**P2[25] —** General purpose digital input/output pin.
			O	**CKEOUT1 —** SDRAM clock enable 1.
P2[26]/ CKEOUT2/ MAT3[0]/MISO0	57[1]	T4[1]	I/O	**P2[26] —** General purpose digital input/output pin.
			O	**CKEOUT2 —** SDRAM clock enable 2.
			O	**MAT3[0] —** Match output for Timer 3, channel 0.
			I/O	**MISO0 —** Master In Slave Out for SSP0.
P2[27]/ CKEOUT3/ MAT3[1]/MOSI0	47[1]	P3[1]	I/O	**P2[27] —** General purpose digital input/output pin.
			O	**CKEOUT3 —** SDRAM clock enable 3.
			O	**MAT3[1] —** Match output for Timer 3, channel 1.
			I/O	**MOSI0 —** Master Out Slave In for SSP0.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P4[1]/A1	79[1]	U10[1]	I/O	**P4[1] —** General purpose digital input/output pin.
			I/O	**A1 —** External memory address line 1.
P4[2]/A2	83[1]	T11[1]	I/O	**P4[2] —** General purpose digital input/output pin.
			I/O	**A2 —** External memory address line 2.
P4[3]/A3	97[1]	U16[1]	I/O	**P4[3] —** General purpose digital input/output pin.
			I/O	**A3 —** External memory address line 3.
P4[4]/A4	103[1]	R15[1]	I/O	**P4[4] —** General purpose digital input/output pin.
			I/O	**A4 —** External memory address line 4.
P4[5]/A5	107[1]	R16[1]	I/O	**P4[5] —** General purpose digital input/output pin.
			I/O	**A5 —** External memory address line 5.
P4[6]/A6	113[1]	M14[1]	I/O	**P4[6] —** General purpose digital input/output pin.
			I/O	**A6 —** External memory address line 6.
P4[7]/A7	121[1]	L16[1]	I/O	**P4[7] —** General purpose digital input/output pin.
			I/O	**A7 —** External memory address line 7.
P4[8]/A8	127[1]	J17[1]	I/O	**P4[8] —** General purpose digital input/output pin.
			I/O	**A8 —** External memory address line 8.
P4[9]/A9	131[1]	H17[1]	I/O	**P4[9] —** General purpose digital input/output pin.
			I/O	**A9 —** External memory address line 9.
P4[10]/A10	135[1]	G17[1]	I/O	**P4[10] —** General purpose digital input/output pin.
			I/O	**A10 —** External memory address line 10.
P4[11]/A11	145[1]	F14[1]	I/O	**P4[11] —** General purpose digital input/output pin.
			I/O	**A11 —** External memory address line 11.
P4[12]/A12	149[1]	C16[1]	I/O	**P4[12] —** General purpose digital input/output pin.
			I/O	**A12 —** External memory address line 12.
P4[13]/A13	155[1]	B16[1]	I/O	**P4[13] —** General purpose digital input/output pin.
			I/O	**A13 —** External memory address line 13.
P4[14]/A14	159[1]	B15[1]	I/O	**P4[14] —** General purpose digital input/output pin.
			I/O	**A14 —** External memory address line 14.
P4[15]/A15	173[1]	A11[1]	I/O	**P4[15] —** General purpose digital input/output pin.
			I/O	**A15 —** External memory address line 15.
P4[16]/A16	101[1]	U17[1]	I/O	**P4[16] —** General purpose digital input/output pin.
			I/O	**A16 —** External memory address line 16.
P4[17]/A17	104[1]	P14[1]	I/O	**P4[17] —** General purpose digital input/output pin.
			I/O	**A17 —** External memory address line 17.
P4[18]/A18	105[1]	P15[1]	I/O	**P4[18] —** General purpose digital input/output pin.
			I/O	**A18 —** External memory address line 18.
P4[19]/A19	111[1]	P16[1]	I/O	**P4[19] —** General purpose digital input/output pin.
			I/O	**A19 —** External memory address line 19.

7. Functional description

7.1 Architectural overview

The LPC2470 microcontroller consists of an ARM7TDMI-S CPU with emulation support, the ARM7 local bus for closely coupled, high-speed access to the majority of on-chip memory, the AMBA AHB interfacing to high-speed on-chip peripherals and external memory, and the AMBA APB for connection to other on-chip peripheral functions. The microcontroller permanently configures the ARM7TDMI-S processor for little-endian byte order.

The LPC2470 implements two AHBs in order to allow the Ethernet block to operate without interference caused by other system activity. The primary AHB, referred to as AHB1, includes the VIC, GPDMA controller, and EMC.

The second AHB, referred to as AHB2, includes only the Ethernet block and an associated 16 kB SRAM. In addition, a bus bridge is provided that allows the secondary AHB to be a bus master on AHB1, allowing expansion of Ethernet buffer space into off-chip memory or unused space in memory residing on AHB1.

In summary, bus masters with access to AHB1 are the ARM7 itself, the GPDMA function, and the Ethernet block (via the bus bridge from AHB2). Bus masters with access to AHB2 are the ARM7 and the Ethernet block.

AHB peripherals are allocated a 2 MB range of addresses at the very top of the 4 GB ARM memory space. Each AHB peripheral is allocated a 16 kB address space within the AHB address space. Lower speed peripheral functions are connected to the APB. The AHB to APB bridge interfaces the APB to the AHB. APB peripherals are also allocated a 2 MB range of addresses, beginning at the 3.5 GB address point. Each APB peripheral is allocated a 16 kB address space within the APB address space.

The ARM7TDMI-S processor is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed complex instruction set computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- the standard 32-bit ARM set
- a 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach higher density compared to standard ARM code while retaining most of the ARM's performance.

7.2 On-chip SRAM

The LPC2470 includes a SRAM memory of 64 kB reserved for the ARM processor exclusive use. This RAM may be used for code and/or data storage and may be accessed as 8 bits, 16 bits, and 32 bits.

A 16 kB SRAM block serving as a buffer for the Ethernet controller and a 16 kB SRAM associated with the second AHB can be used both for data and code storage, too. The 2 kB RTC SRAM can be used for data storage only. The RTC SRAM is battery powered and retains the content in the absence of the main power supply.

7.3 Memory map

The LPC2470 memory map incorporates several distinct regions as shown in Table 5 and Figure 4.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either boot ROM or SRAM (see Section 7.26.6).

Table 5. LPC2470 memory usage and details

Address range	General use	Address range details and description	
0x0000 0000 to 0x3FFF FFFF	Fast I/O	0x3FFF C000 - 0x3FFF FFFF	Fast GPIO registers
0x4000 0000 to 0x7FFF FFFF	On-chip RAM	0x4000 0000 - 0x4000 FFFF	RAM (64 kB)
		0x7FE0 0000 - 0x7FE0 3FFF	Ethernet RAM (16 kB)
		0x7FD0 0000 - 0x7FD0 3FFF	USB RAM (16 kB)
0x8000 0000 to 0xDFFF FFFF	Off-Chip Memory	Four static memory banks, 16 MB each	
		0x8000 0000 - 0x80FF FFFF	Static memory bank 0
		0x8100 0000 - 0x81FF FFFF	Static memory bank 1
		0x8200 0000 - 0x82FF FFFF	Static memory bank 2
		0x8300 0000 - 0x83FF FFFF	Static memory bank 3
		Four dynamic memory banks, 256 MB each	
		0xA000 0000 - 0xAFFF FFFF	Dynamic memory bank 0
		0xB000 0000 - 0xBFFF FFFF	Dynamic memory bank 1
		0xC000 0000 - 0xCFFF FFFF	Dynamic memory bank 2
		0xD000 0000 - 0xDFFF FFFF	Dynamic memory bank 3
0xE000 0000 to 0xEFFF FFFF	APB Peripherals	36 peripheral blocks, 16 kB each	
0xF000 0000 to 0xFFFF FFFF	AHB peripherals		

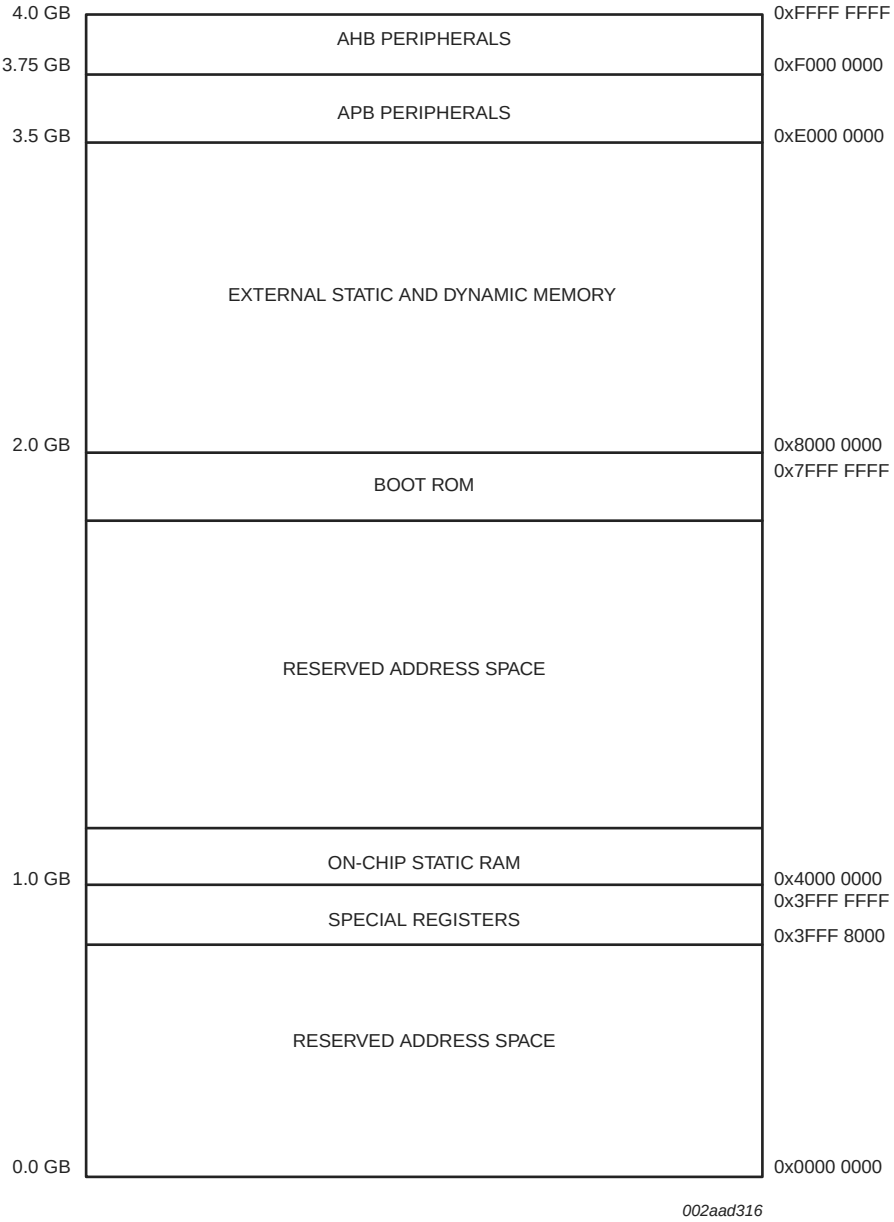


Fig 4. LPC2470 memory map

7.4 Interrupt controller

The ARM processor core has two interrupt inputs called Interrupt ReQuest (IRQ) and Fast Interrupt ReQuest (FIQ). The VIC takes 32 interrupt request inputs which can be programmed as FIQ or vectored IRQ types. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQs have the highest priority. If more than one request is assigned to FIQ, the VIC ORs the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ

- Asynchronous page mode read
- Programmable Wait States
- Bus turnaround delay
- Output enable and write enable delays
- Extended wait

- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control CKE and CLKOUT to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048, 4096, and 8192 row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.7 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected LPC2470 peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master.

7.7.1 Features

- Two DMA channels. Each channel can support a unidirectional transfer.
- The GPDMA can transfer data between the 16 kB SRAM, external memory, and peripherals such as the SD/MMC, two SSPs, and the I^2S interface.
- Single DMA and burst DMA request signals. Each peripheral connected to the GPDMA can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the GPDMA.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority. Each DMA channel has a specific hardware priority. DMA channel 0 has the highest priority and channel 1 has the lowest priority. If requests from two channels become active at the same time, the channel with the highest priority is serviced first.
- AHB slave DMA programming interface. The GPDMA is programmed by writing to the DMA control registers over the AHB slave interface.

7.11.3 USB OTG controller

USB OTG is a supplement to the *USB 2.0 specification* that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG controller integrates the host controller, device controller, and a master-only I^2C interface to implement OTG dual-role device functionality. The dedicated I^2C interface controls an external OTG transceiver.

7.11.3.1 Features

- Fully compliant with On-The-Go supplement to the *USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

7.12 CAN controller and acceptance filters

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.12.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

- UART3 includes an IrDA mode to support infrared communication.

7.16 SPI serial I/O controller

The LPC2470 contains one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

7.16.1 Features

- Compliant with SPI specification
- Synchronous, Serial, Full Duplex Communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

7.17 SSP serial I/O controller

The LPC2470 contains two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.17.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Maximum SPI bus data bit rate of one half (Master mode) and one twelfth (Slave mode) of the input clock rate
- DMA transfers supported by GPDMA

7.18 SD/MMC card interface

The Secure Digital and Multimedia Card Interface (MCI) allows access to external SD memory cards. The SD card interface conforms to the *SD Multimedia Card Specification Version 2.11*.

7.18.1 Features

- The MCI provides all functions specific to the SD/MMC memory card. These include the clock generation unit, power management control, and command and data transfer.

- Conforms to *Multimedia Card Specification v2.11*.
- Conforms to *Secure Digital Memory Card Physical Layer Specification, v0.96.*
- Can be used as a multimedia card bus or a secure digital memory card bus host. The SD/MMC can be connected to several multimedia cards or a single secure digital memory card.
- DMA supported through the GPDMA controller.

7.19 I²C-bus serial I/O controller

The LPC2470 contains three I²C-bus controllers.

The I²C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial Data Line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C-bus is a multi-master bus and can be controlled by more than one bus master connected to it.

The I²C-bus implemented in LPC2470 supports bit rates up to 400 kbit/s (Fast I²C-bus).

7.19.1 Features

- I²C0 is a standard I²C compliant bus interface with open-drain pins.
- I²C1 and I²C2 use standard I/O pins and do not support powering off of individual devices connected to the same bus lines.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.

7.20 I²S-bus serial I/O controllers

The I²S-bus provides a standard communication interface for digital audio applications.

The I²*S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S connection has one master, which is always the master, and one slave. The I²S interface on the LPC2470 provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.25.4 Power control

The LPC2470 supports a variety of power control features. There are four special modes of processor power reduction: Idle mode, Sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The LPC2470 also implements a separate power domain in order to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small SRAM, referred to as the Battery RAM.

7.25.4.1 Idle mode

In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.25.4.2 Sleep mode

In Sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later. The 32 kHz RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The CCLK and USB clock dividers automatically get reset to zero.

The Sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Sleep mode reduces chip power consumption to a very low value.

On the wake-up from Sleep mode, if the IRC was used before entering Sleep mode, the code execution and peripherals activities will resume after 4 cycles expire. If the main external oscillator was used, the code execution will resume when 4096 cycles expire.

The customers need to reconfigure the PLL and clock dividers accordingly.

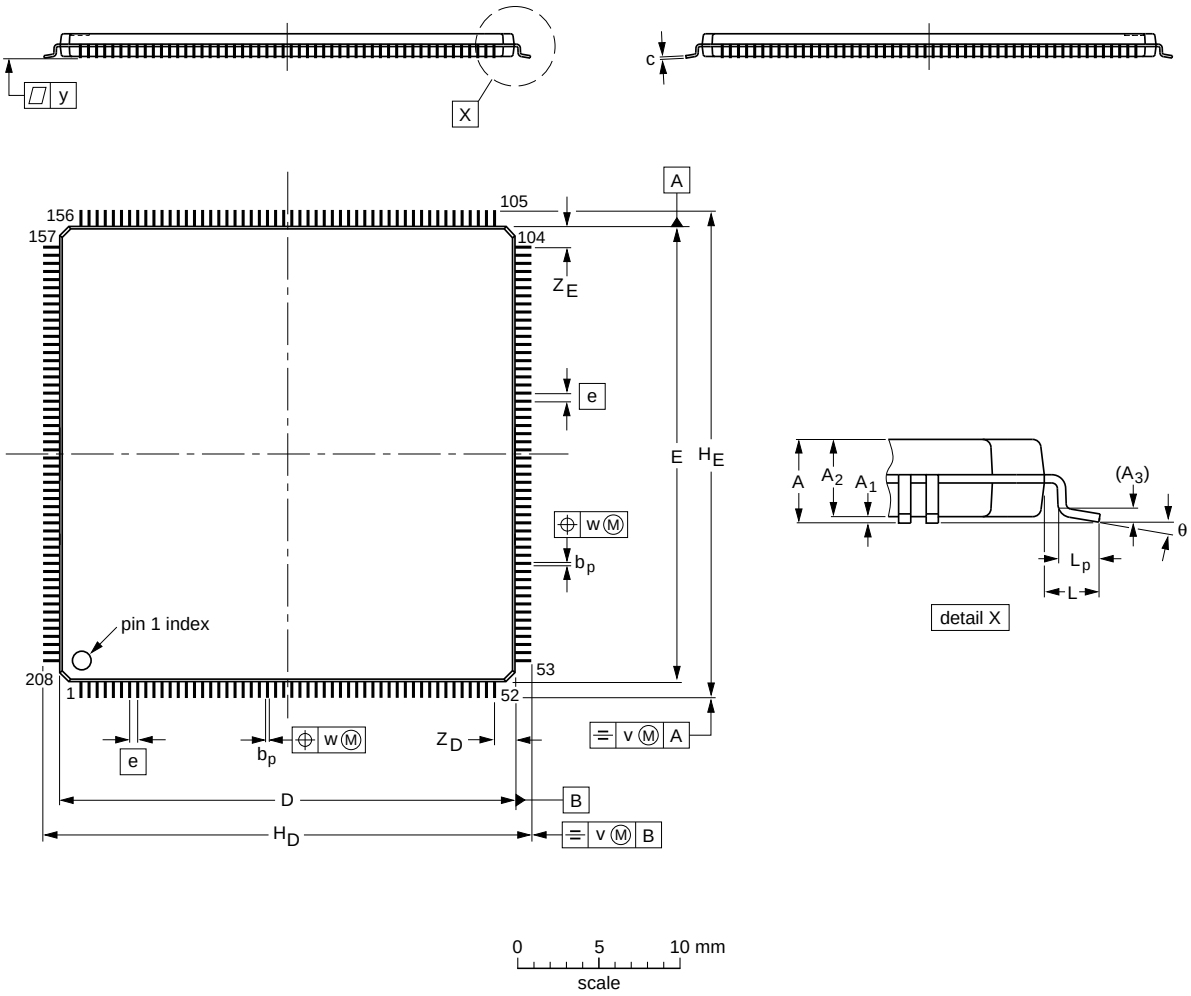
7.25.4.3 Power-down mode

Power-down mode does everything that Sleep mode does but also turns off the IRC oscillator.

On the wake-up from Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. The customers need to reconfigure the PLL and clock dividers accordingly after a wake-up from Power-down mode.

15. Package outline

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

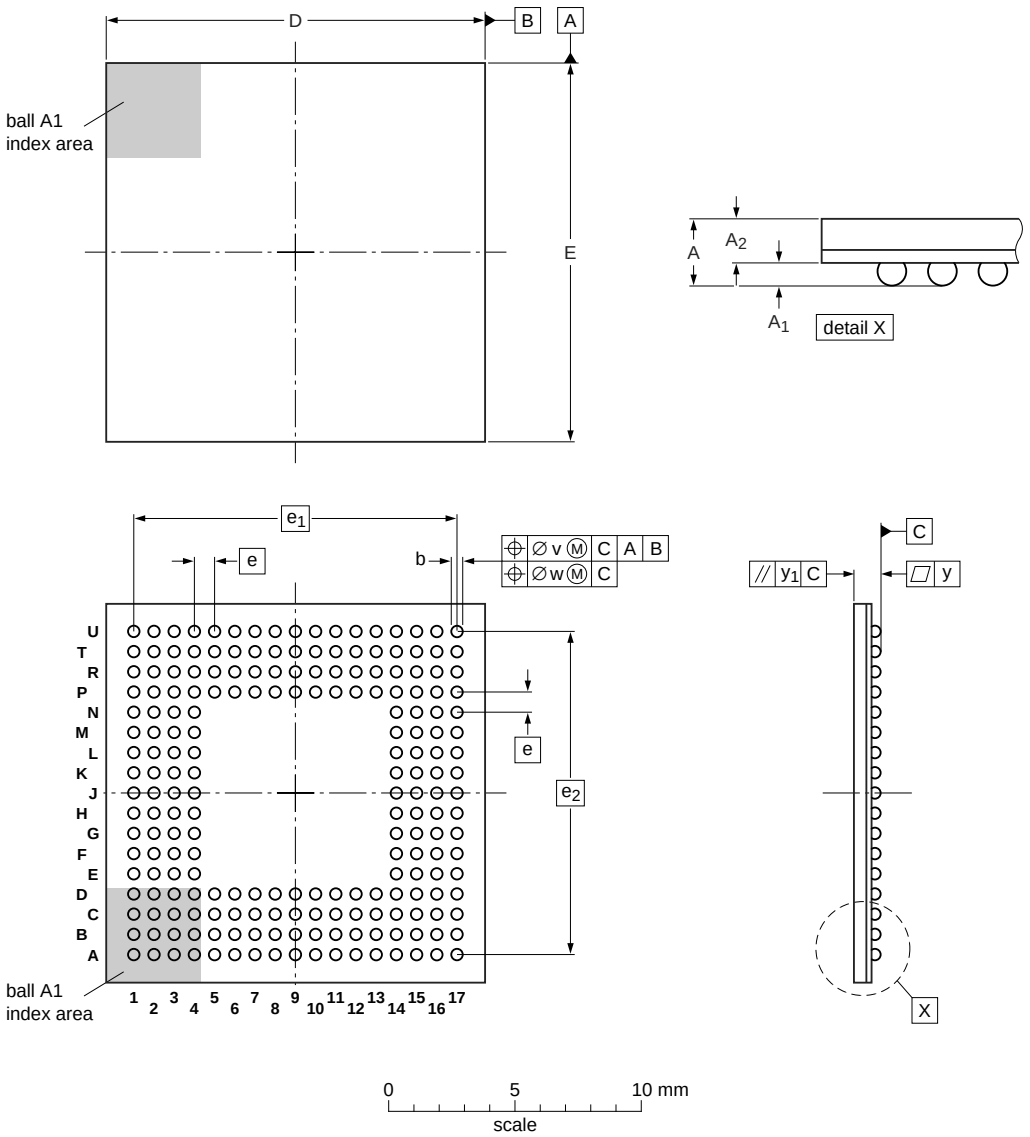
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 34. Package outline SOT459-1 (LQFP208)

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 15 x 15 x 0.7 mm **SOT950-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.6	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT950-1		- - -				~~06-06-01~~ 06-06-14

Fig 35. Package outline SOT950-1 (TFBGA208)

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

20. Contents

continued >>