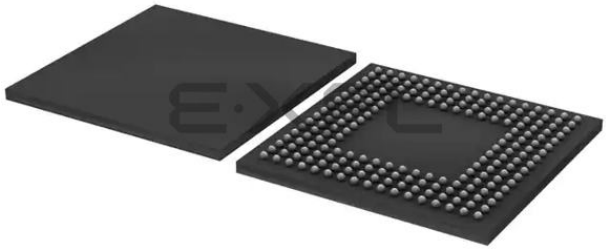

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	160
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	98K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2470fet208-551

- Each peripheral has its own clock divider for further power saving. These dividers help reduce active power by 20 % to 30 %.
- Brownout detect with separate thresholds for interrupt and forced reset.
- On-chip power-on reset.
- On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Boundary scan for simplified board testing.
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace module supports real-time trace.

3. Applications

- Industrial control
- Medical systems
- Portable electronics
- Point-of-Sale (POS) equipment

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2470FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC2470FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					External bus	Ethernet	USB OTG/ OHCI/ device + 4 kB FIFO	CAN channels	SD/ MMC	GP DMA	ADC channels	DAC channels	Temp range
		Local bus	Ethernet buffer	GP/USB	RTC	Total									
LPC2470FBD208	n/a	64	16	16	2	98	Full 32-bit	MII/RMII	yes	2	yes	yes	8	1	−40 °C to +85 °C
LPC2470FET208	n/a	64	16	16	2	98	Full 32-bit	MII/RMII	yes	2	yes	yes	8	1	−40 °C to +85 °C

6. Pinning information

6.1 Pinning

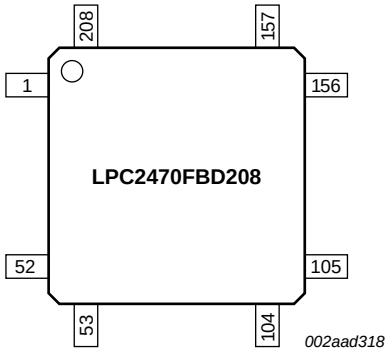


Fig 2. LPC2470 pinning LQFP208 package

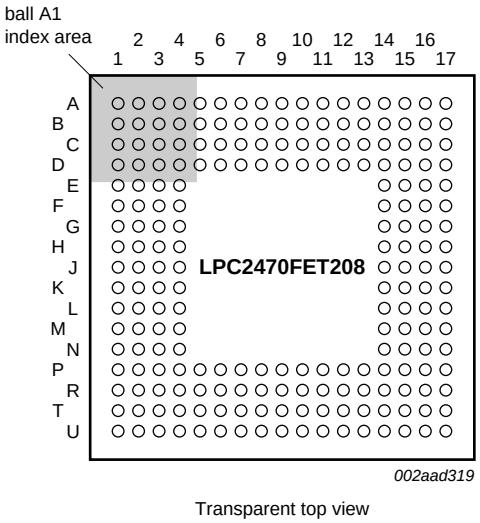


Fig 3. LPC2470 pinning TFBGA208 package

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	P3[27]/D27/ CAP1[0]/PWM1[4]	2	V_{SSIO}	3	P1[0]/ENET_TXD0	4	P4[31]/$\overline{CS1}$
5	P1[4]/ENET_TX_EN	6	P1[9]/ENET_RXD0	7	P1[14]/ENET_RX_ER	8	P1[15]/ ENET_REF_CLK/ ENET_RX_CLK
9	P1[17]/ENET_MDIO	10	P1[3]/ENET_TXD3/ MCICMD/PWM0[2]	11	P4[15]/A15	12	V_{SSIO}

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P0[14]/ USB_HSTEN2/ USB_CONNECT2/ SSEL1	69[1]	T7[1]	I/O	**P0[14] —** General purpose digital input/output pin.
			O	**USB_HSTEN2 —** Host Enabled status for USB port 2.
			O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
			I/O	**SSEL1 —** Slave Select for SSP1.
P0[15]/TXD1/ SCK0/SCK	128[1]	J16[1]	I/O	**P0[15] —** General purpose digital input/output pin.
			O	**TXD1 —** Transmitter output for UART1.
			I/O	**SCK0 —** Serial clock for SSP0.
			I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	130[1]	J14[1]	I/O	**P0[16] —** General purpose digital input/output pin.
			I	**RXD1 —** Receiver input for UART1.
			I/O	**SSEL0 —** Slave Select for SSP0.
			I/O	**SSEL —** Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	126[1]	K17[1]	I/O	**P0[17] —** General purpose digital input/output pin.
			I	**CTS1 —** Clear to Send input for UART1.
			I/O	**MISO0 —** Master In Slave Out for SSP0.
			I/O	**MISO —** Master In Slave Out for SPI.
P0[18]/DCD1/ MOSI0/MOSI	124[1]	K15[1]	I/O	**P0[18] —** General purpose digital input/output pin.
			I	**DCD1 —** Data Carrier Detect input for UART1.
			I/O	**MOSI0 —** Master Out Slave In for SSP0.
			I/O	**MOSI —** Master Out Slave In for SPI.
P0[19]/DSR1/ MCICLK/SDA1	122[1]	L17[1]	I/O	**P0[19] —** General purpose digital input/output pin.
			I	**DSR1 —** Data Set Ready input for UART1.
			O	**MCICLK —** Clock output line for SD/MMC interface.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[20]/DTR1/ MCICMD/SCL1	120[1]	M17[1]	I/O	**P0[20] —** General purpose digital input/output pin.
			O	**DTR1 —** Data Terminal Ready output for UART1.
			I/O	**MCICMD —** Command line for SD/MMC interface.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[21]/RI1/ MCIPWR/RD1	118[1]	M16[1]	I/O	**P0[21] —** General purpose digital input/output pin.
			I	**RI1 —** Ring Indicator input for UART1.
			O	**MCIPWR —** Power Supply Enable for external SD/MMC power supply.
			I	**RD1 —** CAN1 receiver input.
P0[22]/RTS1/ MCIDAT0/TD1	116[1]	N17[1]	I/O	**P0[22] —** General purpose digital input/output pin.
			O	**RTS1 —** Request to Send output for UART1.
			I/O	**MCIDAT0 —** Data line 0 for SD/MMC interface.
			O	**TD1 —** CAN1 transmitter output.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[3]/ ENET_TXD3/ MCICMD/ PWM0[2]	177[1]	A10[1]	I/O	**P1[3] —** General purpose digital input/output pin.
			O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
			I/O	**MCICMD —** Command line for SD/MMC interface.
			O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
P1[4]/ ENET_TX_EN	192[1]	A5[1]	I/O	**P1[4] —** General purpose digital input/output pin.
			O	**ENET_TX_EN —** Ethernet transmit data enable (RMII/MII interface).
P1[5]/ ENET_TX_ER/ MCIPWR/ PWM0[3]	156[1]	A17[1]	I/O	**P1[5] —** General purpose digital input/output pin.
			O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
			O	**MCIPWR —** Power Supply Enable for external SD/MMC power supply.
			O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
P1[6]/ ENET_TX_CLK/ MCIDAT0/ PWM0[4]	171[1]	B11[1]	I/O	**P1[6] —** General purpose digital input/output pin.
			I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
			I/O	**MCIDAT0 —** Data line 0 for SD/MMC interface.
			O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
P1[7]/ ENET_COL/ MCIDAT1/ PWM0[5]	153[1]	D14[1]	I/O	**P1[7] —** General purpose digital input/output pin.
			I	**ENET_COL —** Ethernet Collision detect (MII interface).
			I/O	**MCIDAT1 —** Data line 1 for SD/MMC interface.
			O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
P1[8]/ ENET_CRS_DV/ ENET_CRS	190[1]	C7[1]	I/O	**P1[8] —** General purpose digital input/output pin.
			I	**ENET_CRS_DV/ENET_CRS —** Ethernet Carrier Sense/Data Valid (RMII interface)/ Ethernet Carrier Sense (MII interface).
P1[9]/ ENET_RXD0	188[1]	A6[1]	I/O	**P1[9] —** General purpose digital input/output pin.
			I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
P1[10]/ ENET_RXD1	186[1]	C8[1]	I/O	**P1[10] —** General purpose digital input/output pin.
			I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
P1[11]/ ENET_RXD2/ MCIDAT2/ PWM0[6]	163[1]	A14[1]	I/O	**P1[11] —** General purpose digital input/output pin.
			I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
			I/O	**MCIDAT2 —** Data line 2 for SD/MMC interface.
			O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]/ ENET_RXD3/ MCIDAT3/ PCAP0[0]	157[1]	A16[1]	I/O	**P1[12] —** General purpose digital input/output pin.
			I	**ENET_RXD3 —** Ethernet Receive Data (MII interface).
			I/O	**MCIDAT3 —** Data line 3 for SD/MMC interface.
			I	**PCAP0[0] —** Capture input for PWM0, channel 0.
P1[13]/ ENET_RX_DV	147[1]	D16[1]	I/O	**P1[13] —** General purpose digital input/output pin.
			I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).
P1[14]/ ENET_RX_ER	184[1]	A7[1]	I/O	**P1[14] —** General purpose digital input/output pin.
			I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
P1[15]/ ENET_REF_CLK/ ENET_RX_CLK	182[1]	A8[1]	I/O	**P1[15] —** General purpose digital input/output pin.
			I	**ENET_REF_CLK/ENET_RX_CLK —** Ethernet Reference Clock (RMII interface)/ Ethernet Receive Clock (MII interface).

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[24]/ USB_RX_DM1/ LCDVD[10]/ LCDVD[14]/ PWM1[5]/MOSI0	78[1]	T9[1]	I/O	**P1[24] —** General purpose digital input/output pin.
			I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).[7]
			O	**LCDVD[10]/LCDVD[14] —** LCD data.[7]
			O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
			I/O	**MOSI0 —** Master Out Slave in for SSP0.
P1[25]/$\overline{\text{USB\_LS1}}$/ LCDVD[11]/ $\overline{\text{LCDVD[15]}}$/ $\overline{\text{USB\_HSTEN1}}$/ MAT1[1]	80[1]	T10[1]	I/O	**P1[25] —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_LS1}}$ —** Low Speed status for USB port 1 (OTG transceiver).[7]
			O	**LCDVD[11]/$\overline{\text{LCDVD[15]}}$ —** LCD data.[7]
			O	**$\overline{\text{USB\_HSTEN1}}$ —** Host Enabled status for USB port 1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
$\overline{\text{P1[26]}}$/ $\overline{\text{USB\_SSPND1}}$/ LCDVD[12]/ LCDVD[20]/ PWM1[6]/CAP0[0]	82[1]	R10[1]	I/O	**$\overline{\text{P1[26]}}$ —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_SSPND1}}$ —** USB port 1 Bus Suspend status (OTG transceiver).[7]
			O	**LCDVD[12]/LCDVD[20] —** LCD data.[7]
			O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[27]/$\overline{\text{USB\_INT1}}$/ LCDVD[13]/ $\overline{\text{LCDVD[21]}}$/ $\overline{\text{USB\_OVRCR1}}$/ CAP0[1]	88[1]	T12[1]	I/O	**P1[27] —** General purpose digital input/output pin.
			I	**$\overline{\text{USB\_INT1}}$ —** USB port 1 OTG transceiver interrupt (OTG transceiver).[7]
			O	**LCDVD[13]/LCDVD[21] —** LCD data.[7]
			I	**$\overline{\text{USB\_OVRCR1}}$ —** USB port 1 Over-Current status.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P1[28]/USB_SCL1/ LCDVD[14]/ LCDVD[22]/ PCAP1[0]/MAT0[0]	90[1]	T13[1]	I/O	**P1[28] —** General purpose digital input/output pin.
			I/O	**USB_SCL1 —** USB port 1 I^2C serial clock (OTG transceiver).[7]
			O	**LCDVD[14]/LCDVD[22] —** LCD data.[7]
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/USB_SDA1/ LCDVD[15]/ LCDVD[23]/ PCAP1[1]/MAT0[1]	92[1]	U14[1]	I/O	**P1[29] —** General purpose digital input/output pin.
			I/O	**USB_SDA1 —** USB port 1 I^2C serial data (OTG transceiver).[7]
			O	**LCDVD[15]/LCDVD[23] —** LCD data.[7]
			I	**PCAP1[1] —** Capture input for PWM1, channel 1.
			O	**MAT0[1] —** Match output for Timer 0, channel 0.
P1[30]/ USB_PWRD2/ V_{BUS}/AD0[4]	42[3]	P2[3]	I/O	**P1[30] —** General purpose digital input/output pin.
			I	**USB_PWRD2 —** Power Status for USB port 2.
			I	**V_{BUS} —** Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
			I	**AD0[4] —** A/D converter 0, input 4.
$\overline{\text{P1[31]}}$/ $\overline{\text{USB\_OVRCR2}}$/ SCK1/AD0[5]	40[3]	P1[3]	I/O	**$\overline{\text{P1[31]}}$ —** General purpose digital input/output pin.
			I	**$\overline{\text{USB\_OVRCR2}}$ —** Over-Current status for USB port 2.
			I/O	**SCK1 —** Serial Clock for SSP1.
			I	**AD0[5] —** A/D converter 0, input 5.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P2[14]/$\overline{\text{CS2}}$/ CAP2[0]/SDA1	91[9]	R12[9]	I/O	**P2[14] —** General purpose digital input/output pin.
			O	**$\overline{\text{CS2}}$ —** LOW active Chip Select 2 signal.
			I	**CAP2[0] —** Capture input for Timer 2, channel 0.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P2[15]/$\overline{\text{CS3}}$/ CAP2[1]/SCL1	99[9]	P13[9]	I/O	**P2[15] —** General purpose digital input/output pin.
			O	**$\overline{\text{CS3}}$ —** LOW active Chip Select 3 signal.
			I	**CAP2[1] —** Capture input for Timer 2, channel 1.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P2[16]/$\overline{\text{CAS}}$	87[1]	R11[1]	I/O	**P2[16] —** General purpose digital input/output pin.
			O	**$\overline{\text{CAS}}$ —** LOW active SDRAM Column Address Strobe.
P2[17]/$\overline{\text{RAS}}$	95[1]	R13[1]	I/O	**P2[17] —** General purpose digital input/output pin.
			O	**$\overline{\text{RAS}}$ —** LOW active SDRAM Row Address Strobe.
P2[18]/ CLKOUT0	59[1]	U3[1]	I/O	**P2[18] —** General purpose digital input/output pin.
			O	**CLKOUT0 —** SDRAM clock 0.
P2[19]/ CLKOUT1	67[1]	R7[1]	I/O	**P2[19] —** General purpose digital input/output pin.
			O	**CLKOUT1 —** SDRAM clock 1.
P2[20]/$\overline{\text{DYCS0}}$	73[1]	T8[1]	I/O	**P2[20] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS0}}$ —** SDRAM chip select 0.
P2[21]/$\overline{\text{DYCS1}}$	81[1]	U11[1]	I/O	**P2[21] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS1}}$ —** SDRAM chip select 1.
P2[22]/$\overline{\text{DYCS2}}$/ CAP3[0]/SCK0	85[1]	U12[1]	I/O	**P2[22] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS2}}$ —** SDRAM chip select 2.
			I	**CAP3[0] —** Capture input for Timer 3, channel 0.
			I/O	**SCK0 —** Serial clock for SSP0.
P2[23]/$\overline{\text{DYCS3}}$/ CAP3[1]/SSEL0	64[1]	U5[1]	I/O	**P2[23] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS3}}$ —** SDRAM chip select 3.
			I	**CAP3[1] —** Capture input for Timer 3, channel 1.
			I/O	**SSEL0 —** Slave Select for SSP0.
P2[24]/ CKEOUT0	53[1]	P5[1]	I/O	**P2[24] —** General purpose digital input/output pin.
			O	**CKEOUT0 —** SDRAM clock enable 0.
P2[25]/ CKEOUT1	54[1]	R4[1]	I/O	**P2[25] —** General purpose digital input/output pin.
			O	**CKEOUT1 —** SDRAM clock enable 1.
P2[26]/ CKEOUT2/ MAT3[0]/MISO0	57[1]	T4[1]	I/O	**P2[26] —** General purpose digital input/output pin.
			O	**CKEOUT2 —** SDRAM clock enable 2.
			O	**MAT3[0] —** Match output for Timer 3, channel 0.
			I/O	**MISO0 —** Master In Slave Out for SSP0.
P2[27]/ CKEOUT3/ MAT3[1]/MOSI0	47[1]	P3[1]	I/O	**P2[27] —** General purpose digital input/output pin.
			O	**CKEOUT3 —** SDRAM clock enable 3.
			O	**MAT3[1] —** Match output for Timer 3, channel 1.
			I/O	**MOSI0 —** Master Out Slave In for SSP0.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P3[13]/D13	7[1]	C1[1]	I/O	**P3[13] —** General purpose digital input/output pin.
			I/O	**D13 —** External memory data line 13.
P3[14]/D14	21[1]	H2[1]	I/O	**P3[14] —** General purpose digital input/output pin.
			I/O	**D14 —** External memory data line 14. On POR, this pin serves as the BOOT0 pin.
P3[15]/D15	28[1]	M1[1]	I/O	**P3[15] —** General purpose digital input/output pin.
			I/O	**D15 —** External memory data line 15. On POR, this pin serves as the BOOT1 pin. BOOT[1:0] = 00 selects 8-bit external memory on $\overline{CS1}$. BOOT[1:0] = 01 is reserved. Do not use. BOOT[1:0] = 10 selects 32-bit external memory on $\overline{CS1}$. BOOT[1:0] = 11 selects 16-bit external memory on $\overline{CS1}$.
P3[16]/D16/ PWM0[1]/TXD1	137[1]	F17[1]	I/O	**P3[16] —** General purpose digital input/output pin.
			I/O	**D16 —** External memory data line 16.
			O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
			O	**TXD1 —** Transmitter output for UART1.
P3[17]/D17/ PWM0[2]/RXD1	143[1]	F15[1]	I/O	**P3[17] —** General purpose digital input/output pin.
			I/O	**D17 —** External memory data line 17.
			O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
			I	**RXD1 —** Receiver input for UART1.
P3[18]/D18/ PWM0[3]/CTS1	151[1]	C15[1]	I/O	**P3[18] —** General purpose digital input/output pin.
			I/O	**D18 —** External memory data line 18.
			O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
			I	**CTS1 —** Clear to Send input for UART1.
P3[19]/D19/ PWM0[4]/DCD1	161[1]	B14[1]	I/O	**P3[19] —** General purpose digital input/output pin.
			I/O	**D19 —** External memory data line 19.
			O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
			I	**DCD1 —** Data Carrier Detect input for UART1.
P3[20]/D20/ PWM0[5]/DSR1	167[1]	A13[1]	I/O	**P3[20] —** General purpose digital input/output pin.
			I/O	**D20 —** External memory data line 20.
			O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
			I	**DSR1 —** Data Set Ready input for UART1.
P3[21]/D21/ PWM0[6]/DTR1	175[1]	C10[1]	I/O	**P3[21] —** General purpose digital input/output pin.
			I/O	**D21 —** External memory data line 21.
			O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
			O	**DTR1 —** Data Terminal Ready output for UART1.
P3[22]/D22/ PCAP0[0]/RI1	195[1]	C6[1]	I/O	**P3[22] —** General purpose digital input/output pin.
			I/O	**D22 —** External memory data line 22.
			I	**PCAP0[0] —** Capture input for PWM0, channel 0.
			I	**RI1 —** Ring Indicator input for UART1.

7.13 10-bit ADC

The LPC2470 contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.13.1 Features

- 10-bit successive approximation ADC
- Input multiplexing among 8 pins
- Power-down mode
- Measurement range 0 V to $V_{i(VREF)}$
- 10-bit conversion time $\geq$ 2.44 μs
- Burst conversion mode for single or multiple inputs
- Optional conversion on transition of input pin or Timer Match signal
- Individual result registers for each ADC channel to reduce interrupt overhead

7.14 10-bit DAC

The DAC allows the LPC2470 to generate a variable analog output. The maximum output value of the DAC is $V_{i(VREF)}$.

7.14.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive

7.15 UARTs

The LPC2470 contains four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.15.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

- UART3 includes an IrDA mode to support infrared communication.

7.16 SPI serial I/O controller

The LPC2470 contains one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

7.16.1 Features

- Compliant with SPI specification
- Synchronous, Serial, Full Duplex Communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

7.17 SSP serial I/O controller

The LPC2470 contains two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.17.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Maximum SPI bus data bit rate of one half (Master mode) and one twelfth (Slave mode) of the input clock rate
- DMA transfers supported by GPDMA

7.18 SD/MMC card interface

The Secure Digital and Multimedia Card Interface (MCI) allows access to external SD memory cards. The SD card interface conforms to the *SD Multimedia Card Specification Version 2.11*.

7.18.1 Features

- The MCI provides all functions specific to the SD/MMC memory card. These include the clock generation unit, power management control, and command and data transfer.

7.20.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I^2S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I^2S input and I^2S output.

7.21 General purpose 32-bit timers/external event counters

The LPC2470 includes four 32-bit Timer/Counters. The Timer/Counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The Timer/Counter also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.21.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit prescaler.
- Counter or Timer operation.
- Up to four 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 7.25.2 for additional information.

7.25.1.3 RTC oscillator

The RTC oscillator can be used as the clock source for the RTC and/or the WDT. Also, the RTC oscillator can be used to drive the PLL and the CPU.

7.25.2 PLL

The PLL accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and the USB block.

The PLL input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value 'N', which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL input divider is the PLL multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value 'M', in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL is enabled by software only. The program must configure and activate the PLL, wait for the PLL to lock, then connect to the PLL as a clock source.

7.25.3 Wake-up timer

The LPC2470 begins operation at power-up and when awakened from Power-down and Deep-power down modes by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down and Deep power-down modes, any wake-up of the processor from Power-down modes makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.25.4.4 Deep power-down mode

Deep power-down mode is similar to the Power-down mode, but now the on-chip regulator that supplies power to the internal logic is also shut off. This produces the lowest possible power consumption without removing power from the entire chip. Since the Deep power-down mode shuts down the on-chip logic power supply, there is no register or memory retention, and resumption of operation involves the same activities as a full chip reset.

If power is supplied to the LPC2470 during Deep power-down mode, wake-up can be caused by the RTC Alarm interrupt or by external Reset.

While in Deep power-down mode, external device power may be removed. In this case, the LPC2470 will start up when external power is restored.

Essential data may be retained through Deep power-down mode (or through complete powering off of the chip) by storing data in the Battery RAM, as long as the external power to the VBAT pin is maintained.

7.25.4.5 Power domains

The LPC2470 provides two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the Battery RAM.

On the LPC2470, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(DCDC)(3V3)}$ pins power the on-chip DC-to-DC converter which in turn provides power to the CPU and most of the peripherals.

Although both the I/O pad ring and the core require a 3.3 V supply, different powering schemes can be used depending on the actual application requirements.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(DCDC)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(DCDC)(3V3)}$). Having the on-chip DC-DC converter powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC and the Battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that may be used by external hardware to restore chip power and resume operation.

7.26 System control

7.26.1 Reset

Reset has four sources on the LPC2470: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset, and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 7. Thermal characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	125	°C

Table 8. Thermal resistance value (C/W): ±15 %

V_{DD} = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C unless otherwise specified;

LQFP208		**TFBGA208**	
θja		**θja**	
JEDEC (4.5 in × 4 in)		**JEDEC (4.5 in × 4 in)**	
0 m/s	27.4	0 m/s	41
1 m/s	25.7	1 m/s	35
2.5 m/s	24.4	2.5 m/s	31
Single-layer (4.5 in × 3 in)		**8-layer (4.5 in × 3 in)**	
0 m/s	35.4	0 m/s	34.9
1 m/s	31.2	1 m/s	30.9
2.5 m/s	29.2	2.5 m/s	28
θjc	8.8	θjc	8.3
θjb	15.4	θjb	13.6

11.4 Static external memory interface

Table 14. Dynamic characteristics: Static external memory interface
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles[1]						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		−0.29	0.20	2.54	ns
Read cycle parameters[1][2]						
t_{OELAV}	$\overline{OE}$ LOW to address valid time		−0.29	0.20	2.54	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		−0.78 + $T_{cy(CCLK)}$ × WAITOEN	0 + $T_{cy(CCLK)}$ × WAITOEN	0.49 + $T_{cy(CCLK)}$ × WAITOEN	ns
t_{am}	memory access time	[3][4]	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 12.70	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 9.57	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 8.11	ns
$t_{h(D)}$	data input hold time	[5]	0	-	-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		−0.49	0	0.20	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		−0.20	0.20	2.44	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		−0.59 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0.10 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	
t_{BLSLAV}	$\overline{BLS}$ LOW to address valid time		−0.39	0	2.54	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time		−0.88	0.49	0.68	ns
Write cycle parameters[1][6]						
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		−0.88 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	0.10 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	0.20 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		−0.88	0.49	0.98	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		0.68	2.54	5.86	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		0	2.64	4.79	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[3]	−0.78 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	0 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	0.10 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[3]	−0.88 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	0 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	0.59 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	[3]	0 + $T_{cy(CCLK)}$	0.20 + $T_{cy(CCLK)}$	2.74 + $T_{cy(CCLK)}$	ns

11.5 Dynamic external memory interface

Table 15. Dynamic characteristics: Dynamic external memory interface

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V, EMC Dynamic Read Config Register = 0x0 (RD = 00)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Common							
$t_{d(SV)}$	chip select valid delay time		[1]	-	1.05	1.76	ns
$t_{h(S)}$	chip select hold time		[1]	0.1	1.02	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		[1]	-	1.51	1.95	ns
$t_{h(RAS)}$	row address strobe hold time		[1]	0.5	1.51	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		[1]	-	0.98	1.27	ns
$t_{h(CAS)}$	column address strobe hold time		[1]	0.1	0.97	-	ns
$t_{d(WV)}$	write valid delay time		[1]	-	0.84	1.95	ns
$t_{h(W)}$	write hold time		[1]	0.1	0.84	-	ns
$t_{d(GV)}$	output enable valid delay time		[1]	-	0.95	1.86	ns
$t_{h(G)}$	output enable hold time		[1]	0.1	1	-	ns
$t_{d(AV)}$	address valid delay time		[1]	-	0.87	1.95	ns
$t_{h(A)}$	address hold time		[1]	0.1	0.81	-	ns
Read cycle parameters							
$t_{su(D)}$	data input set-up time		[1]	0.51	2.24	-	ns
$t_{h(D)}$	data input hold time		[1]	0.57	2.41	-	ns
Write cycle parameters							
$t_{d(QV)}$	data output valid delay time		[1]	-	2.65	4.36	ns
$t_{h(Q)}$	data output hold time		[1]	0.49	2.61	-	ns

[1] See Figure 18.

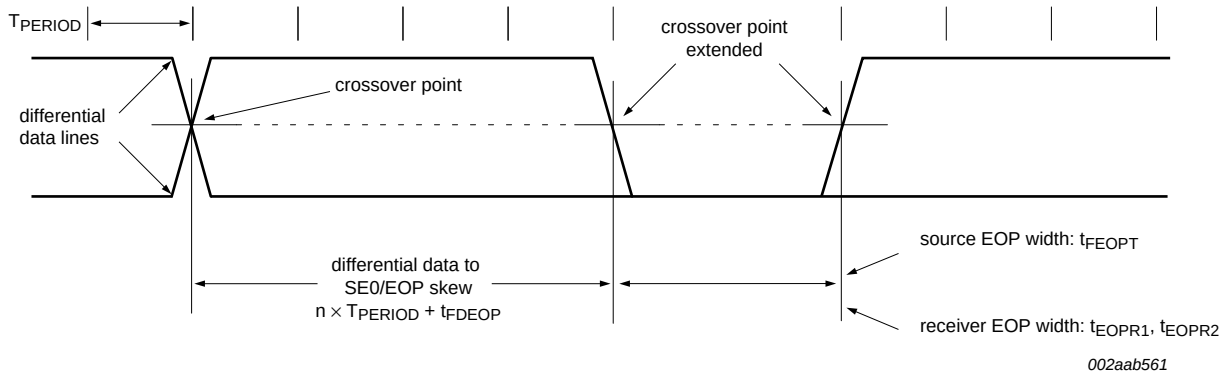


Fig 16. Differential data-to-EOP transition skew and EOP width

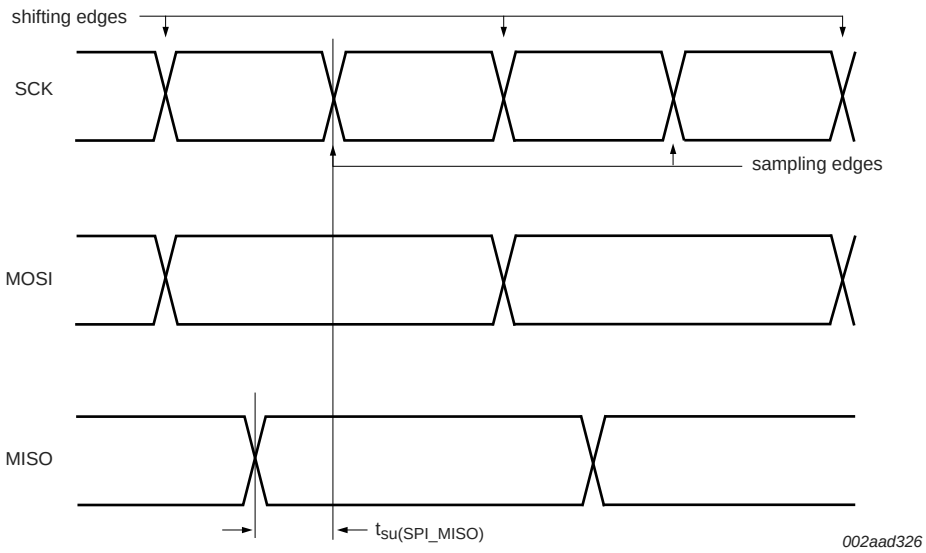


Fig 17. MISO line set-up time in SSP Master mode

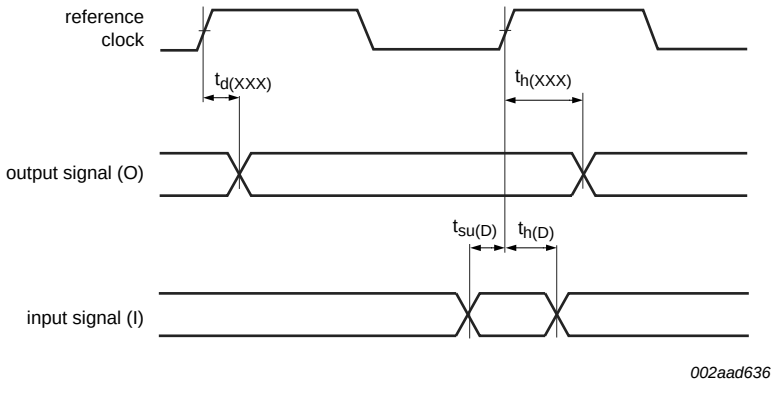


Fig 18. Signal timing

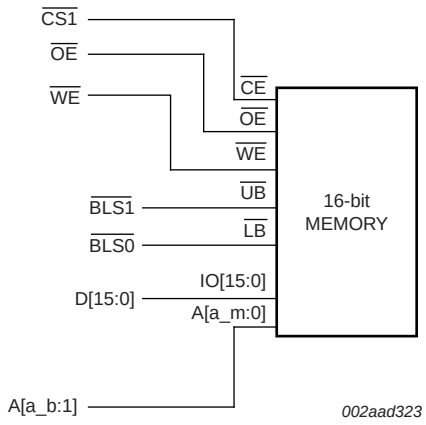


Fig 22. Booting from a single 16-bit memory chip

14.3 Suggested USB interface solutions

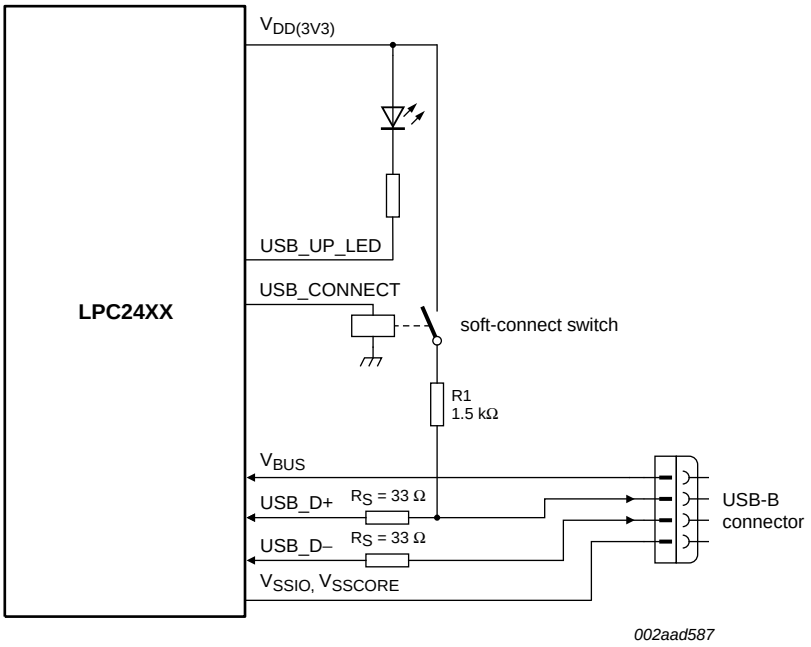


Fig 23. LPC2470 USB interface on a self-powered device

14.6 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1}, C_{X2}, and C_{X3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{X1} and C_{X2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

14.7 Standard I/O pin configuration

Figure 32 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Analog input (for ADC input channels)

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

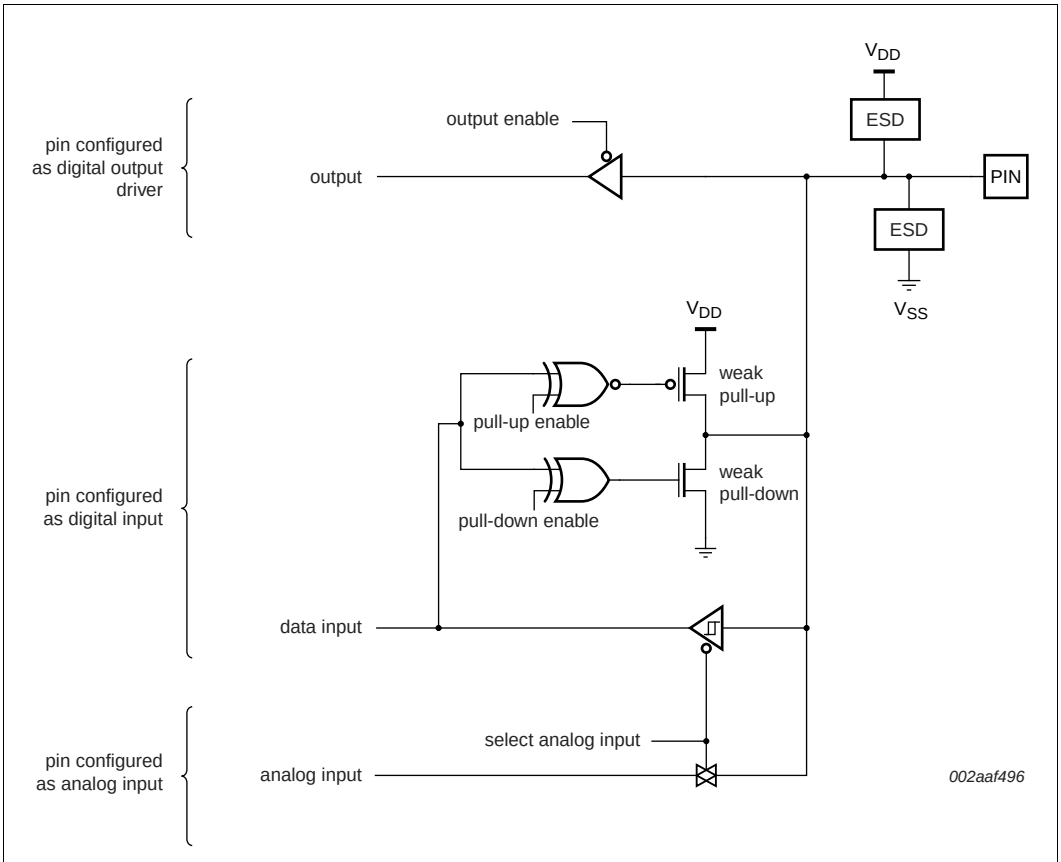
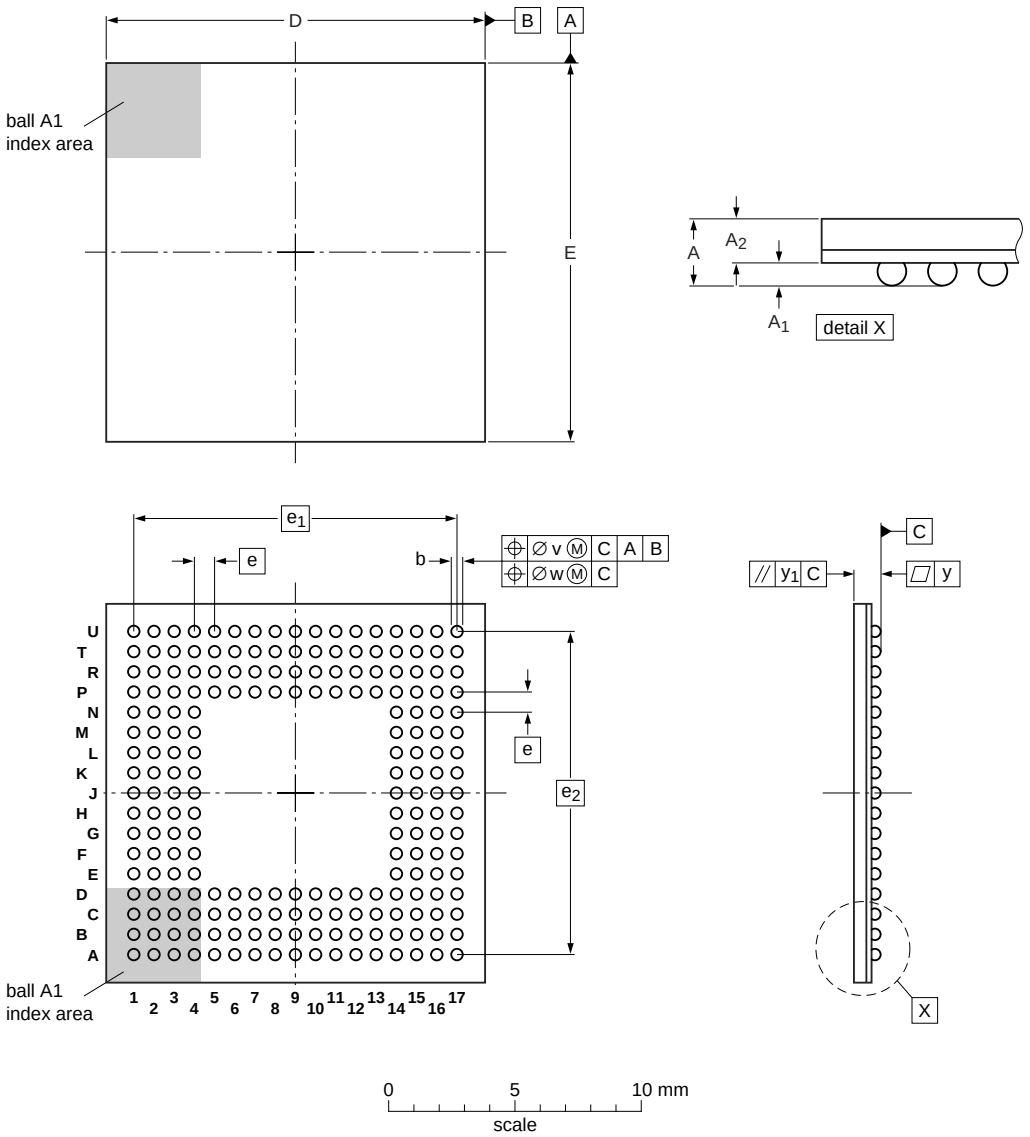


Fig 32. Standard I/O pin configuration with analog input

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 15 x 15 x 0.7 mm **SOT950-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.6	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT950-1		- - -				~~06-06-01~~ 06-06-14

Fig 35. Package outline SOT950-1 (TFBGA208)

20. Contents

continued >>