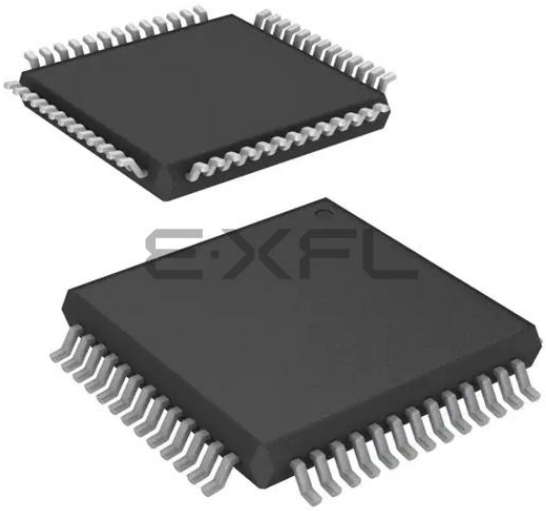
Renesas Electronics America Inc - R5F523T3ADFD#30 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f523t3adfd-30

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.
Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/3)

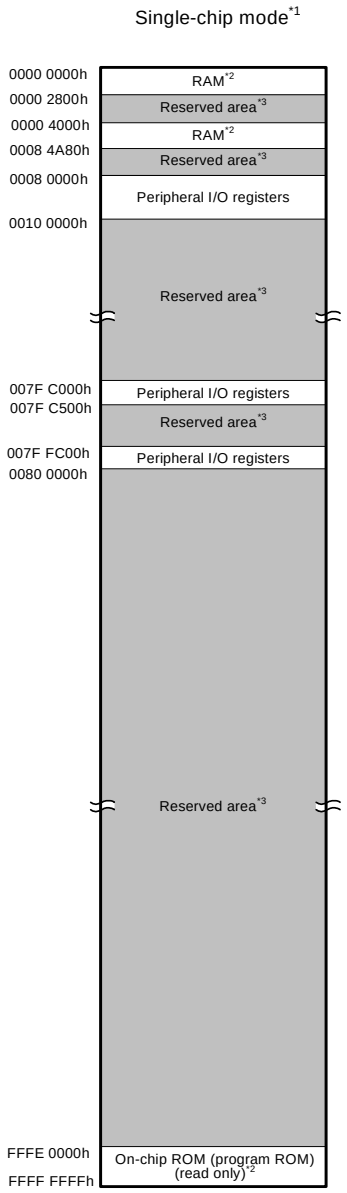
Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 40 MHz • 32-bit RX CPU (RX v2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 Variable-length instruction format • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 64 K/128 Kbytes • 32 MHz, no-wait memory access 32 to 40 MHz: wait states • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 12 Kbytes • 40 MHz, no-wait memory access
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, low-speed and high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC): Available • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 40 MHz (at max.) MTU3c runs in synchronization with the PCLKA: 40 MHz (at max.) Peripheral modules other than MTU3c run in synchronization with the PCLKB: 40 MHz (at max.) ADCLK operated in S12ADE runs in synchronization with the PCLKD: 40 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 2 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 9 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode and middle-speed operating mode

Table 1.6 List of Pins and Pin Functions (64-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCIg, RSPI, RIIC)	Others
1		P02		CTS1#/RTS1#/SS1#	ADST0/IRQ5
2		P00			IRQ2
3	VCL				
4		P01	CACREF		IRQ4
5	MD				FINED
6	RES#				
7	XTAL	P37			
8	VSS				
9	EXTAL	P36			
10	VCC				
11		PE2	POE10#		NMI
12		PD7	TMRI1	SSLA1	
13		PD6	TMO1	SSLA0/CTS1#/RTS1#/SS1#	ADST0/IRQ5
14		PD5	TMRI0	RXD1/SMISO1/SSCL1	IRQ3
15		PD4	TMCI0	SCK1	IRQ2
16		PD3	TMO0	TXD1/SMOSI1/SSDA1	
17		PB7		SCK5	
18		PB6		RXD5/SMISO5/SSCL5	IRQ5
19		PB5		TXD5/SMOSI5/SSDA5	
20	VCC				
21		PB4	POE8#		IRQ3
22	VSS				
23		PB3	MTIOC0A/CACREF	SCK5/RSPCKA	
24		PB2	MTIOC0B/ADSM0	TXD5/SMOSI5/SSDA5/SDA0	
25		PB1	MTIOC0C	RXD5/SMISO5/SSCL5/SCL0	IRQ2
26		PB0	MTIOC0D	MOSIA	
27		PA3	MTIOC2A	SSLA0	
28		PA2	MTIOC2B	CTS5#/RTS5#/SS5#/SSLA1	IRQ4
29		P94	MTIOC0C/TMO1	MISOA	IRQ1
30		P93	MTIOC0B/TMRI1	SCK5/RSPCKA	IRQ0
31		P92	TMCI1	SSLA2	
32		P91		SSLA3	
33		P76	MTIOC4D		
34		P75	MTIOC4C		
35		P74	MTIOC3D		
36		P73	MTIOC4B		
37		P72	MTIOC4A		
38		P71	MTIOC3B		
39		P70	POE0#		IRQ5
40		P33	MTIOC3A/MTCLKA	SSLA3	
41		P32	MTIOC3C/MTCLKB	SSLA2	
42	VCC				
43		P31	MTIOC0A/MTCLKC	SSLA1	
44	VSS				
45		P30	MTIOC0B/MTCLKD	SSLA0	
46		P24	MTIC5U/TMCI2	RSPCKA	COMP0/IRQ3
47		P23	MTIC5V/CACREF/TMO2	MOSIA	COMP1/IRQ4
48		P22	MTIC5W/TMRI2	MISOA	COMP2/IRQ2
49		P47			AN007/CMPC12/ CMPC22
50		P46			AN006/CMPC02
51		P45			AN005/CMPC21
52		P44			AN004/CMPC11
53		P43			AN003/CMPC01

Table 1.7 List of Pins and Pin Functions (52-Pin LQFP)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCIg, RSPI, RIIC)	Others
1		P02		CTS1#/RTS1#/SS1#	ADST0/IRQ5
2	VCL				
3	MD				FINED
4	RES#				
5	XTAL	P37			
6	VSS				
7	EXTAL	P36			
8	VCC				
9		PE2	POE10#		NMI
10		PD6	TMO1	SSLA0/CTS1#/RTS1#/SS1#	ADST0/IRQ5
11		PD5	TMRI0	RXD1/SMISO1/SSCL1	IRQ3
12		PD4	TMCI0	SCK1	IRQ2
13		PD3	TMO0	TXD1/SMOSI1/SSDA1	
14		PB7		SCK5	
15		PB6		RXD5/SMISO5/SSCL5	IRQ5
16		PB5		TXD5/SMOSI5/SSDA5	
17	VCC				
18		PB4	POE8#		IRQ3
19		PB3	MTIOC0A/CACREF	SCK5/RSPCKA	
20		PB2	MTIOC0B/ADSM0	TXD5/SMOSI5/SSDA5/SDA0	
21		PB1	MTIOC0C	RXD5/SMISO5/SSCL5/SCL0	IRQ2
22		PB0	MTIOC0D	MOSIA	
23		PA3	MTIOC2A	SSLA0	
24		PA2	MTIOC2B	CTS5#/RTS5#/SS5#/SSLA1	IRQ4
25		P94	MTIOC0C/TMO1	MISOA	IRQ1
26		P93	MTIOC0B/TMRI1	SCK5/RSPCKA	IRQ0
27		P76	MTIOC4D		
28		P75	MTIOC4C		
29		P74	MTIOC3D		
30		P73	MTIOC4B		
31		P72	MTIOC4A		
32		P71	MTIOC3B		
33		P70	POE0#		IRQ5
34		P33	MTIOC3A/MTCLKA	SSLA3	
35	VCC				
36	VSS				
37		P24	MTIC5U/TMCI2	RSPCKA	COMP0/IRQ3
38		P23	MTIC5V/CACREF/TMO2	MOSIA	COMP1/IRQ4
39		P22	MTIC5W/TMRI2	MISOA	COMP2/IRQ2
40		P47			AN007/CMPC12/ CMPC22
41		P46			AN006/CMPC02
42		P45			AN005/CMPC21
43		P44			AN004/CMPC11
44		P43			AN003/CMPC01
45		P42			AN002/CMPC20
46		P41			AN001/CMPC10
47		P40			AN000/CMPC00
48	AVCC0				
49	AVSS0				
50		P11	MTIOC3A/MTCLKC/TMO3		IRQ1/AN016/ CVREFC0
51		P10	MTCLKD/TMRI3		IRQ0/AN017/ CVREFC1
52		PA5	MTIOC1A/TMCI3	MISOA	



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
128 Kbytes	FFFE 0000h to FFFF FFFFh	12 Kbytes	0000 0000h to 0000 27FFh 0000 4000h to 0000 4A7Fh
64 Kbytes	FFFF 0000h to FFFF FFFFh		

Note: See Table 1.3 and Table 1.4 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(5) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

Table 4.1 List of I/O Registers (Address Order) (3 / 16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC Activation Enable Register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC Activation Enable Register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC Activation Enable Register 045	DTCER045	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8 / 16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB
0008 9066h	S12AD	A/D Sample-and-hold Circuit Control Register	ADSHCR	16	16	2 or 3 PCLKB
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9084h	S12AD	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9086h	S12AD	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 908Ah	S12AD	A/D High-Side/Low-Side Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 90DFh	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 90E4h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB
0008 90E5h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB
0008 90E6h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB

Table 5.5 DC Characteristics (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 40 MHz	I_{CC}	4.6	—	mA	
				ICLK = 32 MHz		3.9	—		
				ICLK = 16 MHz		2.8	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 40 MHz*3		15.0	—		
				ICLK = 32 MHz*4		12.4	—		
				ICLK = 16 MHz*4		7.2	—		
				ICLK = 8 MHz*4		4.6	—		
			All peripheral operation: Max.	ICLK = 40 MHz*3		—	33.0		
				ICLK = 32 MHz*4		—	24.5		
		Sleep mode	No peripheral operation*2	ICLK = 40 MHz		2.7	—		
				ICLK = 32 MHz		2.3	—		
				ICLK = 16 MHz		1.9	—		
				ICLK = 8 MHz		1.6	—		
			All peripheral operation: Normal	ICLK = 40 MHz*3		6.8	—		
				ICLK = 32 MHz*4		5.7	—		
				ICLK = 16 MHz*4		3.6	—		
				ICLK = 8 MHz*4		2.5	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 40 MHz		1.7	—		
				ICLK = 32 MHz		1.5	—		
				ICLK = 16 MHz		1.3	—		
				ICLK = 8 MHz		1.3	—		
			All peripheral operation: Normal	ICLK = 40 MHz*3		5.3	—		
				ICLK = 32 MHz*4		4.4	—		
				ICLK = 16 MHz*4		2.8	—		
				ICLK = 8 MHz*4		2.0	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	2.6	—	mA	
				ICLK = 8 MHz		1.9	—		
				ICLK = 1 MHz		1.3	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		5.5	—		
				ICLK = 8 MHz		4.2	—		
				ICLK = 1 MHz		1.6	—		
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	11.0		

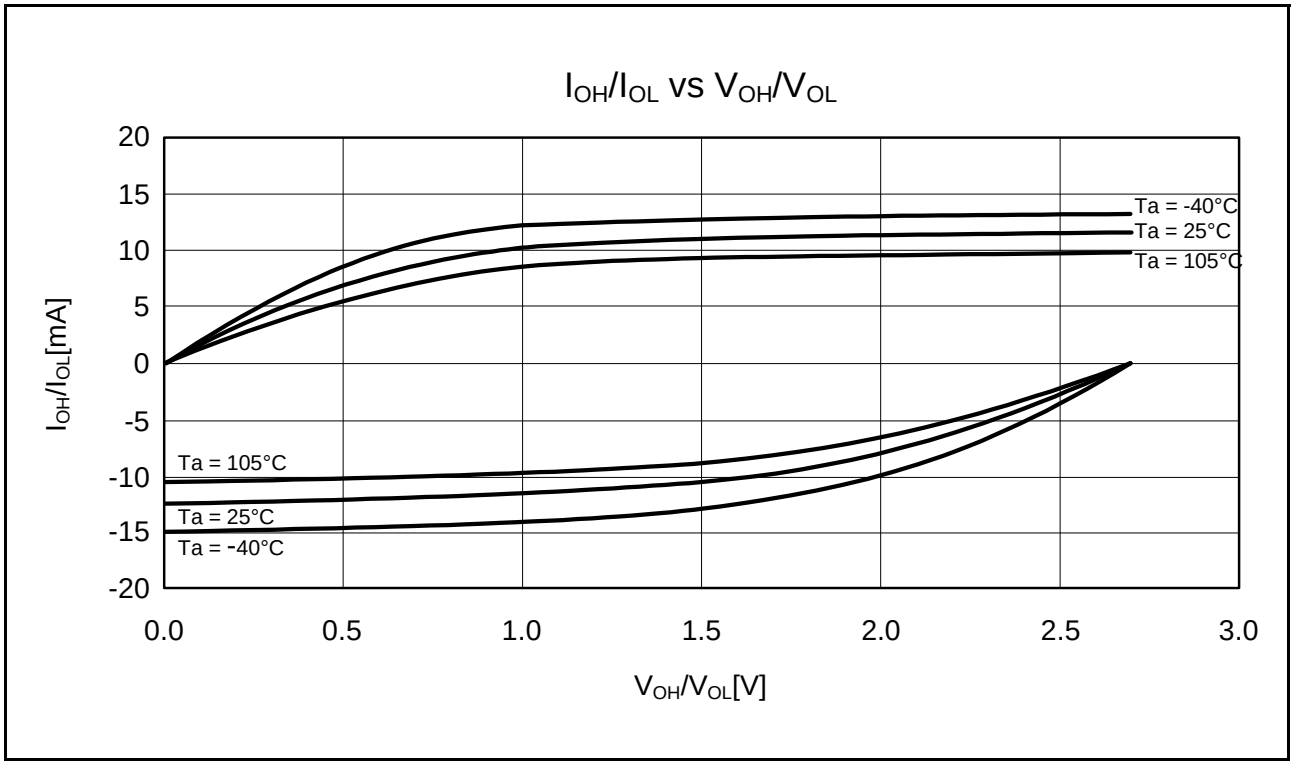


Figure 5.5 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)**

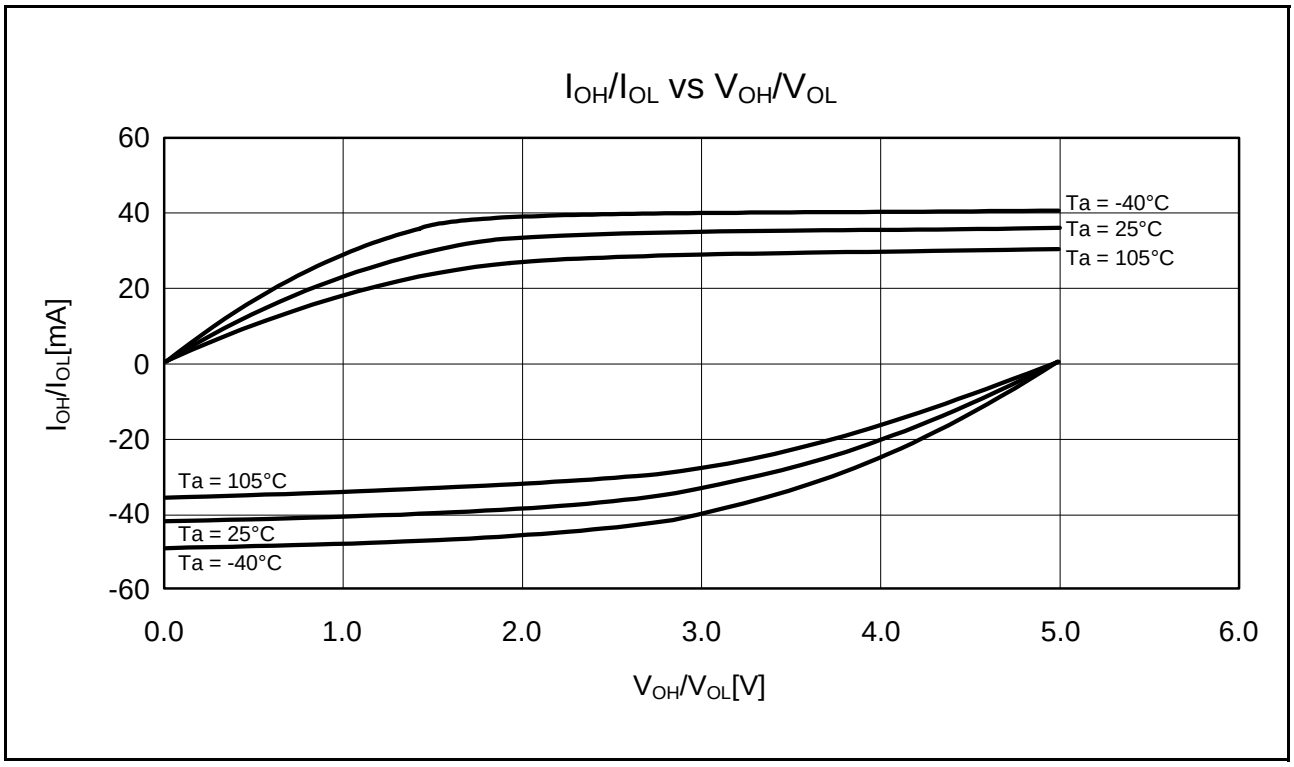


Figure 5.6 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.0 V when Normal Output is Selected (Reference Data)**

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.8 to Figure 5.11 show the characteristics when high-drive output is selected by the drive capacity control register.

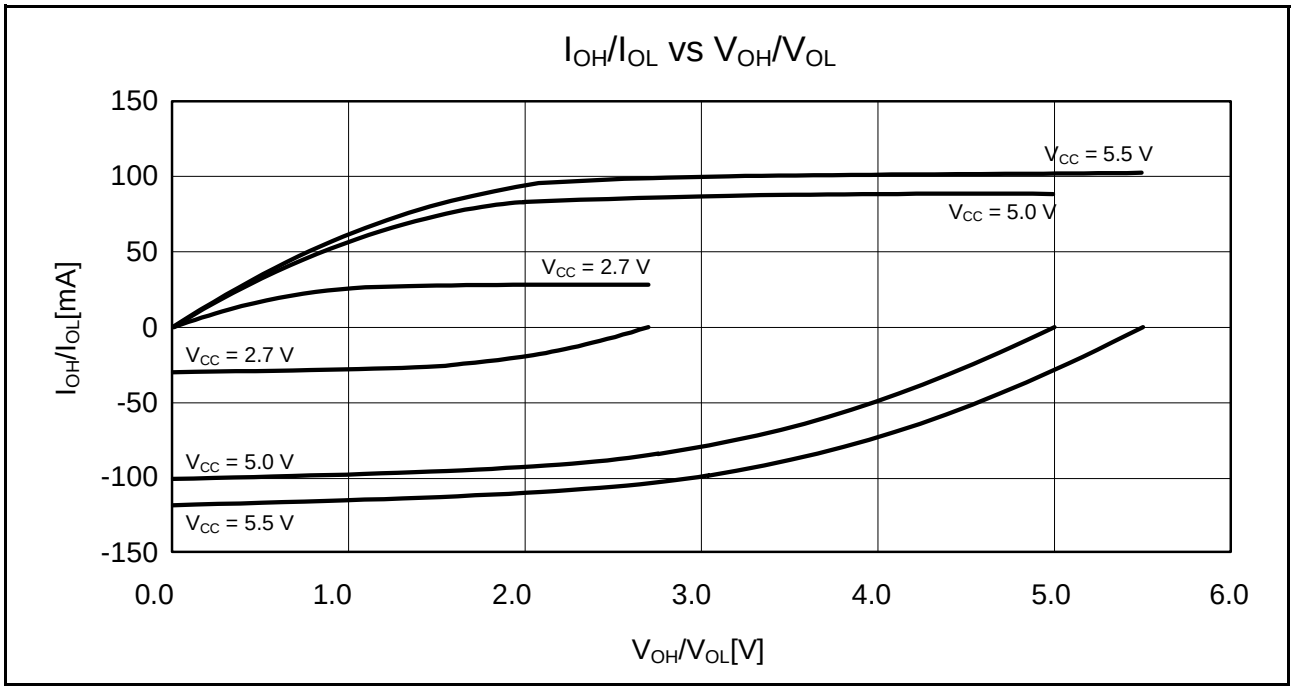


Figure 5.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

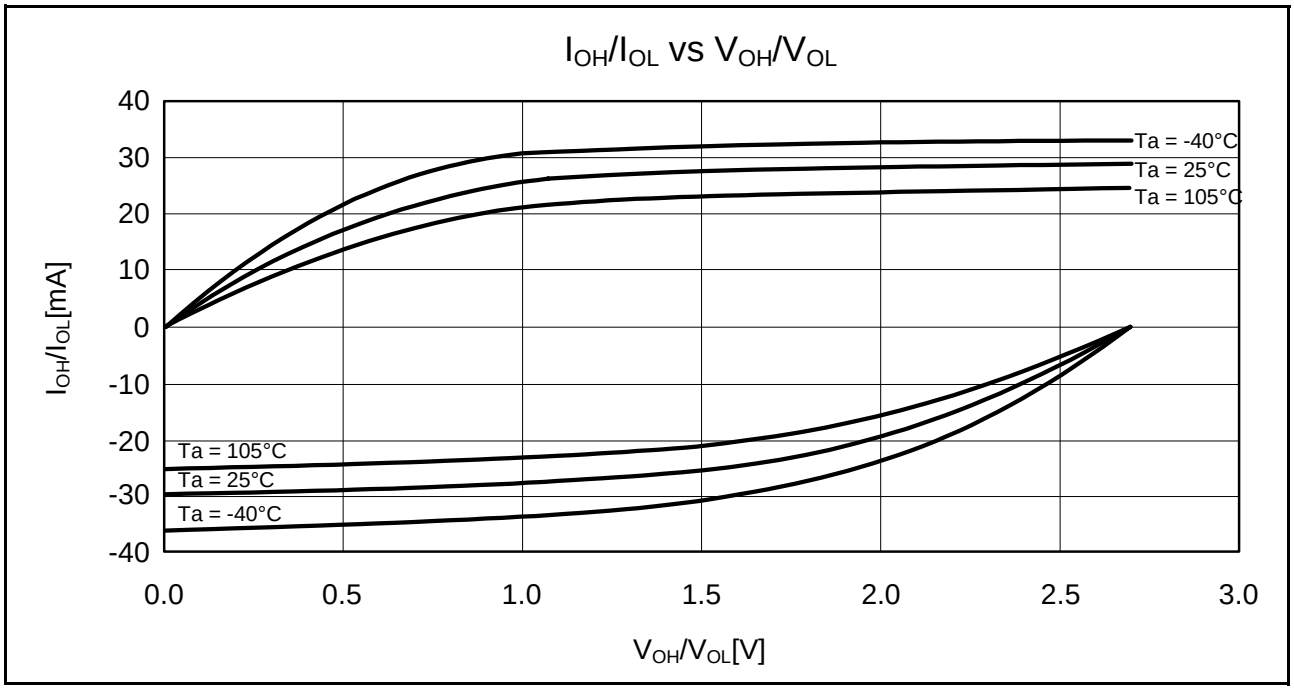


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

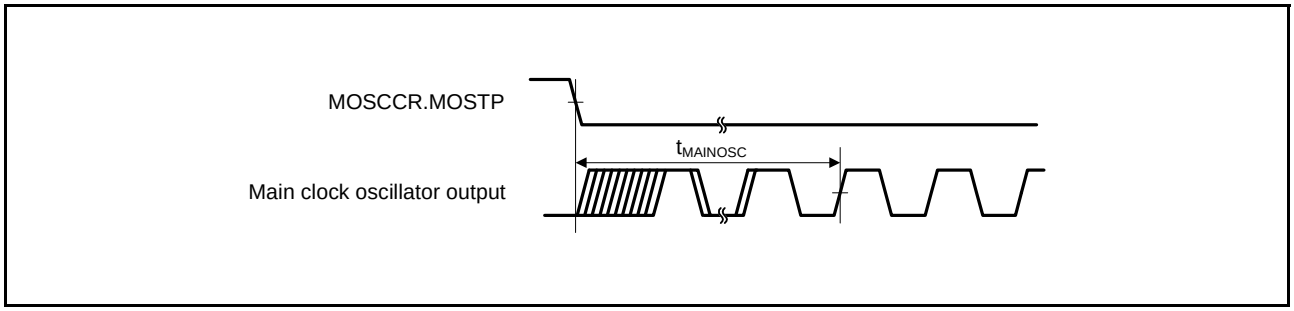


Figure 5.21 Main Clock Oscillation Start Timing

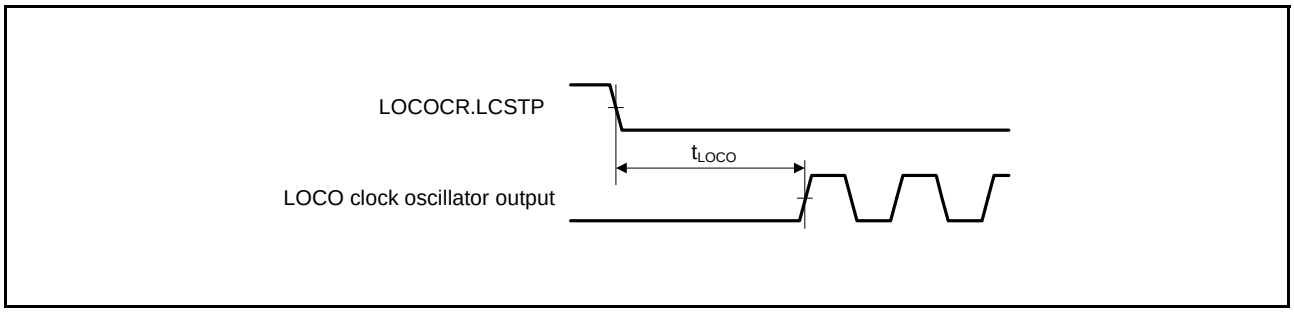


Figure 5.22 LOCO Clock Oscillation Start Timing

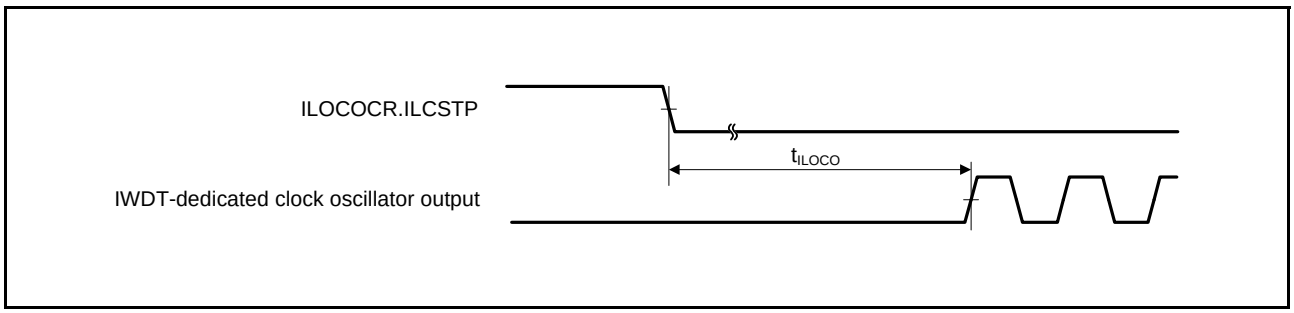


Figure 5.23 IWDT-Dedicated Clock Oscillation Start Timing

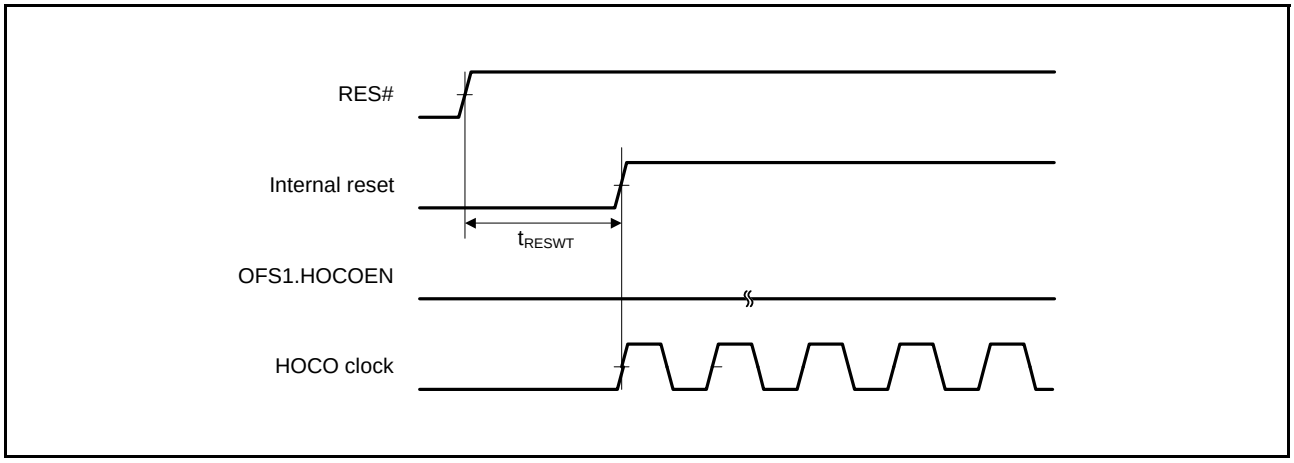


Figure 5.24 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

Table 5.25 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, C = 30pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.42
	SCK clock cycle input (slave)			6	65536	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC = 4.0 V or above	t_{SU}	40	—	ns	Figure 5.43, Figure 5.44
		VCC = 2.7 V or above		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC = 4.0 V or above		—	40		
		VCC = 2.7 V or above		—	65		
	Data output hold time (master)	Master	t_{OH}	–10	—	ns	
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.45, Figure 5.46
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 5.27 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.*2	Max.	Unit	Test Conditions
Simple I²C (Standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 5.47
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{pcyc}*1	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple I²C (Fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 5.47
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{pcyc}*1	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. C_b is the total capacitance of the bus lines.

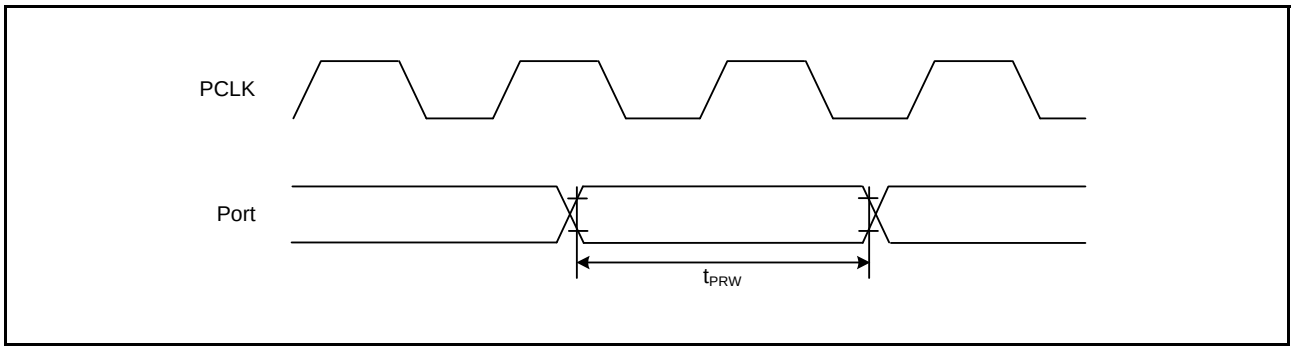


Figure 5.34 I/O Port Input Timing

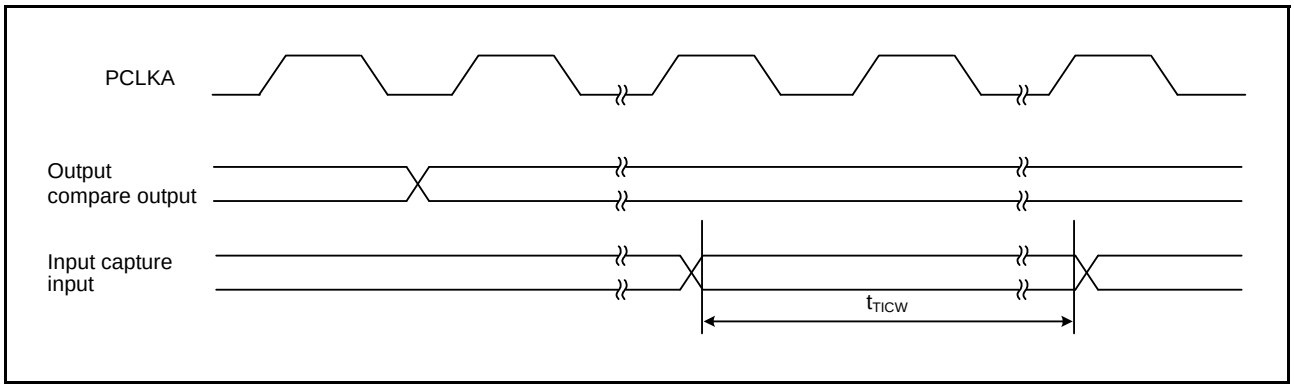


Figure 5.35 MTU3 Input/Output Timing

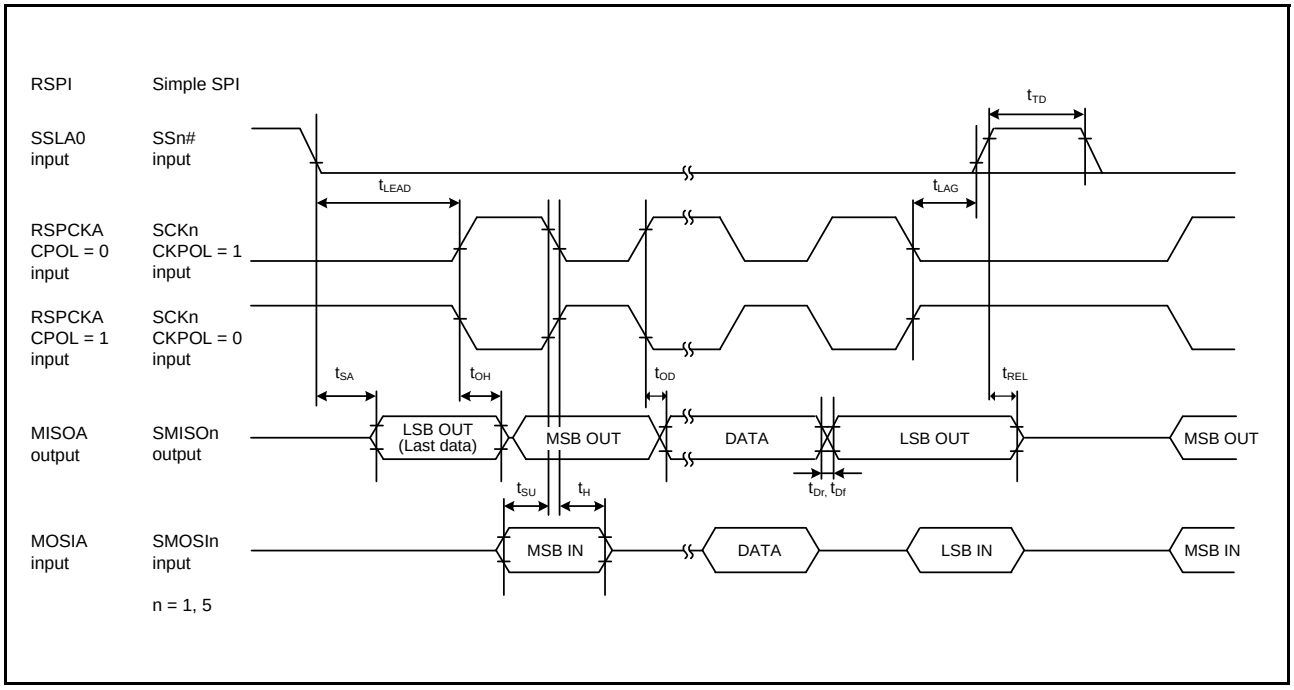


Figure 5.46 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

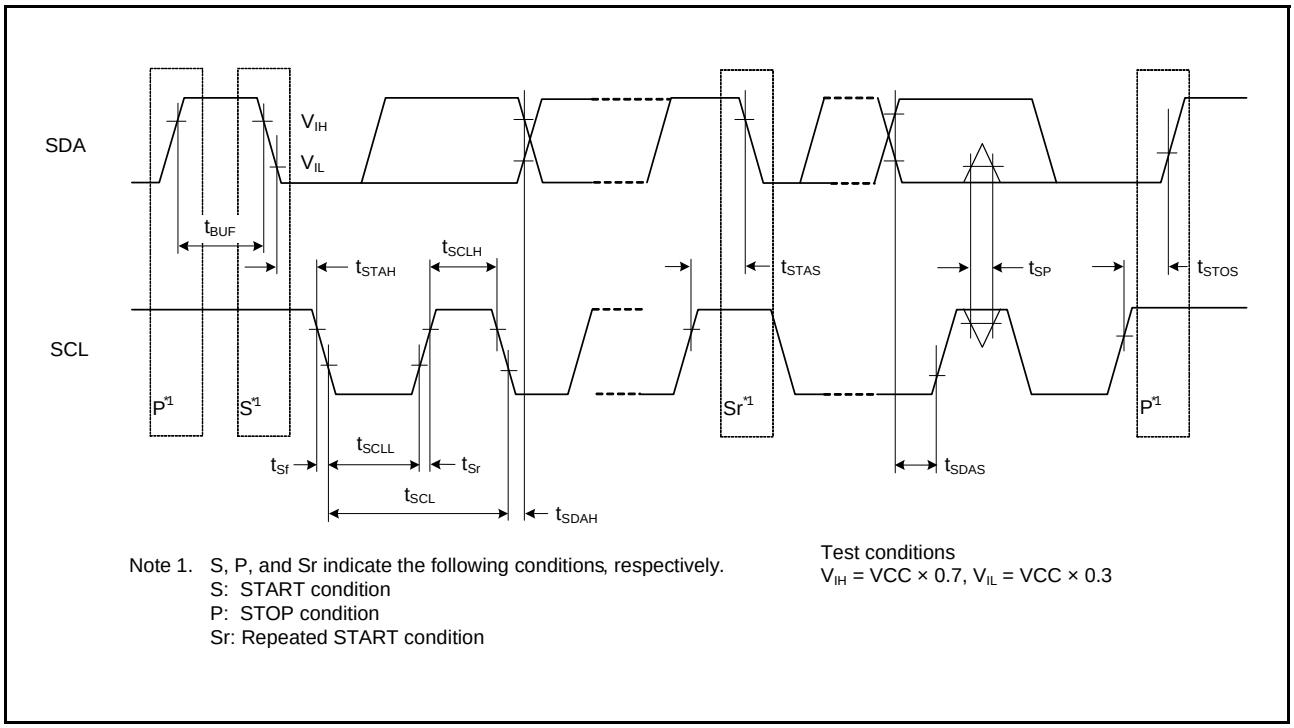


Figure 5.47 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

5.4 A/D Conversion Characteristics

Table 5.28 A/D Conversion Characteristics (1)

Conditions: VCC = 4.5 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	40	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 40 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit not in use	1.00	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 08h
		1.25	—	—	µs	Normal-precision channel ADSSTRn.SST[7:0] bits = 12h
	Permissible signal source impedance (Max.) = 1.0 kΩ / Sample-and-hold circuit in use	1.65	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 08h ADSHCR.SSTSH[7:0] bits = 0Dh AN000 to AN002 = 0.25 V to VREFH0 – 0.25 V
Analog input capacitance		—	—	12	pF	
Offset error		—	—	±6.5	LSB	
Full-scale error		—	—	±6.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	—	±8.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.5	LSB	
INL integral nonlinearity error		—	±2.0	±4.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.5 Comparator Characteristics

Table 5.32 Comparator Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Offset voltage	V_{cioff}	—	—	40	mV	
Reference input voltage range	V_{cref}	0	—	AVCC0	V	
Response time	t_{cr}	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	t_{cf}	—	—	200	ns	
Stabilization wait time for input selection	t_{cwait}	300	—	—	ns	
Operation stabilization wait time	t_{cmp}		—	1	µs	

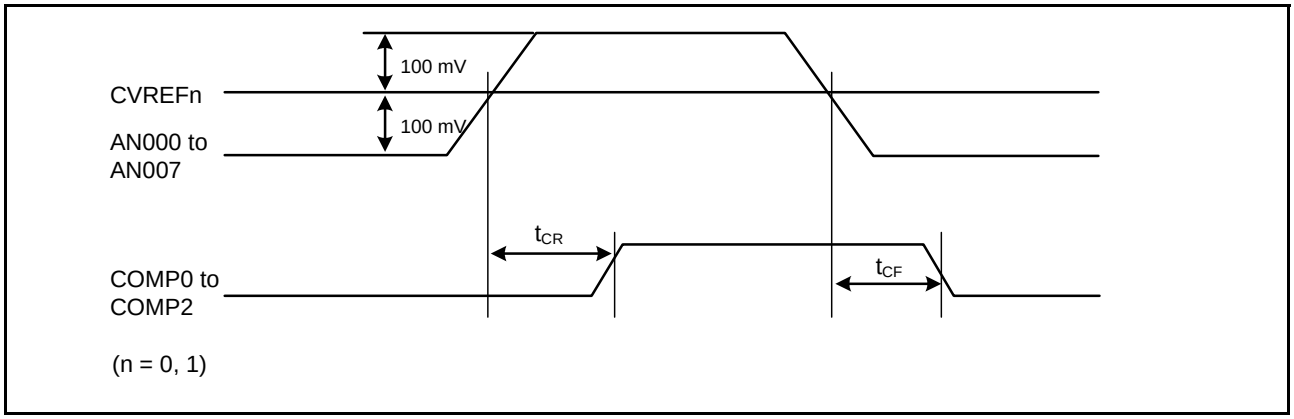
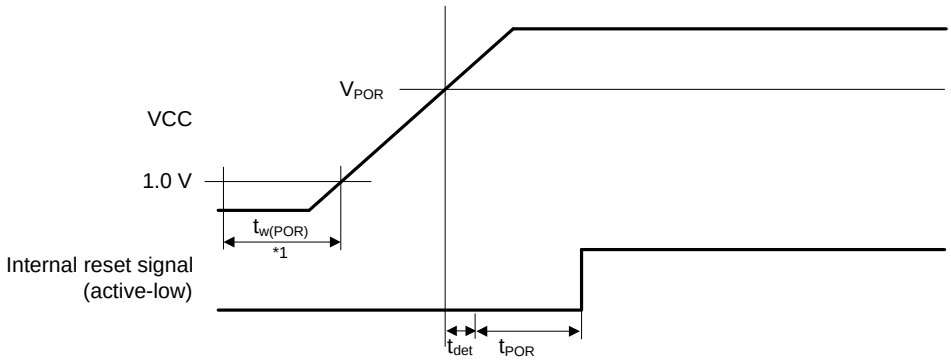


Figure 5.49 Comparator Response Time



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 5.51 Power-On Reset Timing

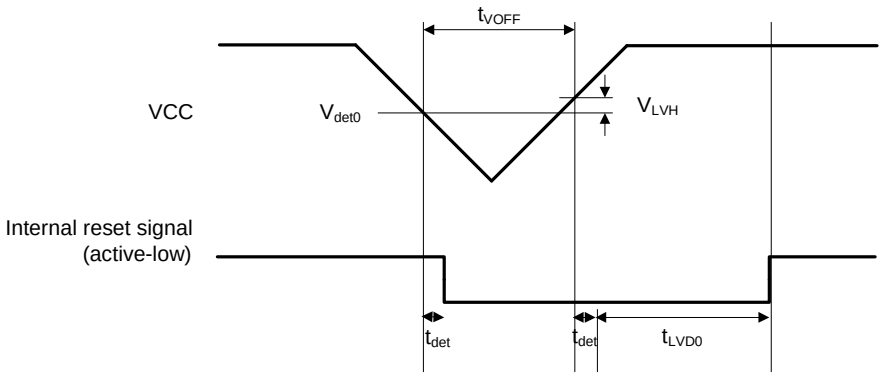
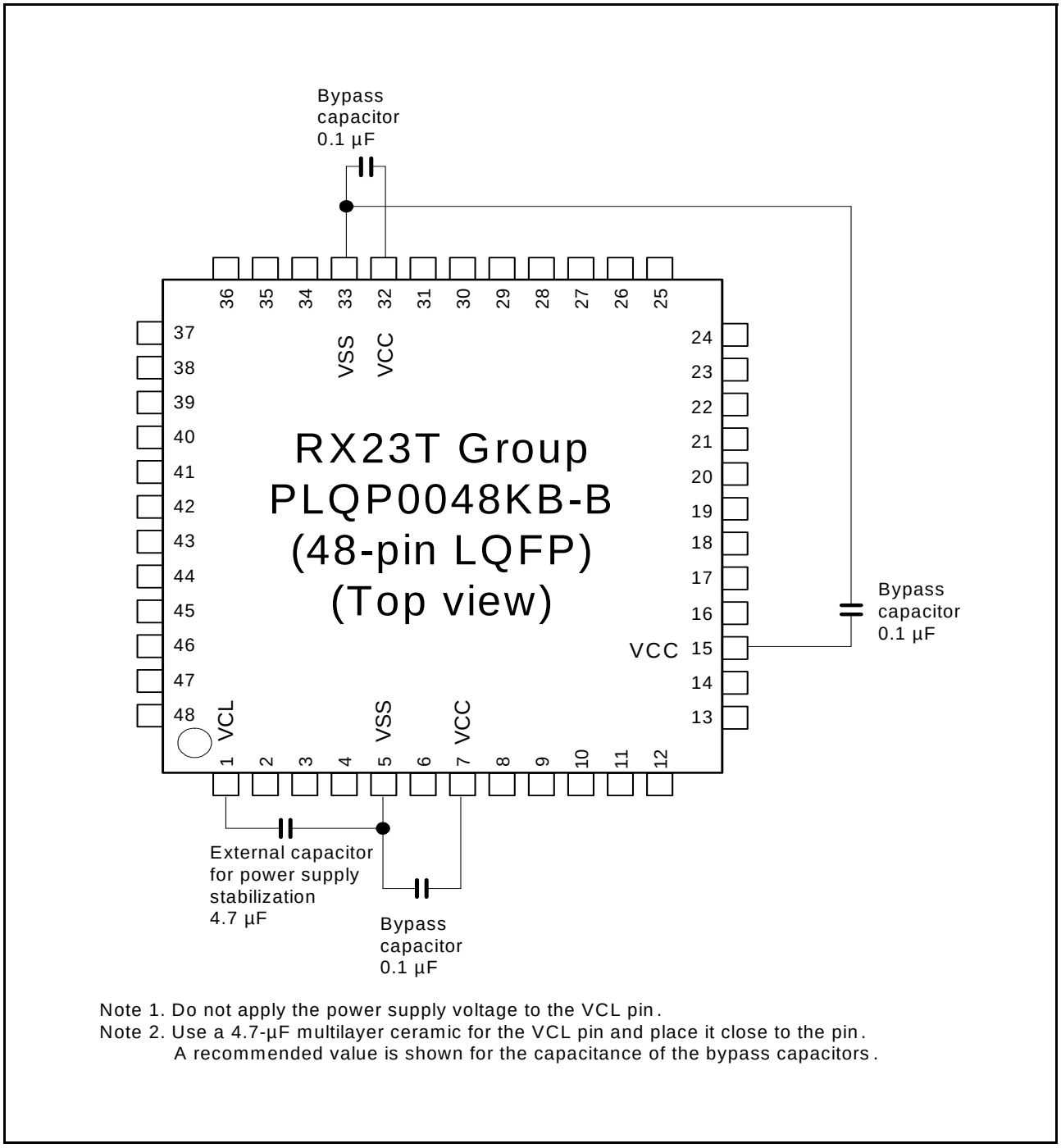


Figure 5.52 Voltage Detection Circuit Timing (Vdet0)



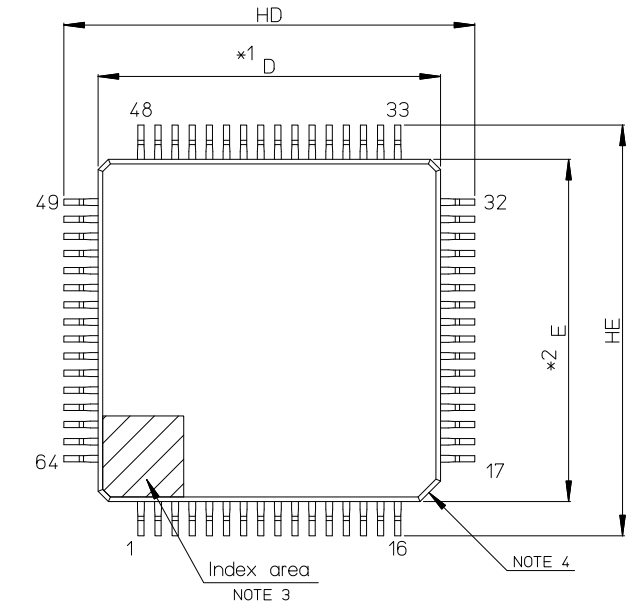
Note 1. Do not apply the power supply voltage to the VCL pin.
Note 2. Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

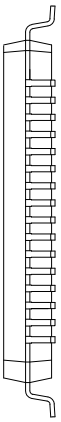
Figure 5.58 Connecting Capacitors (48 Pins)

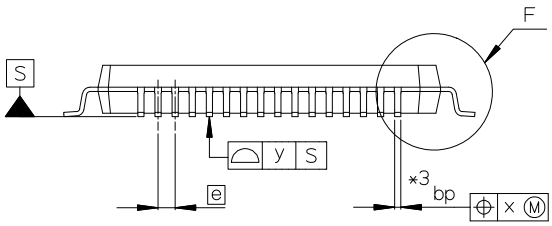
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

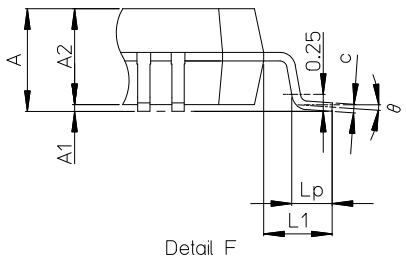
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure A 64-Pin LFQFP (PLQP0064KB-C)

REVISION HISTORY	RX23T Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Mar 31, 2015	—	First edition, issued	
1.10	Oct 30, 2015	Features		
		1	Features changed	
		1. Overview		
		2, 3	Table 1.1 Outline of Specifications (1/3) (2/3) changed	
		6	Table 1.3 List of Products: D Version (Ta = –40 to +85°C) changed	
		6	Table 1.4 List of Products: G Version (Ta = –40 to +105°C) changed	
		7	Figure 1.1 How to Read the Product Part Number changed	
		10	Table 1.5 Pin Functions (2/2) changed	
		11	Figure 1.3 Pin Assignments of the 64-Pin LFQFP changed	
		12	Figure 1.4 Pin Assignments of the 52-Pin LQFP changed	
		13	Figure 1.5 Pin Assignments of the 48-Pin LFQFP changed	
		14	Table 1.6 List of Pins and Pin Functions (64-Pin LFQFP) (1/2) changed	
		16	Table 1.7 List of Pins and Pin Functions (52-Pin LQFP) changed	
		17	Table 1.8 List of Pins and Pin Functions (48-Pin LFQFP) changed	
		3. Address Space		
		22	Figure 3.1 Memory Map in Each Operating Mode changed	
		4. I/O Registers		
		25	Table 4.1 List of I/O Registers (Address Order) (1 / 16) Address: 0008 0036h High-Speed On-Chip Oscillator Control Register (HOCOCR), Address: 0008 00A5h High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR) added	
		34	Table 4.1 List of I/O Registers (Address Order) (10 / 16) Address: 0008 C087h Open Drain Control Register 1 (ODR1) added	
		5. Electrical Characteristics		
		42	Table 5.3 DC Characteristics (1) changed	
		57	Table 5.14 Operating Frequency Value (High-Speed Operating Mode), Table 5.15 Operating Frequency Value (Middle-Speed Operating Mode) changed	
		58	Table 5.16 Clock Timing, Figure 5.20 EXTAL External Clock Input Timing changed	
		59, 60	Figure 5.24 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0), Figure 5.25 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit) added	
		79	Table 5.32 Comparator Characteristics changed	
		80	Table 5.33 D/A Conversion Characteristics symbol added	
		82	Table 5.35 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2) changed	
		83	Figure 5.52 Voltage Detection Circuit Timing (Vdet0) changed	
		89	Figure 5.56 Connecting Capacitors (64 Pins) changed	
		90	Figure 5.57 Connecting Capacitors (52 Pins) changed	
		91	Figure 5.58 Connecting Capacitors (48 Pins) changed	
		Appendix 1. Package Dimensions		
		92	Figure A 64-Pin LFQFP (PLQP0064KB-C) changed	
		93	Figure B 52-Pin LQFP (PLQP0052JA-B) changed	
		94	Figure C 48 -Pin LFQFP (PLQP0048KB-B) changed	