Renesas Electronics America Inc - R5F523T3ADFM#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f523t3adfm-30

1.3 Block Diagram

Figure 1.2 shows a block diagram.

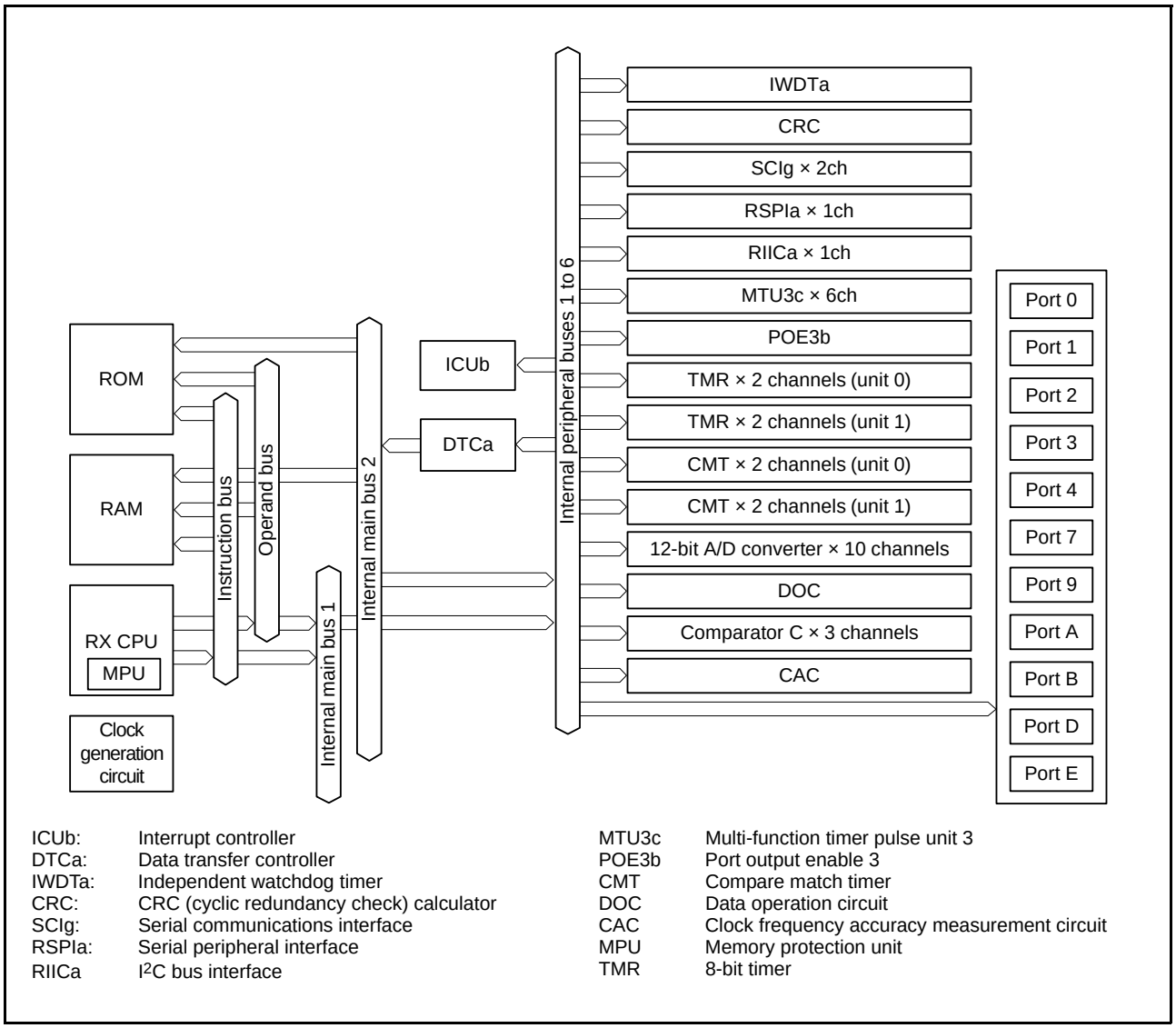


Figure 1.2 Block Diagram

Table 1.7 List of Pins and Pin Functions (52-Pin LQFP)

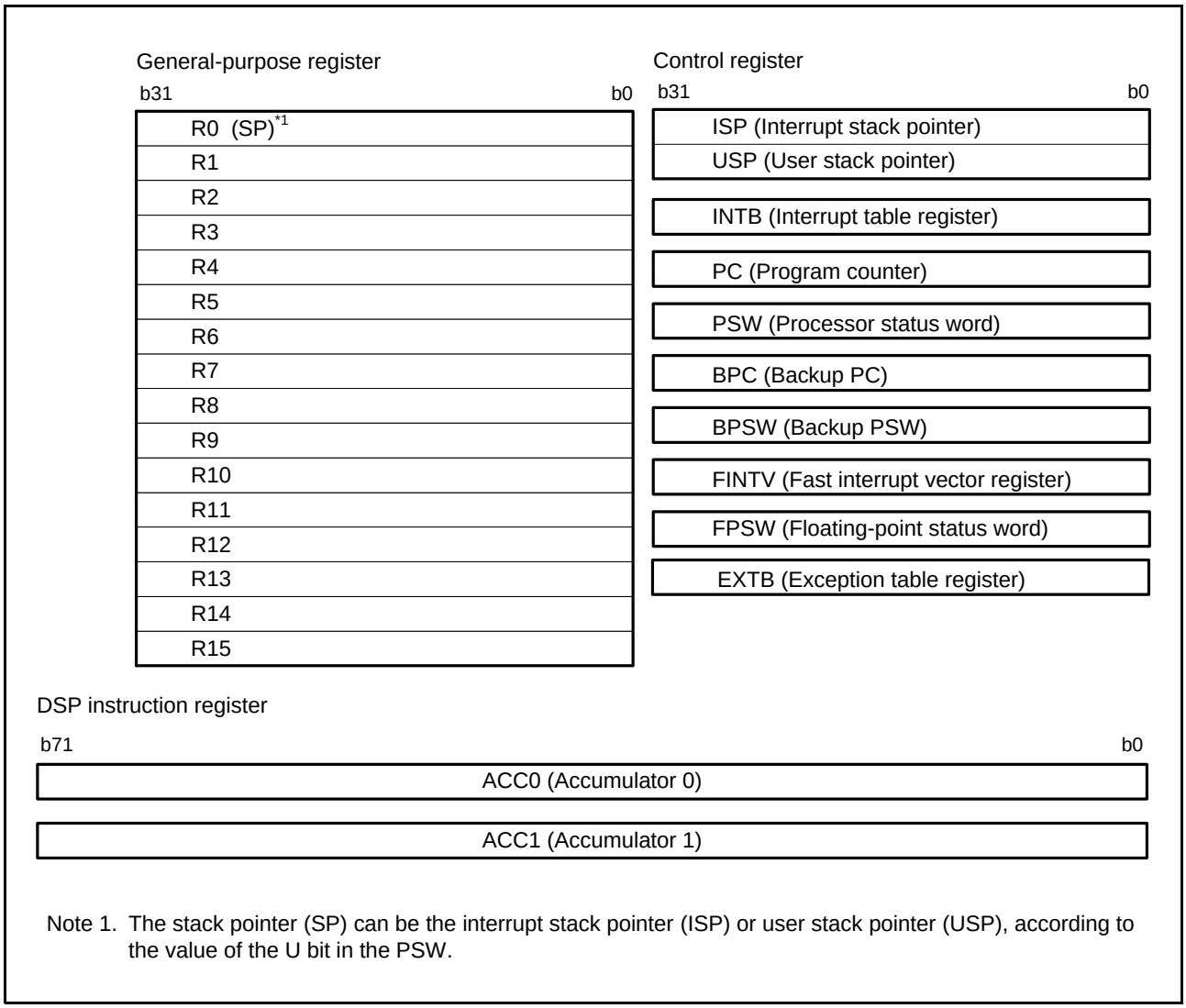
Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCIg, RSPI, RIIC)	Others
1		P02		CTS1#/RTS1#/SS1#	ADST0/IRQ5
2	VCL				
3	MD				FINED
4	RES#				
5	XTAL	P37			
6	VSS				
7	EXTAL	P36			
8	VCC				
9		PE2	POE10#		NMI
10		PD6	TMO1	SSLA0/CTS1#/RTS1#/SS1#	ADST0/IRQ5
11		PD5	TMRI0	RXD1/SMISO1/SSCL1	IRQ3
12		PD4	TMCI0	SCK1	IRQ2
13		PD3	TMO0	TXD1/SMOSI1/SSDA1	
14		PB7		SCK5	
15		PB6		RXD5/SMISO5/SSCL5	IRQ5
16		PB5		TXD5/SMOSI5/SSDA5	
17	VCC				
18		PB4	POE8#		IRQ3
19		PB3	MTIOC0A/CACREF	SCK5/RSPCKA	
20		PB2	MTIOC0B/ADSM0	TXD5/SMOSI5/SSDA5/SDA0	
21		PB1	MTIOC0C	RXD5/SMISO5/SSCL5/SCL0	IRQ2
22		PB0	MTIOC0D	MOSIA	
23		PA3	MTIOC2A	SSLA0	
24		PA2	MTIOC2B	CTS5#/RTS5#/SS5#/SSLA1	IRQ4
25		P94	MTIOC0C/TMO1	MISOA	IRQ1
26		P93	MTIOC0B/TMRI1	SCK5/RSPCKA	IRQ0
27		P76	MTIOC4D		
28		P75	MTIOC4C		
29		P74	MTIOC3D		
30		P73	MTIOC4B		
31		P72	MTIOC4A		
32		P71	MTIOC3B		
33		P70	POE0#		IRQ5
34		P33	MTIOC3A/MTCLKA	SSLA3	
35	VCC				
36	VSS				
37		P24	MTIC5U/TMCI2	RSPCKA	COMP0/IRQ3
38		P23	MTIC5V/CACREF/TMO2	MOSIA	COMP1/IRQ4
39		P22	MTIC5W/TMRI2	MISOA	COMP2/IRQ2
40		P47			AN007/CMPC12/ CMPC22
41		P46			AN006/CMPC02
42		P45			AN005/CMPC21
43		P44			AN004/CMPC11
44		P43			AN003/CMPC01
45		P42			AN002/CMPC20
46		P41			AN001/CMPC10
47		P40			AN000/CMPC00
48	AVCC0				
49	AVSS0				
50		P11	MTIOC3A/MTCLKC/TMO3		IRQ1/AN016/ CVREFC0
51		P10	MTCLKD/TMRI3		IRQ0/AN017/ CVREFC1
52		PA5	MTIOC1A/TMCI3	MISOA	

Table 1.8 List of Pins and Pin Functions (48-Pin LFQFP)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCIg, RSPI, RIIC)	Others
1	VCL				
2	MD				FINED
3	RES#				
4	XTAL	P37			
5	VSS				
6	EXTAL	P36			
7	VCC				
8		PE2	POE10#		NMI
9		PD6	TMO1	SSLA0/CTS1#/RTS1#/SS1#	ADST0/IRQ5
10		PD5	TMRI0	RXD1/SMISO1/SSCL1	IRQ3
11		PD4	TMCI0	SCK1	IRQ2
12		PD3	TMO0	TXD1/SMOSI1/SSDA1	
13		PB6		RXD5/SMISO5/SSCL5	IRQ5
14		PB5		TXD5/SMOSI5/SSDA5	
15	VCC				
16		PB4	POE8#		IRQ3
17		PB3	MTIOC0A/CACREF	SCK5/RSPCKA	
18		PB2	MTIOC0B/ADSM0	TXD5/SMOSI5/SSDA5/SDA0	
19		PB1	MTIOC0C	RXD5/SMISO5/SSCL5/SCL0	IRQ2
20		PB0	MTIOC0D	MOSIA	
21		PA3	MTIOC2A	SSLA0	
22		PA2	MTIOC2B	CTS5#/RTS5#/SS5#/SSLA1	IRQ4
23		P94	MTIOC0C/TMO1	MISOA	IRQ1
24		P93	MTIOC0B/TMRI1	SCK5/RSPCKA	IRQ0
25		P76	MTIOC4D		
26		P75	MTIOC4C		
27		P74	MTIOC3D		
28		P73	MTIOC4B		
29		P72	MTIOC4A		
30		P71	MTIOC3B		
31		P70	POE0#		IRQ5
32	VCC				
33	VSS				
34		P24	MTIC5U/TMCI2	RSPCKA	COMP0/IRQ3
35		P23	MTIC5V/CACREF/TMO2	MOSIA	COMP1/IRQ4
36		P22	MTIC5W/TMRI2	MISOA	COMP2/IRQ2
37		P47			AN007/CMPC12/ CMPC22
38		P46			AN006/CMPC02
39		P45			AN005/CMPC21
40		P44			AN004/CMPC11
41		P43			AN003/CMPC01
42		P42			AN002/CMPC20
43		P41			AN001/CMPC10
44		P40			AN000/CMPC00
45	AVCC0				
46	AVSS0				
47		P11	MTIOC3A/MTCLKC/TMO3		IRQ1/AN016/ CVREFC0
48		P10	MTCLKD/TMRI3		IRQ0/AN017/ CVREFC1

2. CPU

Figure 2.1 shows register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (7 / 16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB
0008 8300h	RIIC0	I^2C Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB
0008 8301h	RIIC0	I^2C Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB
0008 8302h	RIIC0	I^2C Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB
0008 8303h	RIIC0	I^2C Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB
0008 8304h	RIIC0	I^2C Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB
0008 8305h	RIIC0	I^2C Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB
0008 8306h	RIIC0	I^2C Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB
0008 8307h	RIIC0	I^2C Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB
0008 8308h	RIIC0	I^2C Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB
0008 8309h	RIIC0	I^2C Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB
0008 8310h	RIIC0	I^2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB
0008 8311h	RIIC0	I^2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB
0008 8312h	RIIC0	I^2C Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB
0008 8313h	RIIC0	I^2C Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (9 / 16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 90E7h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0A9h	SCI5	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0AAh	SCI5	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0ABh	SCI5	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0ACh	SCI5	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (15 / 16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000C 1405h	MTU2	Timer Status Register	TSR	8	8	4 or 5 PCLKA
000C 1406h	MTU2	Timer Counter	TCNT	16	16	4 or 5 PCLKA
000C 1408h	MTU2	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 140Ch	MTU2	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1480h	MTU5	Timer Counter U	TCNTU	16	16, 32	4 or 5 PCLKA
000C 1482h	MTU5	Timer General Register U	TGRU	16	16	4 or 5 PCLKA
000C 1484h	MTU5	Timer Control Register U	TCRU	8	8	4 or 5 PCLKA
000C 1485h	MTU5	Timer Control Register 2U	TCR2U	8	8	4 or 5 PCLKA
000C 1486h	MTU5	Timer I/O Control Register U	TIORU	8	8	4 or 5 PCLKA
000C 1490h	MTU5	Timer Counter V	TCNTV	16	16, 32	4 or 5 PCLKA
000C 1492h	MTU5	Timer General Register V	TGRV	16	16	4 or 5 PCLKA
000C 1494h	MTU5	Timer Control Register V	TCRV	8	8	4 or 5 PCLKA
000C 1495h	MTU5	Timer Control Register 2V	TCR2V	8	8	4 or 5 PCLKA
000C 1496h	MTU5	Timer I/O Control Register V	TIORV	8	8	4 or 5 PCLKA
000C 14A0h	MTU5	Timer Counter W	TCNTW	16	16, 32	4 or 5 PCLKA
000C 14A2h	MTU5	Timer General Register W	TGRW	16	16	4 or 5 PCLKA
000C 14A4h	MTU5	Timer Control Register W	TCRW	8	8	4 or 5 PCLKA
000C 14A5h	MTU5	Timer Control Register 2W	TCR2W	8	8	4 or 5 PCLKA
000C 14A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	4 or 5 PCLKA
000C 14B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA
000C 14B4h	MTU5	Timer Start Register	TSTR	8	8	4 or 5 PCLKA
000C 14B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	4 or 5 PCLKA
000C 1D30h	MTU	A/D Conversion Start Request Select Register 0	TADSTRGR0	8	8	4 or 5 PCLKA
007F C100h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F C104h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F C108h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F C110h	FLASH	Flash Processing Start Address Register H	FSARH	16	16	2 or 3 FCLK
007F C114h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F C118h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F C120h	FLASH	Flash Processing End Address Register H	FEARH	16	16	2 or 3 FCLK
007F C124h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F C12Ch	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F C130h	FLASH	Flash Write Buffer Register 0	FWB0	16	16	2 or 3 FCLK
007F C138h	FLASH	Flash Write Buffer Register 1	FWB1	16	16	2 or 3 FCLK
007F C140h	FLASH	Flash Write Buffer Register 2	FWB2	16	16	2 or 3 FCLK
007F C144h	FLASH	Flash Write Buffer Register 3	FWB3	16	16	2 or 3 FCLK
007F C180h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK
007F C184h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK
007F C1C0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK
007F C1C8h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	2 or 3 FCLK
007F C1D0h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C1D8h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C1DCh	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C1E0h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C1E8h	FLASH	Flash Error Address Monitor Register H	FEAMH	16	16	2 or 3 FCLK
007F C1F0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK
007F C350h	FLASHCONST	Unique ID Register 0	UIDR0	32	32	2 or 3 FCLK
007F C354h	FLASHCONST	Unique ID Register 1	UIDR1	32	32	2 or 3 FCLK
007F C358h	FLASHCONST	Unique ID Register 2	UIDR2	32	32	2 or 3 FCLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Port 4	V_{in}	-0.3 to AVCC0+0.3	V
	Except for port 4 and ports for 5 V tolerant*1		–0.3 to VCC+0.3	V
	Ports for 5 V tolerant*1		–0.3 to +6.5	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0+0.3	V
Analog power supply voltage		AVCC0	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN007 used	V_{AN}	–0.3 to AVCC0+0.3	V
	When AN016 and AN017 used		–0.3 to VCC+0.3	
Operating temperature*2		T_{opr}	–40 to +85 –40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.

The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports B1 and B2 are 5 V tolerant.

Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2		2.7	—	5.5	V
	VSS		—	0	—	
Analog power supply voltages	AVCC0*1, *2		VCC	—	5.5	V
	VREFH0*1, *2		—	AVCC0	—	
	AVSS0, VREFL0		—	0	—	

Note 1. AVCC0/VREFH0 and VCC can be set individually within the operating range.

Note 2. When powering on the VCC and AVCC0/VREFH0 pins, power them on at the same time or the VCC pin first and then the AVCC0/VREFH0 pin.

Table 5.10 DC Characteristics (8)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (2.7 V). When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 5.3 $V_{r\,(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 5.3 $V_{r\,(VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 5.3 $V_{r\,(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

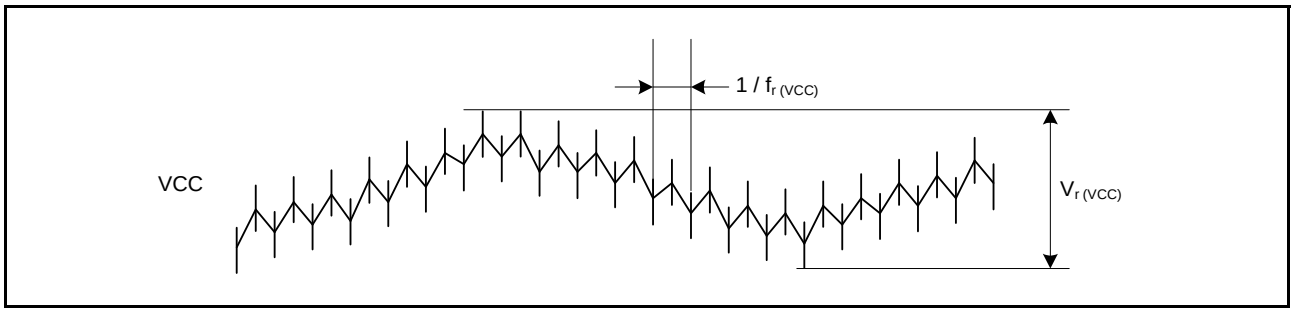


Figure 5.3 Ripple Waveform

Table 5.11 DC Characteristics (9)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	3.3	4.7	6.1	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

Table 5.12 Permissible Output Currents

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Max.	Unit
Permissible output low current	Large current ports (Ports 71 to 76, port B5, port D3)		I_{OL}	10.0	mA
	RIIC pins			6.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of large current ports		ΣI_{OL}	50	
	Total of all output pins			110	
Permissible output high current	Large current ports (Ports 71 to 76, port B5, port D3)		I_{OH}	–5.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of large current ports		ΣI_{OH}	–25	
	Total of all output pins			–35	

Note: Do not exceed the permissible total supply current.

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.8 to Figure 5.11 show the characteristics when high-drive output is selected by the drive capacity control register.

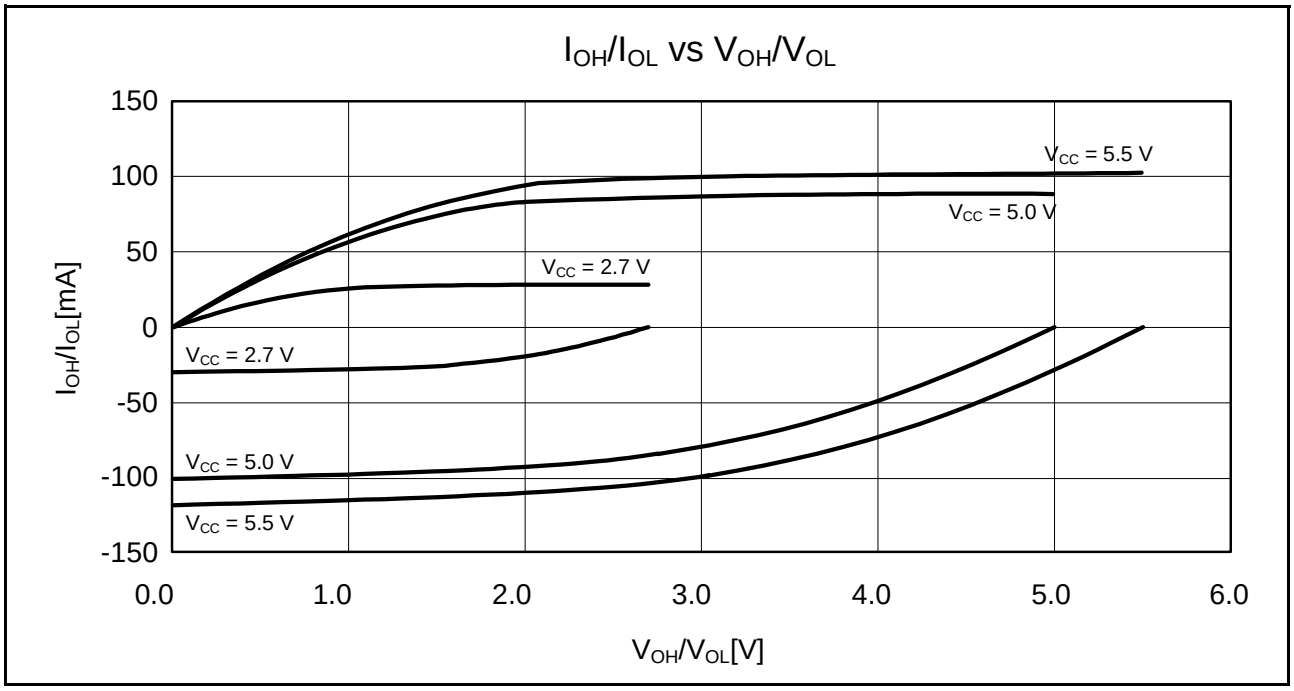


Figure 5.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

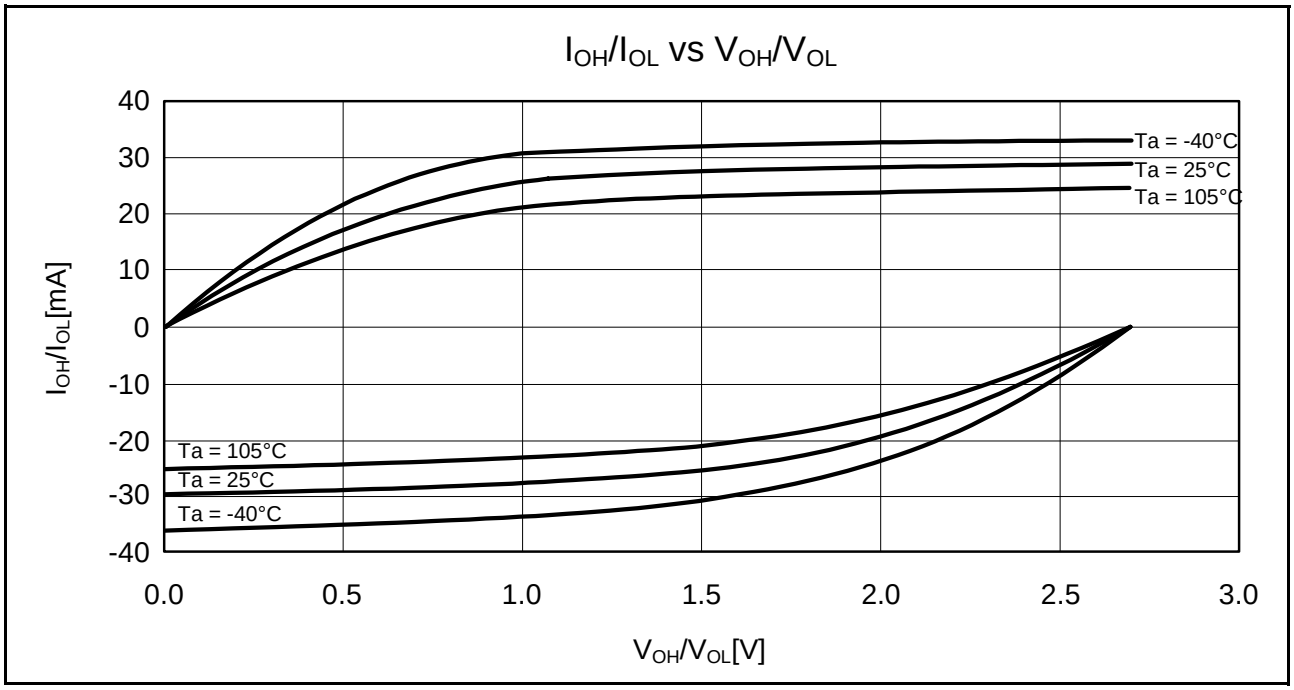


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

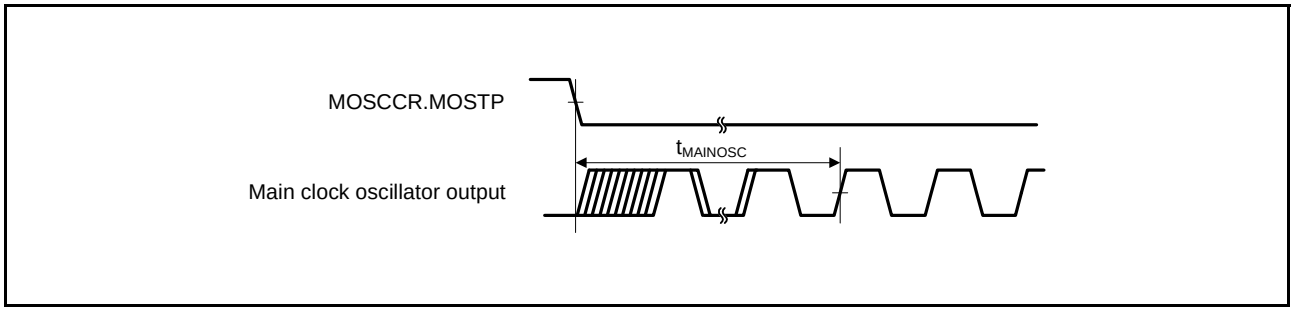


Figure 5.21 Main Clock Oscillation Start Timing

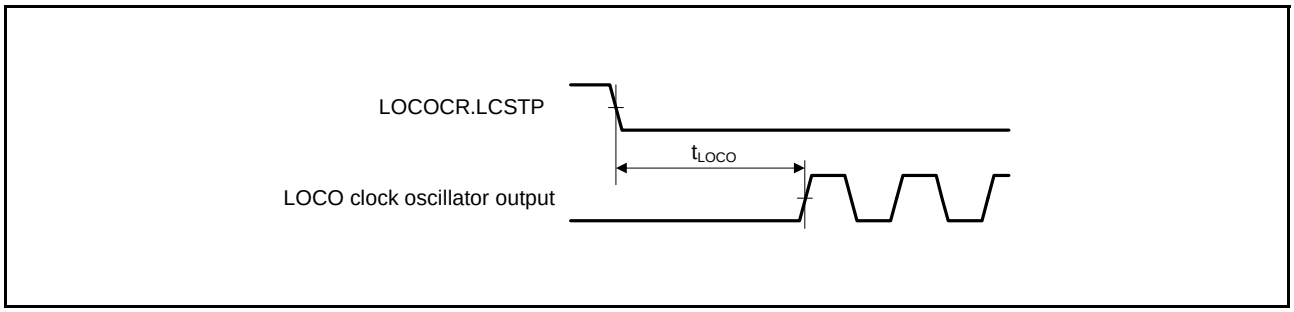


Figure 5.22 LOCO Clock Oscillation Start Timing

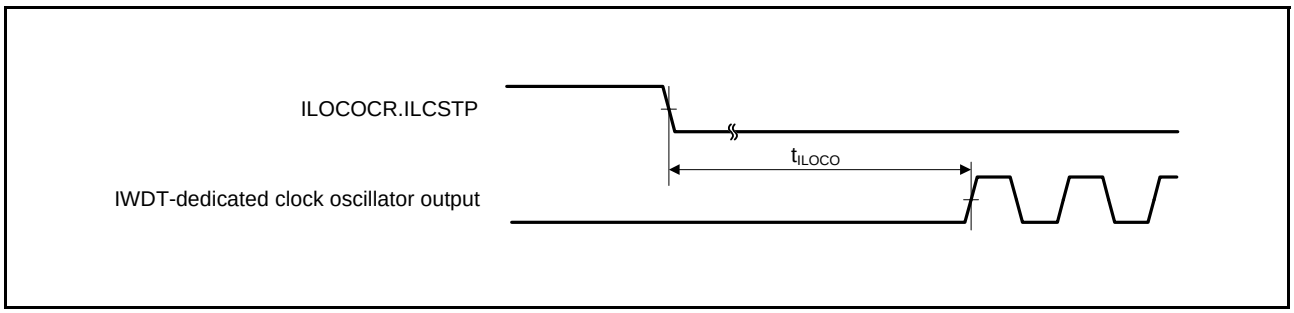


Figure 5.23 IWDT-Dedicated Clock Oscillation Start Timing

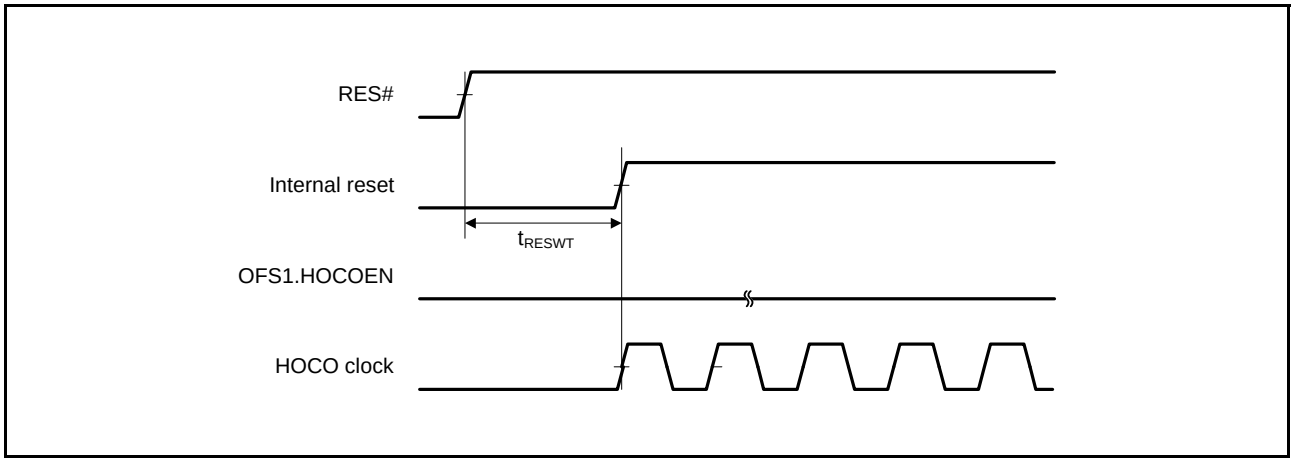


Figure 5.24 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

5.3.2 Reset Timing

Table 5.17 Reset Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.27
	Other than above	t_{RESW}	30	—	—	µs	Figure 5.28
Wait time after RES# cancellation (at power-on)		t_{RESWT}	—	27.5	—	ms	Figure 5.27
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	114	—	µs	Figure 5.28
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.29
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*1		t_{RESW2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESW2}	—	168	—	µs	

Note 1. When IWDTCR.CKS[3:0] = 0000b.

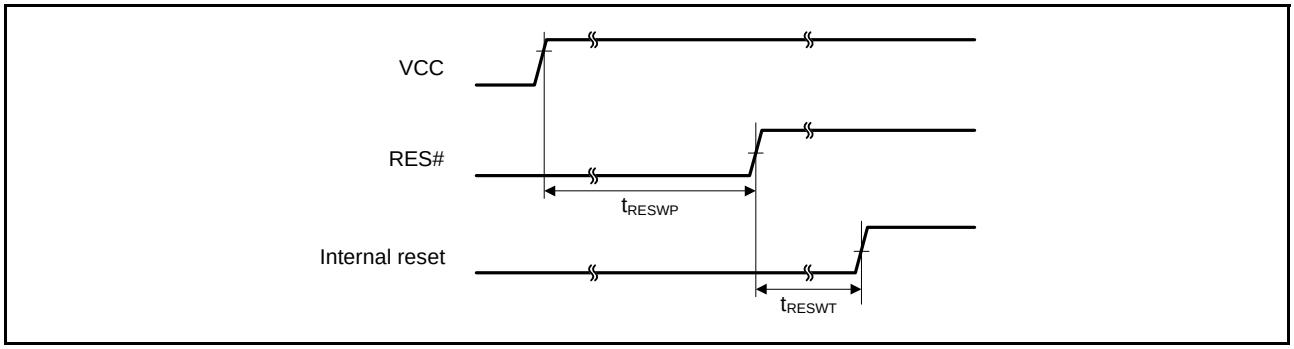


Figure 5.27 Reset Input Timing at Power-On

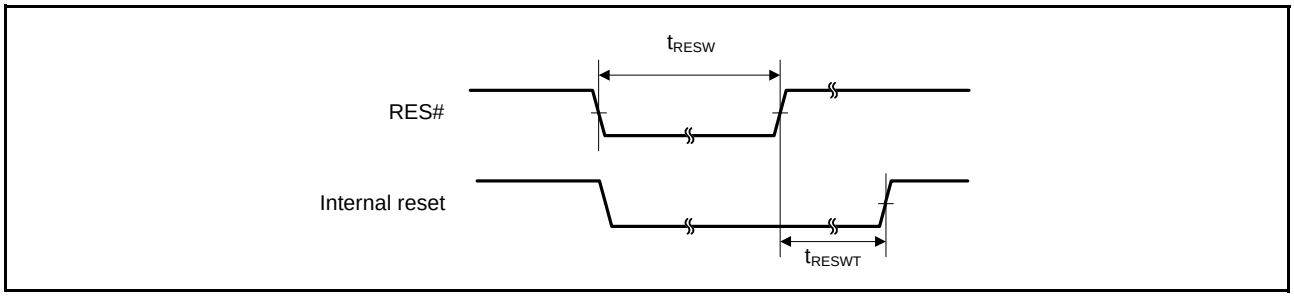


Figure 5.28 Reset Input Timing (1)

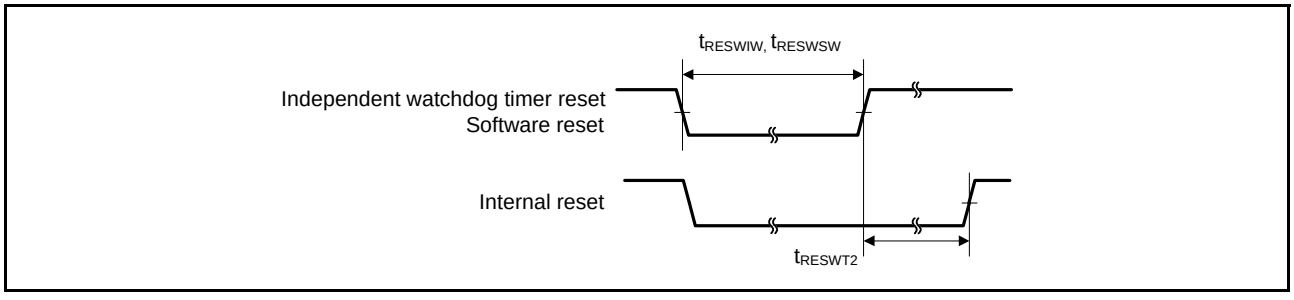


Figure 5.29 Reset Input Timing (2)

Table 5.25 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, C = 30pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.42
	SCK clock cycle input (slave)			6	65536	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC = 4.0 V or above	t_{SU}	40	—	ns	Figure 5.43, Figure 5.44
		VCC = 2.7 V or above		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC = 4.0 V or above		—	40		
		VCC = 2.7 V or above		—	65		
	Data output hold time (master)	Master	t_{OH}	–10	—	ns	
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.45, Figure 5.46
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

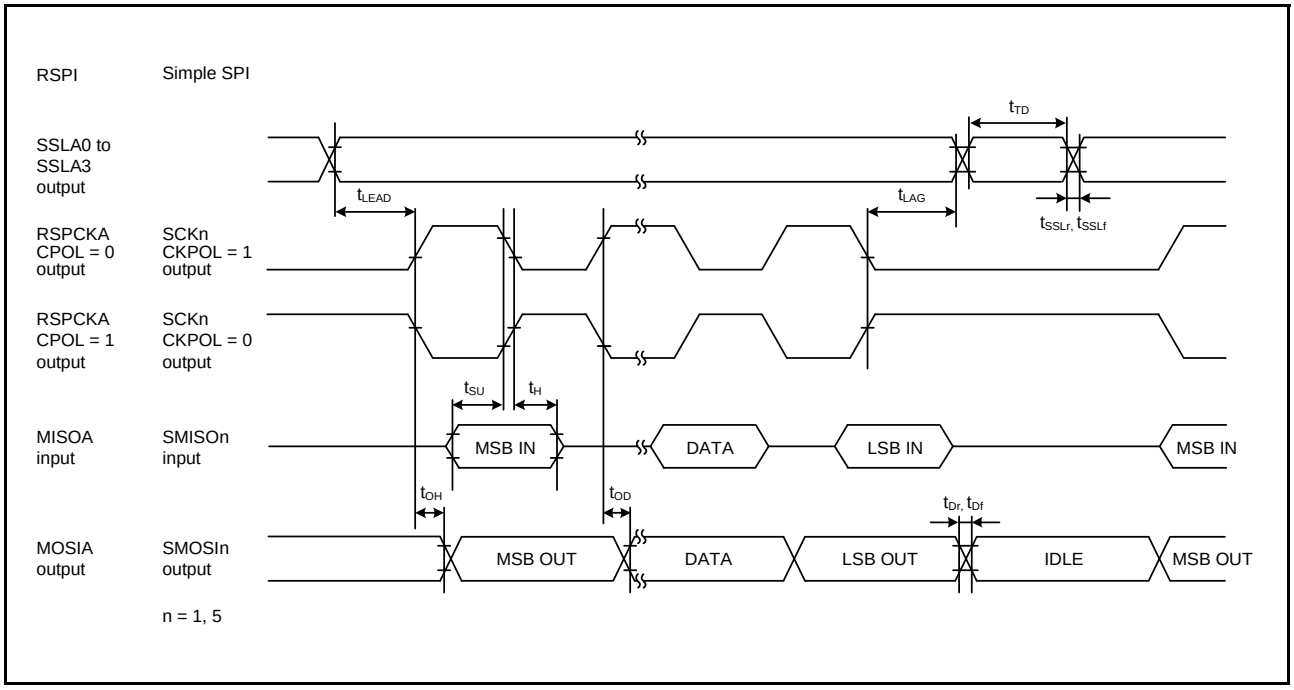


Figure 5.44 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

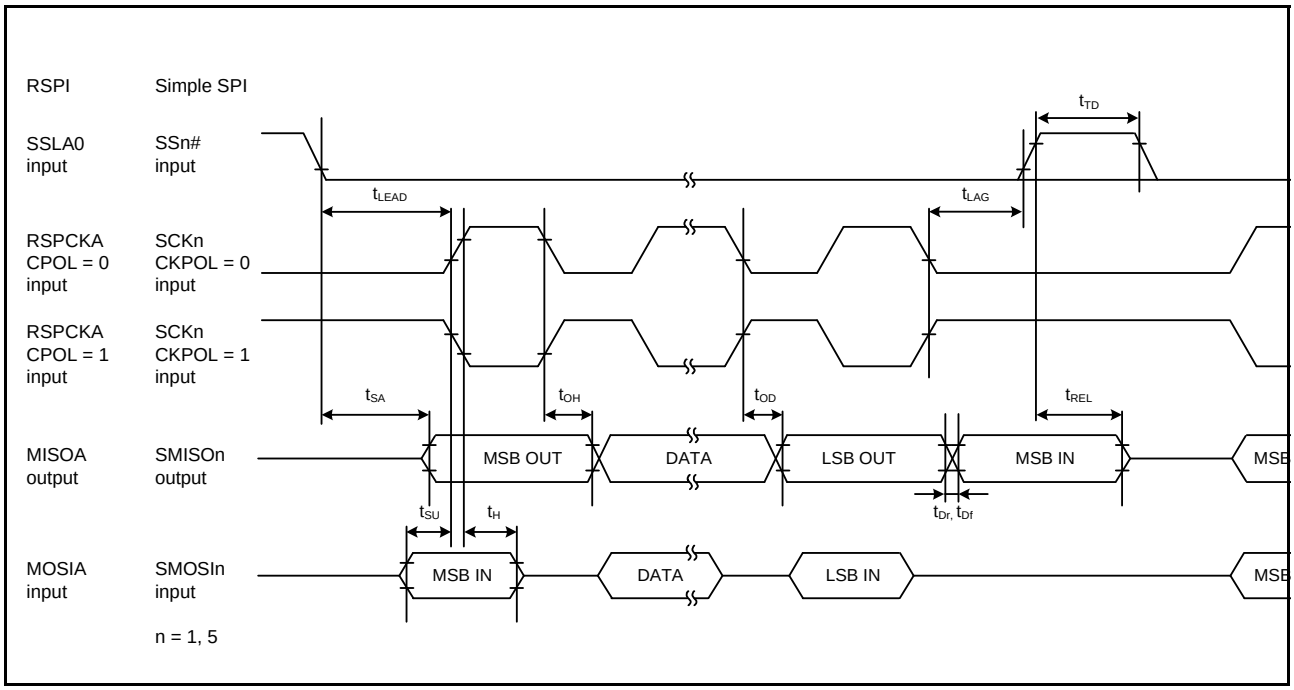


Figure 5.45 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

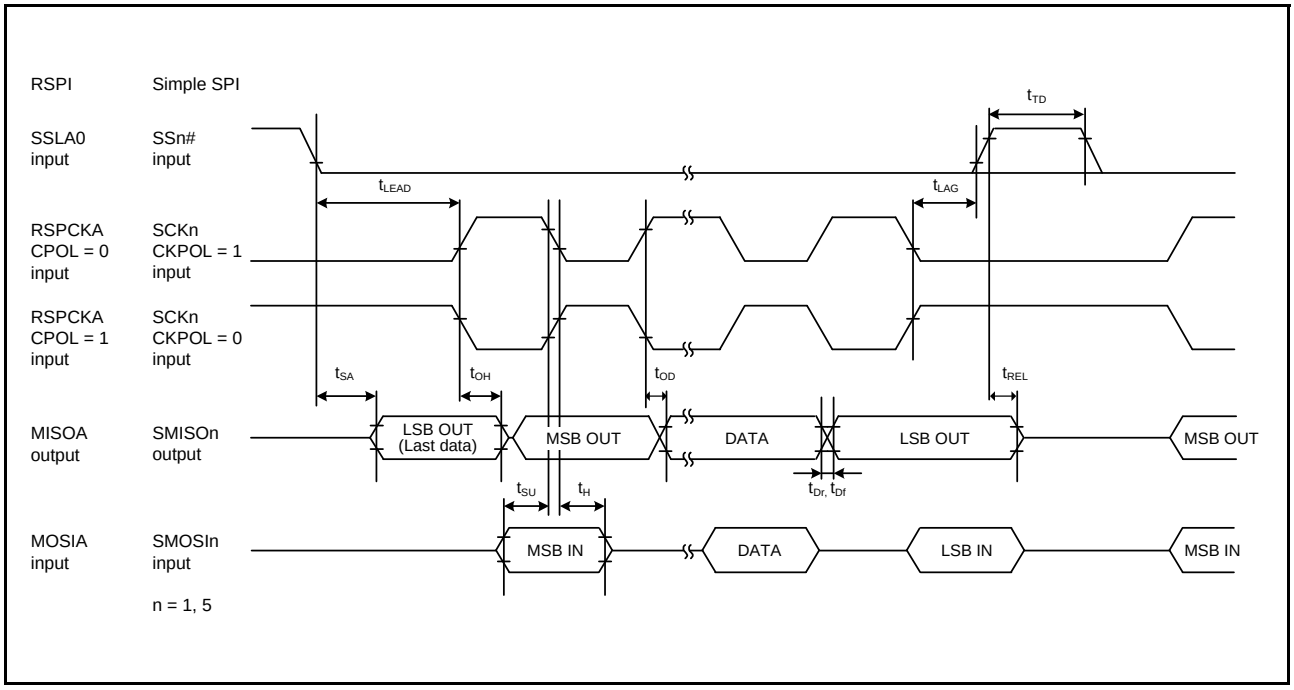


Figure 5.46 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

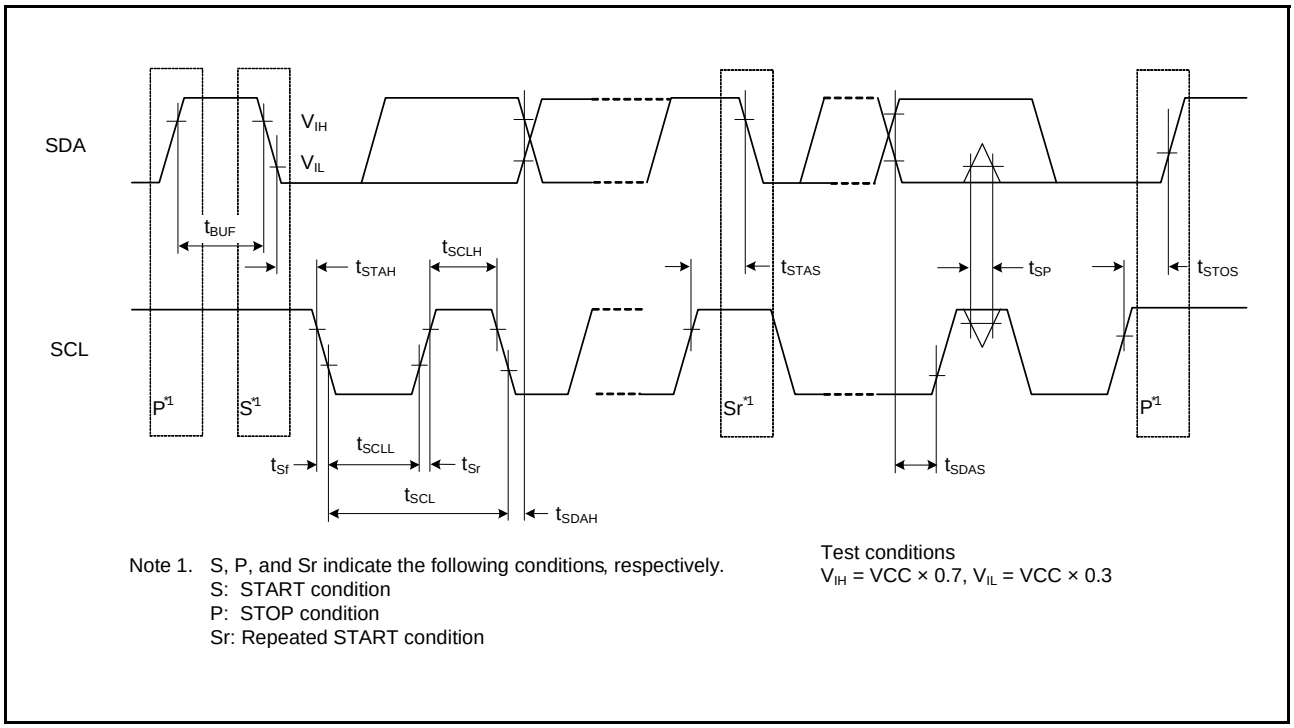


Figure 5.47 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.7 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.34 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

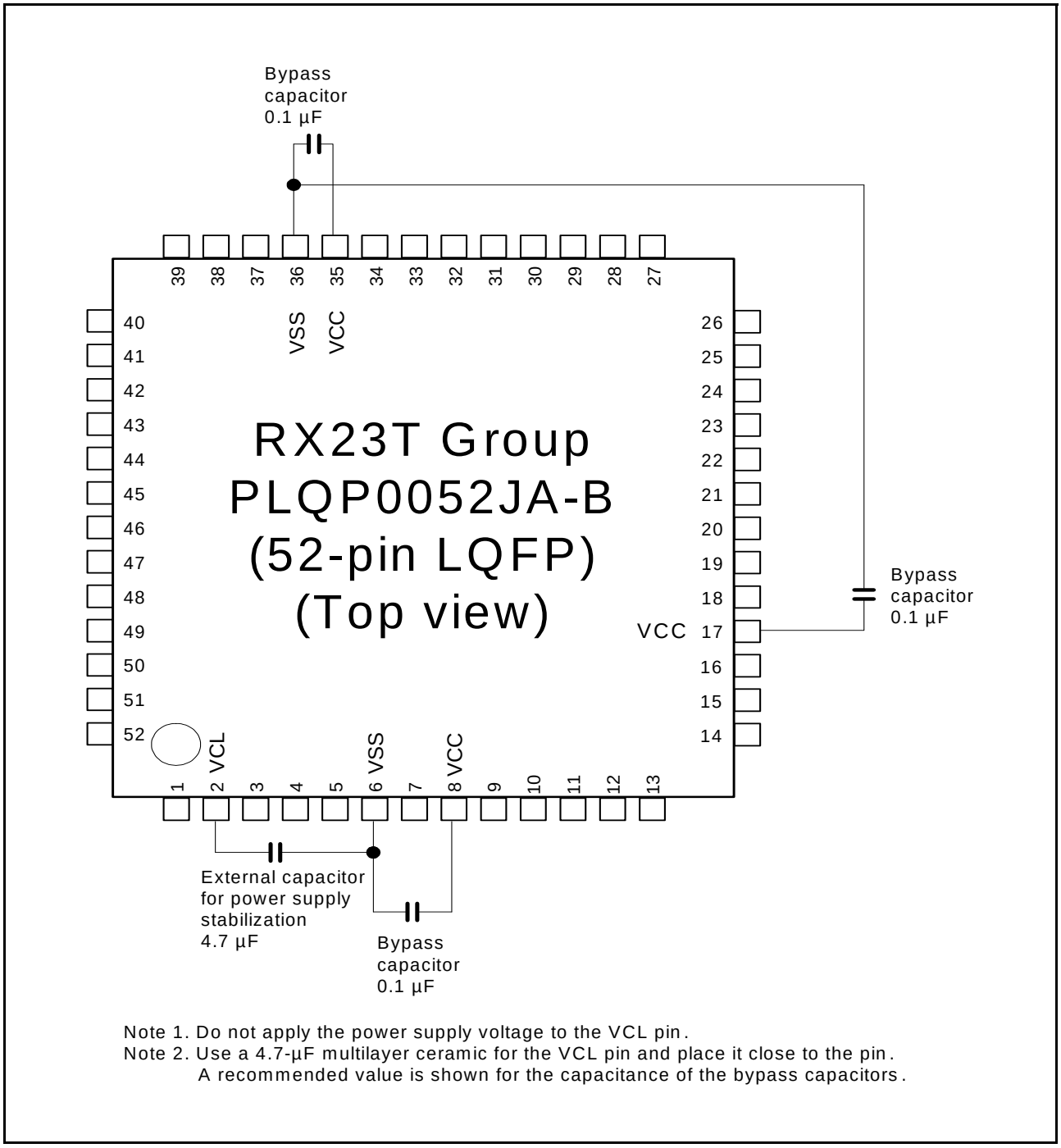
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 5.50, Figure 5.51
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97	V	
		V_{det0_2}	2.37	2.51	2.67		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 5.53 At falling edge VCC
		V_{det1_1}	3.98	4.14	4.28		
		V_{det1_2}	3.86	4.02	4.16		
		V_{det1_3}	3.68	3.84	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
	Voltage detection circuit (LVD2)*1	V_{det2_0}*2	4.08	4.29	4.48		Figure 5.54 At falling edge VCC
		V_{det2_1}	3.95	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet0_n denotes the value of the LVDS0[1:0] bits.

Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.



Note 1. Do not apply the power supply voltage to the VCL pin.
Note 2. Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.57 Connecting Capacitors (52 Pins)