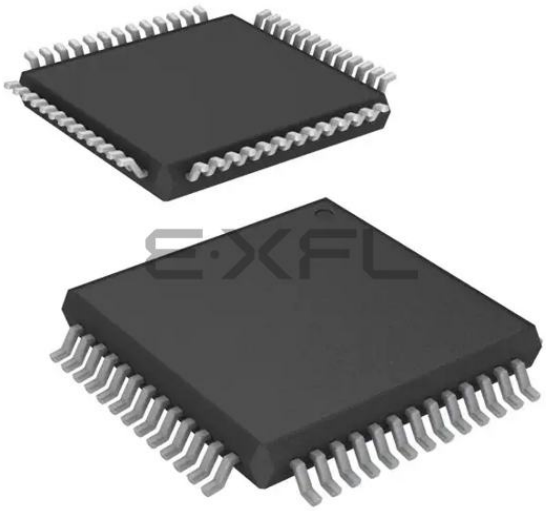

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 40MHz |
| Connectivity | I²C, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 52-LQFP |
| Supplier Device Package | 52-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f523t5adfd-30 |

**Table 1.1 Outline of Specifications (2/3)**

| Classification | Module/Function | Description |
|---|---|---|
| Interrupt | Interrupt controller (ICUb) | • Interrupt vectors: 83<br>• External interrupts: 7 (NMI, IRQ0 to IRQ5 pins)<br>• Non-maskable interrupts: 5 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt)<br>• 16 levels specifiable for the order of priority |
| DMA | Data transfer controller (DTCa) | • Transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Interrupts<br>• Chain transfer function |
| I/O ports | General I/O ports | 64-/52-/48-pin<br>• I/O: 50/40/37<br>• Input: 1/1/1<br>• Pull-up resistors: 50/40/37<br>• Open-drain outputs: 42/32/29<br>• 5-V tolerance: 2/2/2 |
| Multi-function pin controller (MPC) | | Capable of selecting the input/output function from multiple pins |
| Timers | Multi-function timer pulse unit 3 (MTU3c) | • 6 units (16bis × 6 channels)<br>• Provides up to 16 pulse-input/output lines and three pulse-input lines<br>• Select from among fourteen counter-input clock signals for each channel (PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, PCLK/32, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) other than channel 1/3/4, for which only eleven signals are available, channel 2 for 12, channel 5 for 10<br>• 26 output compare/input capture registers<br>• Counter clear operation (with compare match- or input capture-sourced simultaneous counter clear capability)<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Simultaneous register input/output by synchronous counter operation<br>• Buffer operation<br>• Cascaded operation<br>• 28 interrupt sources<br>• Automatic transfer of register data<br>• Pulse output modes: Toggle/PWM/complementary PWM/reset-synchronized PWM<br>• Complementary PWM output mode<br>3-phase non-overlapping waveform output for inverter control<br>Automatic dead time setting<br>Adjustable PWM duty cycle: from 0 to 100%<br>A/D conversion request delaying function<br>Interrupt at crest/trough can be skipped<br>Double buffer function<br>• Reset-synchronized PWM mode<br>Outputs three phases each for positive and negative PWM waveforms in user-specified duty cycle<br>• Phase counting modes: 16-bit mode (channel 1 and 2)/32-bit mode (channel 1 and 2)<br>• Dead time compensation counter function<br>• A/D converter start trigger can be generated<br>• A/D converter start triggers can be skipped<br>• Signals from the input capture and external counter clock pins are input via a digital filter |
| | Port output enable 3 (POE3b) | Controls the high-impedance state of the MTU's waveform output pins |
| | Compare match timer (CMT) | • (16 bits × 2 channels) × 2 units<br>• Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) |
| | Independent watchdog timer (IWDTa) | • 14 bits × 1 channel<br>• Count clock: Dedicated low-speed on-chip oscillator for the IWDT<br>Frequency divided by 1, 16, 32, 64, 128, or 256 |
| | 8-bit timer (TMR) | • (8 bits × 2 channels) × 2 units<br>• Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected<br>• Pulse output and PWM output with any duty cycle are available<br>• Two channels can be cascaded and used as a 16-bit timer<br>• Generates A/D conversion start trigger<br>• Generates baud rate clock for the SCI5 |

**Table 1.2 Comparison of Functions for Different Packages**

| Module/Functions | | RX23T Group | | |
|---|---|---|---|---|
| | | **48 Pins** | **52 Pins** | **64 Pins** |
| Interrupts | External interrupts | NMI, IRQ0 to IRQ5 | | |
| DTC | Data transfer controller | Available | | |
| Timers | Multi-function timer pulse unit 3*1 | 6 channels | | |
| | Port output enable 3 | POE0# to POE8#, POE10# | | |
| | 8-bit timer | 2 channels × 2 units | | |
| | Compare match timer | 2 channels × 2 units | | |
| | Independent watchdog timer | Available | | |
| Communication functions | Serial communications interfaces (SCIg) [including simple IIC and simple SPI] | 2 channels (SCI1, 5) | | |
| | $I^2C$ bus interface | 1 channel | | |
| | Serial peripheral interface | 1 channel | | |
| 12-bit A/D converter (including high-precision channels) | | 10 channels (8 channels) | | |
| CRC calculator | | Available | | |
| Packages | | 48-pin LFQFP | 52-pin LQFP | 64-pin LFQFP |

Note 1. For multi-function timer pulse unit 3, the number of pins differs depending on the package. For details, see the "List of Pins and Pin Functions" table for each pin.

**Table 1.7 List of Pins and Pin Functions (52-Pin LQFP)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE, CAC) | Communications (SCIg, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| 1 | | P02 | | CTS1#/RTS1#/SS1# | ADST0/IRQ5 |
| 2 | VCL | | | | |
| 3 | MD | | | | FINED |
| 4 | RES# | | | | |
| 5 | XTAL | P37 | | | |
| 6 | VSS | | | | |
| 7 | EXTAL | P36 | | | |
| 8 | VCC | | | | |
| 9 | | PE2 | POE10# | | NMI |
| 10 | | PD6 | TMO1 | SSLA0/CTS1#/RTS1#/SS1# | ADST0/IRQ5 |
| 11 | | PD5 | TMRI0 | RXD1/SMISO1/SSCL1 | IRQ3 |
| 12 | | PD4 | TMCI0 | SCK1 | IRQ2 |
| 13 | | PD3 | TMO0 | TXD1/SMOSI1/SSDA1 | |
| 14 | | PB7 | | SCK5 | |
| 15 | | PB6 | | RXD5/SMISO5/SSCL5 | IRQ5 |
| 16 | | PB5 | | TXD5/SMOSI5/SSDA5 | |
| 17 | VCC | | | | |
| 18 | | PB4 | POE8# | | IRQ3 |
| 19 | | PB3 | MTIOC0A/CACREF | SCK5/RSPCKA | |
| 20 | | PB2 | MTIOC0B/ADSM0 | TXD5/SMOSI5/SSDA5/SDA0 | |
| 21 | | PB1 | MTIOC0C | RXD5/SMISO5/SSCL5/SCL0 | IRQ2 |
| 22 | | PB0 | MTIOC0D | MOSIA | |
| 23 | | PA3 | MTIOC2A | SSLA0 | |
| 24 | | PA2 | MTIOC2B | CTS5#/RTS5#/SS5#/SSLA1 | IRQ4 |
| 25 | | P94 | MTIOC0C/TMO1 | MISOA | IRQ1 |
| 26 | | P93 | MTIOC0B/TMRI1 | SCK5/RSPCKA | IRQ0 |
| 27 | | P76 | MTIOC4D | | |
| 28 | | P75 | MTIOC4C | | |
| 29 | | P74 | MTIOC3D | | |
| 30 | | P73 | MTIOC4B | | |
| 31 | | P72 | MTIOC4A | | |
| 32 | | P71 | MTIOC3B | | |
| 33 | | P70 | POE0# | | IRQ5 |
| 34 | | P33 | MTIOC3A/MTCLKA | SSLA3 | |
| 35 | VCC | | | | |
| 36 | VSS | | | | |
| 37 | | P24 | MTIC5U/TMCI2 | RSPCKA | COMP0/IRQ3 |
| 38 | | P23 | MTIC5V/CACREF/TMO2 | MOSIA | COMP1/IRQ4 |
| 39 | | P22 | MTIC5W/TMRI2 | MISOA | COMP2/IRQ2 |
| 40 | | P47 | | | AN007/CMPC12/ CMPC22 |
| 41 | | P46 | | | AN006/CMPC02 |
| 42 | | P45 | | | AN005/CMPC21 |
| 43 | | P44 | | | AN004/CMPC11 |
| 44 | | P43 | | | AN003/CMPC01 |
| 45 | | P42 | | | AN002/CMPC20 |
| 46 | | P41 | | | AN001/CMPC10 |
| 47 | | P40 | | | AN000/CMPC00 |
| 48 | AVCC0 | | | | |
| 49 | AVSS0 | | | | |
| 50 | | P11 | MTIOC3A/MTCLKC/TMO3 | | IRQ1/AN016/ CVREFC0 |
| 51 | | P10 | MTCLKD/TMRI3 | | IRQ0/AN017/ CVREFC1 |
| 52 | | PA5 | MTIOC1A/TMCI3 | MISOA | |

**Table 1.8 List of Pins and Pin Functions (48-Pin LFQFP)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE, CAC) | Communications (SCIg, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| 1 | VCL | | | | |
| 2 | MD | | | | FINED |
| 3 | RES# | | | | |
| 4 | XTAL | P37 | | | |
| 5 | VSS | | | | |
| 6 | EXTAL | P36 | | | |
| 7 | VCC | | | | |
| 8 | | PE2 | POE10# | | NMI |
| 9 | | PD6 | TMO1 | SSLA0/CTS1#/RTS1#/SS1# | ADST0/IRQ5 |
| 10 | | PD5 | TMRI0 | RXD1/SMISO1/SSCL1 | IRQ3 |
| 11 | | PD4 | TMCI0 | SCK1 | IRQ2 |
| 12 | | PD3 | TMO0 | TXD1/SMOSI1/SSDA1 | |
| 13 | | PB6 | | RXD5/SMISO5/SSCL5 | IRQ5 |
| 14 | | PB5 | | TXD5/SMOSI5/SSDA5 | |
| 15 | VCC | | | | |
| 16 | | PB4 | POE8# | | IRQ3 |
| 17 | | PB3 | MTIOC0A/CACREF | SCK5/RSPCKA | |
| 18 | | PB2 | MTIOC0B/ADSM0 | TXD5/SMOSI5/SSDA5/SDA0 | |
| 19 | | PB1 | MTIOC0C | RXD5/SMISO5/SSCL5/SCL0 | IRQ2 |
| 20 | | PB0 | MTIOC0D | MOSIA | |
| 21 | | PA3 | MTIOC2A | SSLA0 | |
| 22 | | PA2 | MTIOC2B | CTS5#/RTS5#/SS5#/SSLA1 | IRQ4 |
| 23 | | P94 | MTIOC0C/TMO1 | MISOA | IRQ1 |
| 24 | | P93 | MTIOC0B/TMRI1 | SCK5/RSPCKA | IRQ0 |
| 25 | | P76 | MTIOC4D | | |
| 26 | | P75 | MTIOC4C | | |
| 27 | | P74 | MTIOC3D | | |
| 28 | | P73 | MTIOC4B | | |
| 29 | | P72 | MTIOC4A | | |
| 30 | | P71 | MTIOC3B | | |
| 31 | | P70 | POE0# | | IRQ5 |
| 32 | VCC | | | | |
| 33 | VSS | | | | |
| 34 | | P24 | MTIC5U/TMCI2 | RSPCKA | COMP0/IRQ3 |
| 35 | | P23 | MTIC5V/CACREF/TMO2 | MOSIA | COMP1/IRQ4 |
| 36 | | P22 | MTIC5W/TMRI2 | MISOA | COMP2/IRQ2 |
| 37 | | P47 | | | AN007/CMPC12/ CMPC22 |
| 38 | | P46 | | | AN006/CMPC02 |
| 39 | | P45 | | | AN005/CMPC21 |
| 40 | | P44 | | | AN004/CMPC11 |
| 41 | | P43 | | | AN003/CMPC01 |
| 42 | | P42 | | | AN002/CMPC20 |
| 43 | | P41 | | | AN001/CMPC10 |
| 44 | | P40 | | | AN000/CMPC00 |
| 45 | AVCC0 | | | | |
| 46 | AVSS0 | | | | |
| 47 | | P11 | MTIOC3A/MTCLKC/TMO3 | | IRQ1/AN016/ CVREFC0 |
| 48 | | P10 | MTCLKD/TMRI3 | | IRQ0/AN017/ CVREFC1 |

# 4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

## (1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

## (2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

**[Examples of cases requiring special care]**

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

**Table 4.1 List of I/O Registers (Address Order) (2 / 16)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK |
|---|---|---|---|---|---|---|
| 0008 642Ch | MPU | Region-5 End Page Number Register | REPAGE5 | 32 | 32 | 1 ICLK |
| 0008 6430h | MPU | Region-6 Start Page Number Register | RSPAGE6 | 32 | 32 | 1 ICLK |
| 0008 6434h | MPU | Region-6 End Page Number Register | REPAGE6 | 32 | 32 | 1 ICLK |
| 0008 6438h | MPU | Region-7 Start Page Number Register | RSPAGE7 | 32 | 32 | 1 ICLK |
| 0008 643Ch | MPU | Region-7 End Page Number Register | REPAGE7 | 32 | 32 | 1 ICLK |
| 0008 6500h | MPU | Memory-Protection Enable Register | MPEN | 32 | 32 | 1 ICLK |
| 0008 6504h | MPU | Background Access Control Register | MPBAC | 32 | 32 | 1 ICLK |
| 0008 6508h | MPU | Memory-Protection Error Status-Clearing Register | MPECLR | 32 | 32 | 1 ICLK |
| 0008 650Ch | MPU | Memory-Protection Error Status Register | MPESTS | 32 | 32 | 1 ICLK |
| 0008 6514h | MPU | Data Memory-Protection Error Address Register | MPDEA | 32 | 32 | 1 ICLK |
| 0008 6520h | MPU | Region Search Address Register | MPSA | 32 | 32 | 1 ICLK |
| 0008 6524h | MPU | Region Search Operation Register | MPOPS | 16 | 16 | 1 ICLK |
| 0008 6526h | MPU | Region Invalidation Operation Register | MPOPI | 16 | 16 | 1 ICLK |
| 0008 6528h | MPU | Instruction-Hit Region Register | MHITI | 32 | 32 | 1 ICLK |
| 0008 652Ch | MPU | Data-Hit Region Register | MHITD | 32 | 32 | 1 ICLK |
| 0008 7010h | ICU | Interrupt Request Register 016 | IR016 | 8 | 8 | 2 ICLK |
| 0008 7017h | ICU | Interrupt Request Register 023 | IR023 | 8 | 8 | 2 ICLK |
| 0008 701Bh | ICU | Interrupt Request Register 027 | IR027 | 8 | 8 | 2 ICLK |
| 0008 701Ch | ICU | Interrupt Request Register 028 | IR028 | 8 | 8 | 2 ICLK |
| 0008 701Dh | ICU | Interrupt Request Register 029 | IR029 | 8 | 8 | 2 ICLK |
| 0008 701Eh | ICU | Interrupt Request Register 030 | IR030 | 8 | 8 | 2 ICLK |
| 0008 701Fh | ICU | Interrupt Request Register 031 | IR031 | 8 | 8 | 2 ICLK |
| 0008 7020h | ICU | Interrupt Request Register 032 | IR032 | 8 | 8 | 2 ICLK |
| 0008 7021h | ICU | Interrupt Request Register 033 | IR033 | 8 | 8 | 2 ICLK |
| 0008 7022h | ICU | Interrupt Request Register 034 | IR034 | 8 | 8 | 2 ICLK |
| 0008 702Ch | ICU | Interrupt Request Register 044 | IR044 | 8 | 8 | 2 ICLK |
| 0008 702Dh | ICU | Interrupt Request Register 045 | IR045 | 8 | 8 | 2 ICLK |
| 0008 702Eh | ICU | Interrupt Request Register 046 | IR046 | 8 | 8 | 2 ICLK |
| 0008 702Fh | ICU | Interrupt Request Register 047 | IR047 | 8 | 8 | 2 ICLK |
| 0008 7039h | ICU | Interrupt Request Register 057 | IR057 | 8 | 8 | 2 ICLK |
| 0008 7040h | ICU | Interrupt Request Register 064 | IR064 | 8 | 8 | 2 ICLK |
| 0008 7041h | ICU | Interrupt Request Register 065 | IR065 | 8 | 8 | 2 ICLK |
| 0008 7042h | ICU | Interrupt Request Register 066 | IR066 | 8 | 8 | 2 ICLK |
| 0008 7043h | ICU | Interrupt Request Register 067 | IR067 | 8 | 8 | 2 ICLK |
| 0008 7044h | ICU | Interrupt Request Register 068 | IR068 | 8 | 8 | 2 ICLK |
| 0008 7045h | ICU | Interrupt Request Register 069 | IR069 | 8 | 8 | 2 ICLK |
| 0008 7058h | ICU | Interrupt Request Register 088 | IR088 | 8 | 8 | 2 ICLK |
| 0008 7059h | ICU | Interrupt Request Register 089 | IR089 | 8 | 8 | 2 ICLK |
| 0008 7066h | ICU | Interrupt Request Register 102 | IR102 | 8 | 8 | 2 ICLK |
| 0008 7067h | ICU | Interrupt Request Register 103 | IR103 | 8 | 8 | 2 ICLK |
| 0008 706Ch | ICU | Interrupt Request Register 108 | IR108 | 8 | 8 | 2 ICLK |
| 0008 706Dh | ICU | Interrupt Request Register 109 | IR109 | 8 | 8 | 2 ICLK |
| 0008 706Eh | ICU | Interrupt Request Register 110 | IR110 | 8 | 8 | 2 ICLK |
| 0008 7072h | ICU | Interrupt Request Register 114 | IR114 | 8 | 8 | 2 ICLK |
| 0008 7073h | ICU | Interrupt Request Register 115 | IR115 | 8 | 8 | 2 ICLK |
| 0008 7074h | ICU | Interrupt Request Register 116 | IR116 | 8 | 8 | 2 ICLK |
| 0008 7075h | ICU | Interrupt Request Register 117 | IR117 | 8 | 8 | 2 ICLK |
| 0008 7076h | ICU | Interrupt Request Register 118 | IR118 | 8 | 8 | 2 ICLK |
| 0008 7077h | ICU | Interrupt Request Register 119 | IR119 | 8 | 8 | 2 ICLK |
| 0008 7078h | ICU | Interrupt Request Register 120 | IR120 | 8 | 8 | 2 ICLK |
| 0008 7079h | ICU | Interrupt Request Register 121 | IR121 | 8 | 8 | 2 ICLK |
| 0008 707Ah | ICU | Interrupt Request Register 122 | IR122 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (7 / 16)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK |
|---|---|---|---|---|---|---|
| 0008 8205h | TMR1 | Time Constant Register A | TCORA | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8206h | TMR0 | Time Constant Register B | TCORB | 8 | 8 | 2 or 3 PCLKB |
| 0008 8207h | TMR1 | Time Constant Register B | TCORB | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8208h | TMR0 | Timer Counter | TCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8209h | TMR1 | Timer Counter | TCNT | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 820Ah | TMR0 | Timer Counter Control Register | TCCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 820Bh | TMR1 | Timer Counter Control Register | TCCR | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8210h | TMR2 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8211h | TMR3 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8212h | TMR2 | Timer Control/Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8213h | TMR3 | Timer Control/Status Register | TCSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8214h | TMR2 | Time Constant Register A | TCORA | 8 | 8 | 2 or 3 PCLKB |
| 0008 8215h | TMR3 | Time Constant Register A | TCORA | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8216h | TMR2 | Time Constant Register B | TCORB | 8 | 8 | 2 or 3 PCLKB |
| 0008 8217h | TMR3 | Time Constant Register B | TCORB | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8218h | TMR2 | Timer Counter | TCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8219h | TMR3 | Timer Counter | TCNT | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 821Ah | TMR2 | Timer Counter Control Register | TCCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 821Bh | TMR3 | Timer Counter Control Register | TCCR | 8 | 8*1 | 2 or 3 PCLKB |
| 0008 8280h | CRC | CRC Control Register | CRCCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8281h | CRC | CRC Data Input Register | CRCDIR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8282h | CRC | CRC Data Output Register | CRCDOR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8300h | RIIC0 | $I^2C$ Bus Control Register 1 | ICCR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8301h | RIIC0 | $I^2C$ Bus Control Register 2 | ICCR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8302h | RIIC0 | $I^2C$ Bus Mode Register 1 | ICMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8303h | RIIC0 | $I^2C$ Bus Mode Register 2 | ICMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8304h | RIIC0 | $I^2C$ Bus Mode Register 3 | ICMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8305h | RIIC0 | $I^2C$ Bus Function Enable Register | ICFER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8306h | RIIC0 | $I^2C$ Bus Status Enable Register | ICSER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8307h | RIIC0 | $I^2C$ Bus Interrupt Enable Register | ICIER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8308h | RIIC0 | $I^2C$ Bus Status Register 1 | ICSR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8309h | RIIC0 | $I^2C$ Bus Status Register 2 | ICSR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Ah | RIIC0 | Slave Address Register L0 | SARL0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Bh | RIIC0 | Slave Address Register U0 | SARU0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Ch | RIIC0 | Slave Address Register L1 | SARL1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Dh | RIIC0 | Slave Address Register U1 | SARU1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Eh | RIIC0 | Slave Address Register L2 | SARL2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Fh | RIIC0 | Slave Address Register U2 | SARU2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8310h | RIIC0 | $I^2C$ Bus Bit Rate Low-Level Register | ICBRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 8311h | RIIC0 | $I^2C$ Bus Bit Rate High-Level Register | ICBRH | 8 | 8 | 2 or 3 PCLKB |
| 0008 8312h | RIIC0 | $I^2C$ Bus Transmit Data Register | ICDRT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8313h | RIIC0 | $I^2C$ Bus Receive Data Register | ICDRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8380h | RSPI0 | RSPI Control Register | SPCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8381h | RSPI0 | RSPI Slave Select Polarity Register | SSLP | 8 | 8 | 2 or 3 PCLKB |
| 0008 8382h | RSPI0 | RSPI Pin Control Register | SPPCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8383h | RSPI0 | RSPI Status Register | SPSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8384h | RSPI0 | RSPI Data Register | SPDR | 32 | 16, 32 | 2 or 3 PCLKB |
| 0008 8388h | RSPI0 | RSPI Sequence Control Register | SPSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8389h | RSPI0 | RSPI Sequence Status Register | SPSSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Ah | RSPI0 | RSPI Bit Rate Register | SPBR | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Bh | RSPI0 | RSPI Data Control Register | SPDCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Ch | RSPI0 | RSPI Clock Delay Register | SPCKD | 8 | 8 | 2 or 3 PCLKB |

**Table 4.1 List of I/O Registers (Address Order) (13 / 16)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK |
| 000A 0CACh | CMPC1 | Comparator Output Monitor Register 1 | CMPMON | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CB0h | CMPC1 | Comparator External Output Enable Register 1 | CMPIOC | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CC0h | CMPC2 | Comparator Control Register 2 | CMPCTL | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CC4h | CMPC2 | Comparator Input Select Register 2 | CMPSEL0 | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CC8h | CMPC2 | Comparator Reference Voltage Select Register 2 | CMPSEL1 | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CCCh | CMPC2 | Comparator Output Monitor Register 2 | CMPMON | 8 | 8 | 1 or 2 PCLKB |
| 000A 0CD0h | CMPC2 | Comparator External Output Enable Register 2 | CMPIOC | 8 | 8 | 1 or 2 PCLKB |
| 000C 1200h | MTU3 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1201h | MTU4 | Timer Control Register | TCR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1202h | MTU3 | Timer Mode Register 1 | TMDR1 | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1203h | MTU4 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1204h | MTU3 | Timer I/O Control Register H | TIORH | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1205h | MTU3 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 or 5 PCLKA |
| 000C 1206h | MTU4 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1207h | MTU4 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 or 5 PCLKA |
| 000C 1208h | MTU3 | Timer Interrupt Enable Register | TIER | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1209h | MTU4 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4 or 5 PCLKA |
| 000C 120Ah | MTU | Timer Output Master Enable Register A | TOERA | 8 | 8 | 4 or 5 PCLKA |
| 000C 120Dh | MTU | Timer Gate Control Register | TGCRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 120Eh | MTU | Timer Output Control Register 1A | TOCR1A | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 120Fh | MTU | Timer Output Control Register 2A | TOCR2A | 8 | 8 | 4 or 5 PCLKA |
| 000C 1210h | MTU3 | Timer Counter | TCNT | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1212h | MTU4 | Timer Counter | TCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 1214h | MTU | Timer Cycle Data Register A | TCDRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1216h | MTU | Timer Dead Time Data Register A | TDDRA | 16 | 16 | 4 or 5 PCLKA |
| 000C 1218h | MTU3 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 121Ah | MTU3 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 121Ch | MTU4 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 121Eh | MTU4 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1220h | MTU | Timer Subcounters A | TCNTSA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1222h | MTU | Timer Cycle Buffer Register A | TCBRA | 16 | 16 | 4 or 5 PCLKA |
| 000C 1224h | MTU3 | Timer General Register C | TGRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1226h | MTU3 | Timer General Register D | TGRD | 16 | 16 | 4 or 5 PCLKA |
| 000C 1228h | MTU4 | Timer General Register C | TGRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 122Ah | MTU4 | Timer General Register D | TGRD | 16 | 16 | 4 or 5 PCLKA |
| 000C 122Ch | MTU3 | Timer Status Register | TSR | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 122Dh | MTU4 | Timer Status Register | TSR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1230h | MTU | Timer Interrupt Skipping Set Register 1A | TITCR1A | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1231h | MTU | Timer Interrupt Skipping Counters 1A | TITCNT1A | 8 | 8 | 4 or 5 PCLKA |
| 000C 1232h | MTU | Timer Buffer Transfer Set Register A | TBTERA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1234h | MTU | Timer Dead Time Enable Register A | TDERA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1236h | MTU | Timer Output Level Buffer Register A | TOLBRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1238h | MTU3 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1239h | MTU4 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 or 5 PCLKA |
| 000C 123Ah | MTU | Timer Interrupt Skipping Mode Register A | TITMRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 123Bh | MTU | Timer Interrupt Skipping Set Register 2A | TITCR2A | 8 | 8 | 4 or 5 PCLKA |
| 000C 123Ch | MTU | Timer Interrupt Skipping Counters 2A | TITCNT2A | 8 | 8 | 4 or 5 PCLKA |
| 000C 1240h | MTU4 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 4 or 5 PCLKA |
| 000C 1244h | MTU4 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1246h | MTU4 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1248h | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16, 32 | 4 or 5 PCLKA |

**Table 4.1 List of I/O Registers (Address Order) (14 / 16)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK |
| 000C 124Ah | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 124Ch | MTU3 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 124Dh | MTU4 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1260h | MTU | Timer Waveform Control Register A | TWCRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1270h | MTU | Timer Mode Register 2A | TMDR2A | 8 | 8 | 4 or 5 PCLKA |
| 000C 1272h | MTU3 | Timer General Register E | TGRE | 16 | 16 | 4 or 5 PCLKA |
| 000C 1274h | MTU4 | Timer General Register E | TGRE | 16 | 16 | 4 or 5 PCLKA |
| 000C 1276h | MTU4 | Timer General Register F | TGRF | 16 | 16 | 4 or 5 PCLKA |
| 000C 1280h | MTU | Timer Start Register A | TSTRA | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1281h | MTU | Timer Synchronous Register A | TSYRA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1282h | MTU | Timer Counter Synchronous Start Register | TCSYSTR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1284h | MTU | Timer Read/Write Enable Register A | TRWERA | 8 | 8 | 4 or 5 PCLKA |
| 000C 1290h | MTU0 | Noise Filter Control Register 0 | NFCR0 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1291h | MTU1 | Noise Filter Control Register 1 | NFCR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1292h | MTU2 | Noise Filter Control Register 2 | NFCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1293h | MTU3 | Noise Filter Control Register 3 | NFCR3 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1294h | MTU4 | Noise Filter Control Register 4 | NFCR4 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1299h | MTU0 | Noise Filter Control Register C | NFCRC | 8 | 8 | 4 or 5 PCLKA |
| 000C 1300h | MTU0 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1301h | MTU0 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1302h | MTU0 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1303h | MTU0 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 or 5 PCLKA |
| 000C 1304h | MTU0 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1306h | MTU0 | Timer Counter | TCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 1308h | MTU0 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 130Ah | MTU0 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 130Ch | MTU0 | Timer General Register C | TGRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 130Eh | MTU0 | Timer General Register D | TGRD | 16 | 16 | 4 or 5 PCLKA |
| 000C 1320h | MTU0 | Timer General Register E | TGRE | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1322h | MTU0 | Timer General Register F | TGRF | 16 | 16 | 4 or 5 PCLKA |
| 000C 1324h | MTU0 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1326h | MTU0 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 or 5 PCLKA |
| 000C 1328h | MTU0 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1380h | MTU1 | Timer Control Register | TCR | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1381h | MTU1 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1382h | MTU1 | Timer I/O Control Register | TIOR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1384h | MTU1 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 1385h | MTU1 | Timer Status Register | TSR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1386h | MTU1 | Timer Counter | TCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 1388h | MTU1 | Timer General Register A | TGRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 138Ah | MTU1 | Timer General Register B | TGRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1390h | MTU1 | Timer Input Capture Control Register | TICCR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1391h | MTU1 | Timer Mode Register 3 | TMDR3 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1394h | MTU1 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 13A0h | MTU1 | Timer Longword Counter | TCNTLW | 32 | 32 | 4 or 5 PCLKA |
| 000C 13A4h | MTU1 | Timer Longword General Register | TGRALW | 32 | 32 | 4 or 5 PCLKA |
| 000C 13A8h | MTU1 | Timer Longword General Register | TGRBLW | 32 | 32 | 4 or 5 PCLKA |
| 000C 1400h | MTU2 | Timer Control Register | TCR | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1401h | MTU2 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1402h | MTU2 | Timer I/O Control Register | TIOR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1404h | MTU2 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 or 5 PCLKA |

**Table 4.1 List of I/O Registers (Address Order) (16 / 16)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK |
| 007F C35Ch | FLASHCONST | Unique ID Register 3 | UIDR3 | 32 | 32 | 2 or 3 FCLK |
| 007F FFB2h | FLASH | Flash P/E Mode Entry Register | FENTRYR | 16 | 16 | 2 or 3 FCLK |

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 22.4 lists register allocation for 16-bit access in the User's Manual: Hardware.

## 5.2 DC Characteristics

**Table 5.3 DC Characteristics (1)**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | RIIC input pin (except for SMBus, 5 V tolerant) | $V_{IH}$ | VCC × 0.7 | — | 5.8 | V | |
| | Ports B1 and B2 (5 V tolerant) | | VCC × 0.8 | — | 5.8 | | |
| | Ports 00 to 02, 10, 11<br>Ports 22 to 24<br>Ports 30 to 33, 36, 37<br>Ports 70 to 76<br>Ports 91 to 94<br>Ports A2 to A5<br>Ports B0, B3 to B7<br>Ports D3 to D7<br>Port E2<br>Port RES# | | VCC × 0.8 | — | VCC + 0.3 | | |
| | Ports 40 to 47 | | AVCC0 × 0.8 | — | AVCC0 + 0.3 | | |
| | RIIC input pin (except for SMBus) | $V_{IL}$ | –0.3 | — | VCC × 0.3 | | |
| | Ports 40 to 47 | | –0.3 | — | AVCC0 × 0.2 | | |
| | Other than RIIC input pin or ports 40 to 47 | | –0.3 | — | VCC × 0.2 | | |
| | RIIC input pin (except for SMBus) | $\Delta V_T$ | VCC × 0.05 | — | — | | |
| | Ports 40 to 47 | | AVCC0 × 0.1 | — | — | | |
| | Other than RIIC input pin or ports 40 to 47 | | VCC × 0.1 | — | — | | |
| Input level voltage (except for Schmitt trigger input pins) | MD | $V_{IH}$ | VCC × 0.9 | — | VCC + 0.3 | V | |
| | EXTAL (external clock input) | | VCC × 0.8 | — | VCC + 0.3 | | |
| | RIIC input pin (SMBus) | | 2.1 | — | VCC + 0.3 | | |
| | MD | $V_{IL}$ | –0.3 | — | VCC × 0.1 | | |
| | EXTAL (external clock input) | | –0.3 | — | VCC × 0.2 | | |
| | RIIC input pin (SMBus) | | –0.3 | — | 0.8 | | |

**Table 5.4 DC Characteristics (2)**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input leakage current | RES#, MD, port E2 | $\lvert I_{in} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V, VCC |
| Three-state leakage current (off-state) | Port 4 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V, AVCC0 |
| | Ports except for 5-V tolerant ports and port 4 | | — | — | 0.2 | | $V_{in}$ = 0 V, VCC |
| | Ports for 5 V tolerant | | — | — | 1.0 | | $V_{in}$ = 0 V, 5.8 V |
| Input capacitance | All input pins | $C_{in}$ | — | 4 | 15 | pF | $V_{in}$ = 0 mV,<br>f = 1 MHz,<br>$T_a$ = 25°C |
| Input pull-up resistor | All ports (except for port E2) | $R_U$ | 10 | 20 | 50 | kΩ | $V_{in}$ = 0 V |

### 5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.8 to Figure 5.11 show the characteristics when high-drive output is selected by the drive capacity control register.

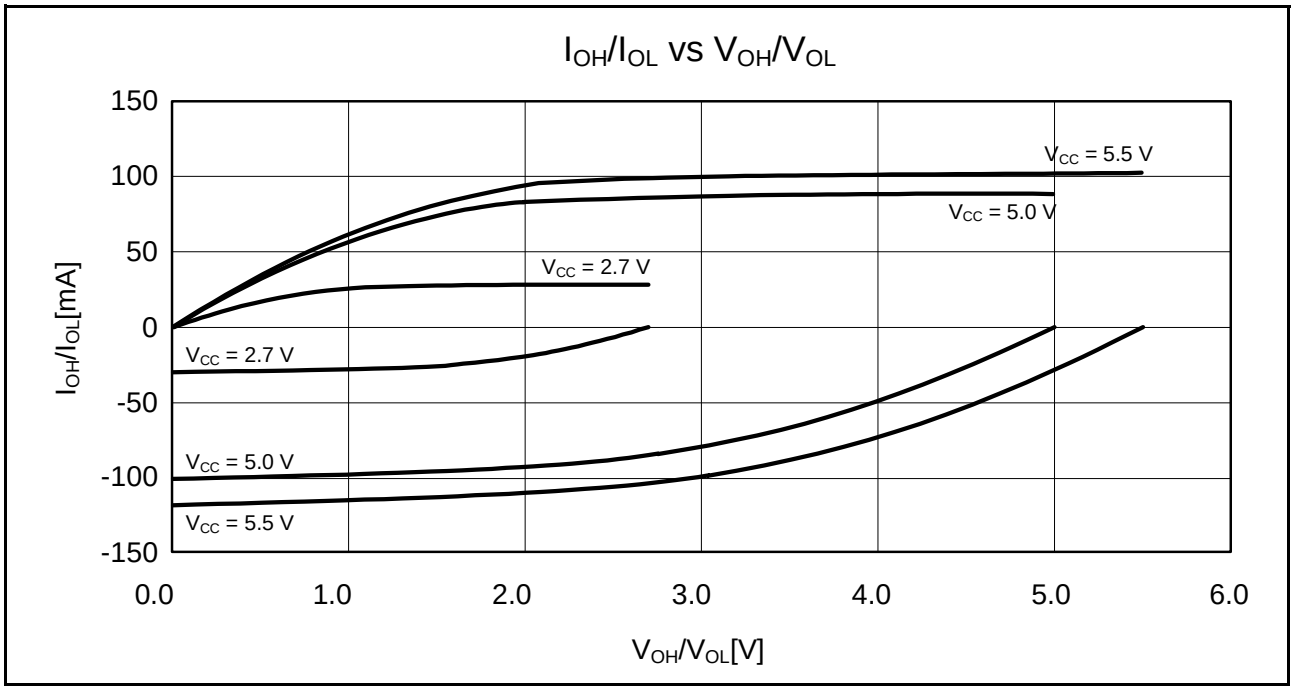



**Figure 5.8** $V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ Voltage Characteristics at $T_a$ = 25°C When Normal Output is Selected (Reference Data)

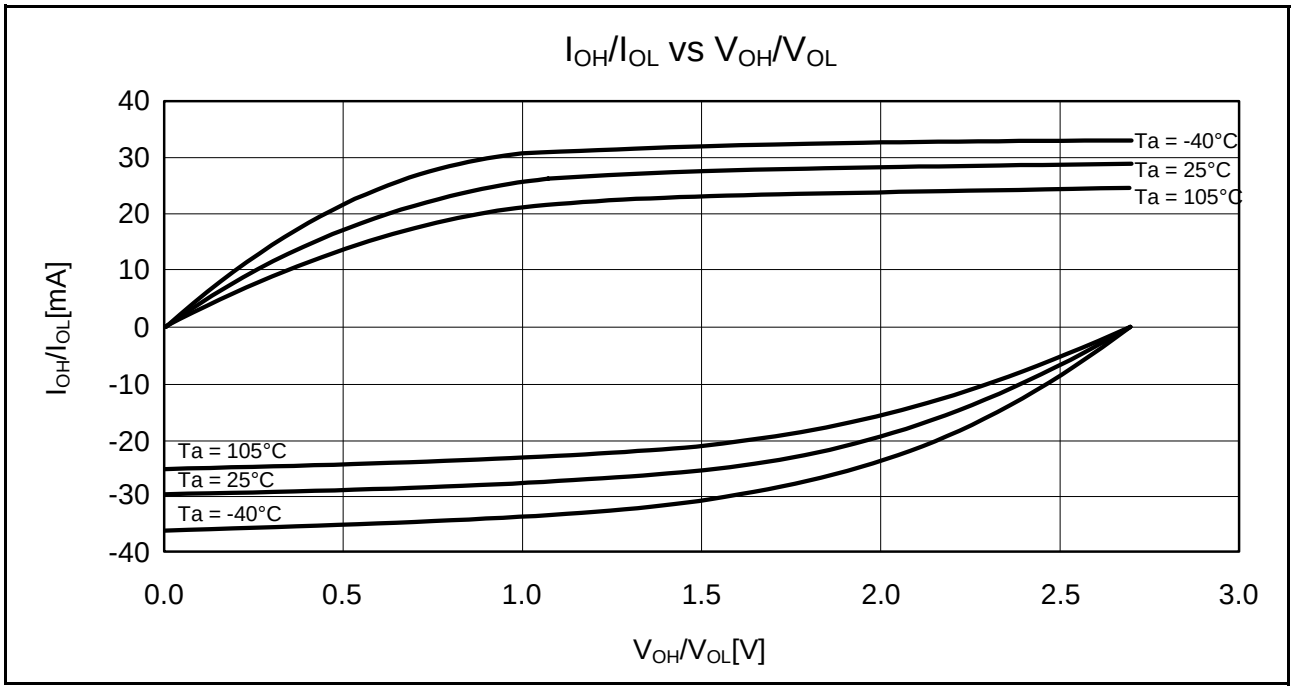



**Figure 5.9** $V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

## 5.3.3 Timing of Recovery from Low Power Consumption Modes

**Table 5.18 Timing of Recovery from Low Power Consumption Modes (1)**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Recovery time from software standby mode*1 | High-speed mode | Crystal connected to main clock oscillator | Main clock oscillator operating*2 | $t_{SBYMC}$ | — | 2 | 3 | ms | Figure 5.30 |
| | | External clock input to main clock oscillator | Main clock oscillator operating*3 | $t_{SBYEX}$ | — | 35 | 50 | µs | |
| | | | Main clock oscillator and PLL circuit operating*4 | $t_{SBYPE}$ | — | 70 | 95 | µs | |
| | | LOCO clock oscillator operating | | $t_{SBYLO}$ | — | 40 | 55 | µs | |

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of crystal is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of the external clock is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 4. When the frequency of PLL is 40 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

**Table 5.19 Timing of Recovery from Low Power Consumption Modes (2)**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Recovery time from software standby mode*1 | Middle-speed mode | Crystal connected to main clock oscillator | Main clock oscillator operating*2 | $t_{SBYMC}$ | — | 2 | 3 | ms | Figure 5.30 |
| | | External clock input to main clock oscillator | Main clock oscillator operating*3 | $t_{SBYEX}$ | — | 3 | 4 | µs | |
| | | | Main clock oscillator and PLL circuit operating*4 | $t_{SBYPE}$ | — | 65 | 85 | µs | |
| | | LOCO clock oscillator operating | | $t_{SBYLO}$ | — | 5 | 7 | µs | |

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of the external clock is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 4. When the frequency of PLL is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

## 5.3.4 Control Signal Timing

**Table 5.22 Control Signal Timing**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | NMI digital filter disabled (NMIFLTE.NFLTEN = 0) | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | NMI digital filter enabled (NMIFLTE.NFLTEN = 1) | $t_{NMICK} \times 3 \leq 200$ ns |
| | | $t_{NMICK} \times 3.5$*2 | — | — | | | $t_{NMICK} \times 3 > 200$ ns |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | IRQ digital filter disabled (IRQFLTE0.FLTENi = 0) | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | IRQ digital filter enabled (IRQFLTE0.FLTENi = 1) | $t_{IRQCK} \times 3 \leq 200$ ns |
| | | $t_{IRQCK} \times 3.5$*3 | — | — | | | $t_{IRQCK} \times 3 > 200$ ns |

Note: 200 ns minimum in software standby mode.
Note 1. $t_{Pcyc}$ indicates the cycle of PCLKB.
Note 2. $t_{NMICK}$ indicates the cycle of the NMI digital filter sampling clock.
Note 3. $t_{IRQCK}$ indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 5).

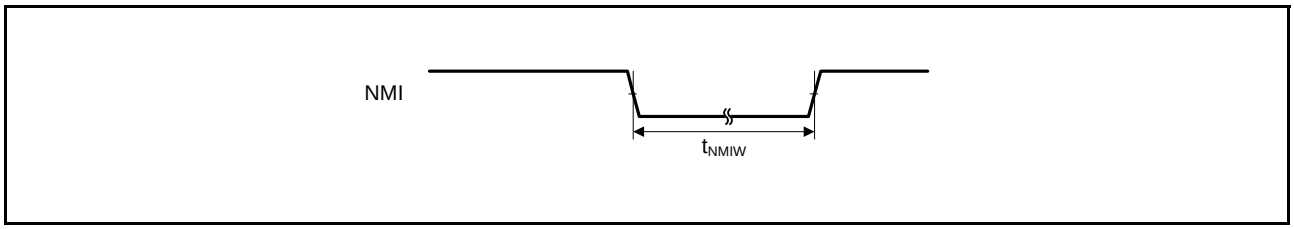



**Figure 5.32 NMI Interrupt Input Timing**

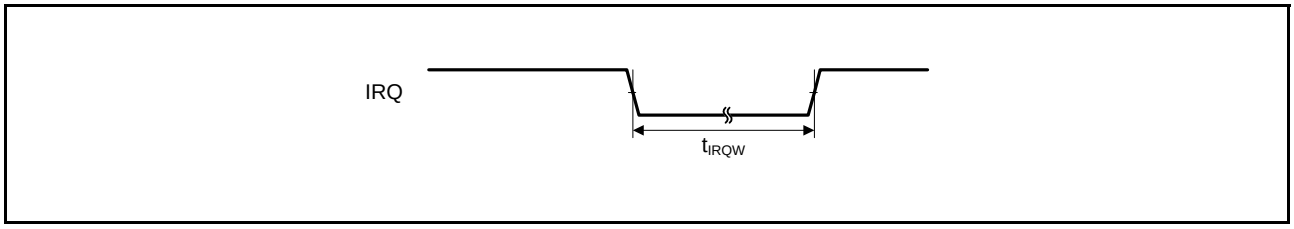



**Figure 5.33 IRQ Interrupt Input Timing**

**Table 5.24 Timing of On-Chip Peripheral Modules (2)**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, $T_a$ = –40 to +105°C, C = 30pF

| Item | | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| RSPI | RSPCK clock cycle | Master | | $t_{SPcyc}$ | 2 | 4096 | $t_{Pcyc}$*1 | Figure 5.42 |
| | | Slave | | | 8 | 4096 | | |
| | RSPCK clock high pulse width | Master | VCC = 4.0 V or above | $t_{SPCKWH}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$ | — | ns | |
| | | | VCC = 2.7 V or above | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$ | — | | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$ | — | | |
| | RSPCK clock low pulse width | Master | VCC = 4.0 V or above | $t_{SPCKWL}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$ | — | ns | |
| | | | VCC = 2.7 V or above | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$ | — | | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$ | — | | |
| | RSPCK clock rise/fall time | Output | VCC = 4.0 V or above | $t_{SPCKr}$, $t_{SPCKf}$ | — | 6 | ns | |
| | | | VCC = 2.7 V or above | | — | 10 | | |
| | | Input | | | — | 0.1 | μs/V | |
| | Data input setup time | Master | VCC = 4.0 V or above | $t_{SU}$ | 10 | — | ns | Figure 5.43 to Figure 5.46 |
| | | | VCC = 2.7 V or above | | 26 | — | | |
| | | Slave | | | $25 - t_{Pcyc}$ | — | | |
| | Data input hold time | Master | RSPCK set to a division ratio other than PCLKB divided by 2 | $t_H$ | $t_{Pcyc}$ | — | ns | |
| | | | RSPCK set to PCLKB divided by 2 | $t_{HF}$ | 0 | — | | |
| | | Slave | | $t_H$ | $20 + 2 \times t_{Pcyc}$ | — | | |
| | SSL setup time | Master | | $t_{LEAD}$ | $-30 + N^{*2} \times t_{SPcyc}$ | — | ns | |
| | | Slave | | | 2 | — | $t_{Pcyc}$ | |
| | SSL hold time | Master | | $t_{LAG}$ | $-30 + N^{*3} \times t_{SPcyc}$ | — | ns | |
| | | Slave | | | 2 | — | $t_{Pcyc}$ | |
| | Data output delay time | Master | VCC = 4.0 V or above | $t_{OD}$ | — | 10 | ns | |
| | | | VCC = 2.7 V or above | | — | 14 | | |
| | | Slave | | | — | $3 \times t_{Pcyc} + 65$ | | |
| | Data output hold time | Master | 2.7 V or above | $t_{OH}$ | 0 | — | ns | |
| | | Slave | | | 0 | — | | |
| | Successive transmission delay time | Master | | $t_{TD}$ | $t_{SPcyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{Pcyc}$ | ns | |
| | | Slave | | | $4 \times t_{Pcyc}$ | — | | |
| | MOSI and MISO rise/fall time | Output | | $t_{Dr}$, $t_{Df}$ | — | 10 | ns | |
| | | Input | | | — | 1 | μs | |
| | SSL rise/fall time | Output | | $t_{SSLr}$, $t_{SSLf}$ | — | 10 | ns | |
| | | Input | | | — | 1 | μs | |
| | Slave access time | | | $t_{SA}$ | — | 6 | $t_{Pcyc}$ | Figure 5.45, Figure 5.46 |
| | Slave output release time | | | $t_{REL}$ | — | 5 | $t_{Pcyc}$ | |

Note 1. $t_{Pcyc}$: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

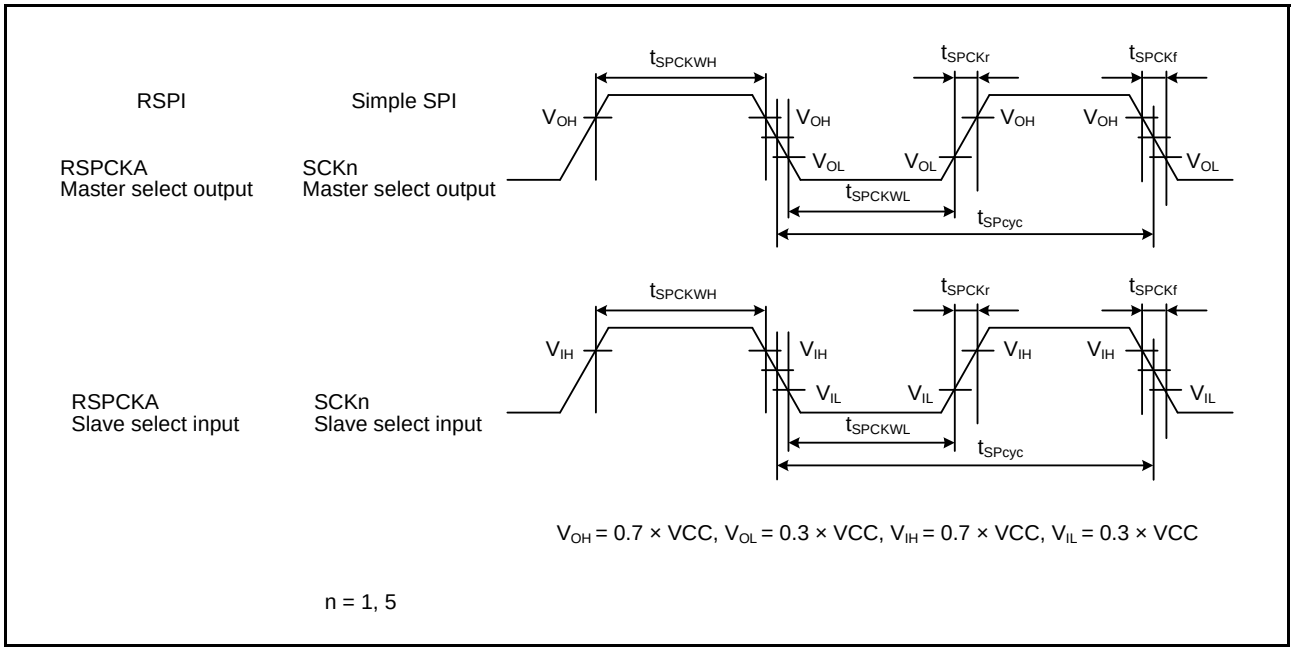



**Figure 5.42 RSPI Clock Timing and Simple SPI Clock Timing**

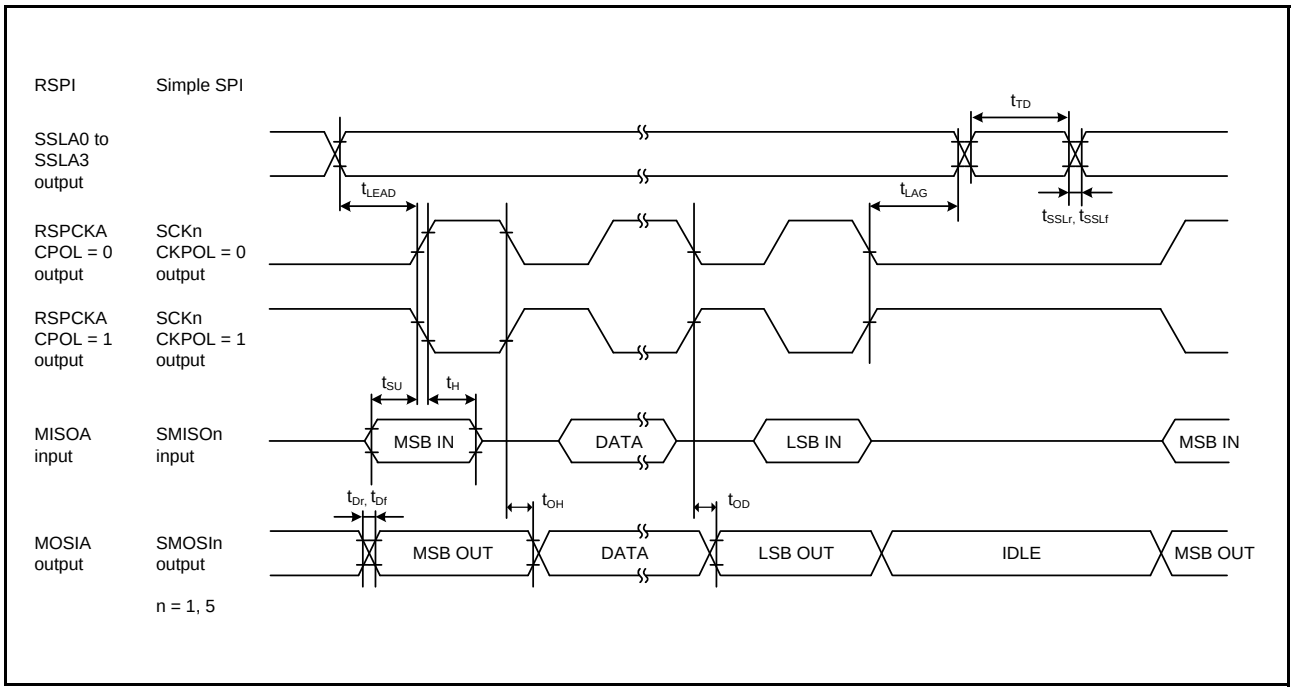



**Figure 5.43 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)**

**Table 5.35 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VREFH0 = VCC to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, Ta = –40 to +105°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Wait time after power-on reset cancellation | $t_{POR}$ | — | 28.4 | — | ms | Figure 5.51 |
| Wait time after voltage monitoring 0 reset cancellation | $t_{LVD0}$ | — | 568 | — | µs | Figure 5.52 |
| Wait time after voltage monitoring 1 reset cancellation | $t_{LVD1}$ | — | 100 | — | µs | Figure 5.53 |
| Wait time after voltage monitoring 2 reset cancellation | $t_{LVD2}$ | — | 100 | — | µs | Figure 5.54 |
| Response delay time | $t_{det}$ | — | — | 350 | µs | Figure 5.50 |
| Minimum VCC down time*1 | $t_{VOFF}$ | 350 | — | — | µs | Figure 5.50, VCC = 1.0 V or above |
| Power-on reset enable time | $t_{W(POR)}$ | 1 | — | — | ms | Figure 5.51, VCC = below 1.0 V |
| LVD operation stabilization time (after LVD is enabled) | $Td_{(E-A)}$ | — | — | 300 | µs | Figure 5.53, Figure 5.54 |
| Hysteresis width (LVD1 and LVD2) | $V_{LVH}$ | — | 70 | — | mV | Vdet1_0 to 4 selected |
| | | — | 60 | — | | Vdet1_5 to 8, LVD2 selected |

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det1}$, and $V_{det2}$ for the POR/LVD.

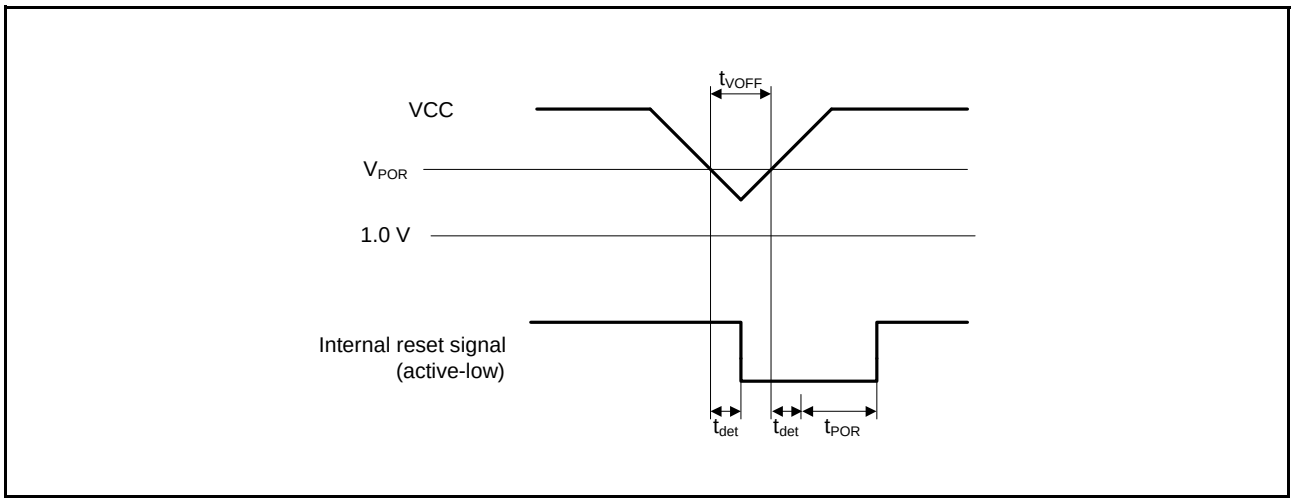
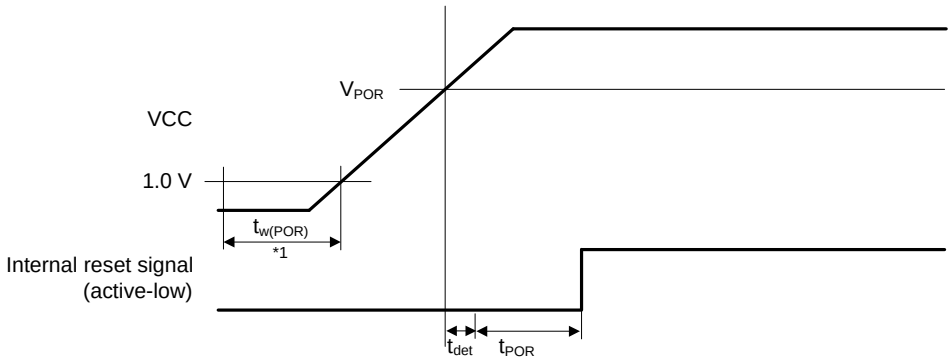



**Figure 5.50 Voltage Detection Reset Timing**




Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

**Figure 5.51 Power-On Reset Timing**

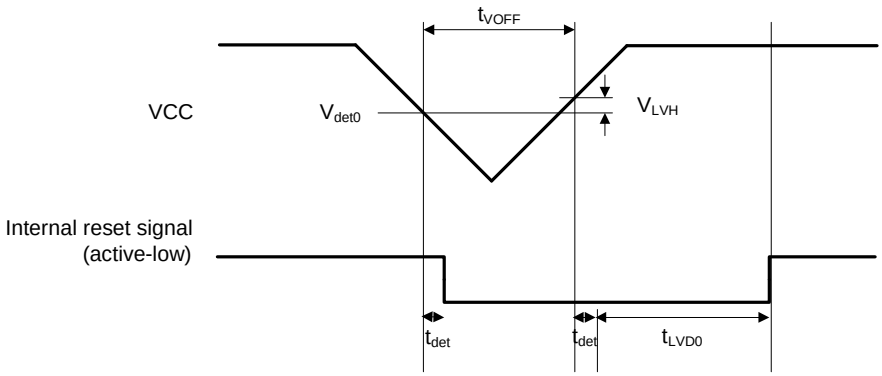



**Figure 5.52 Voltage Detection Circuit Timing (Vdet0)**

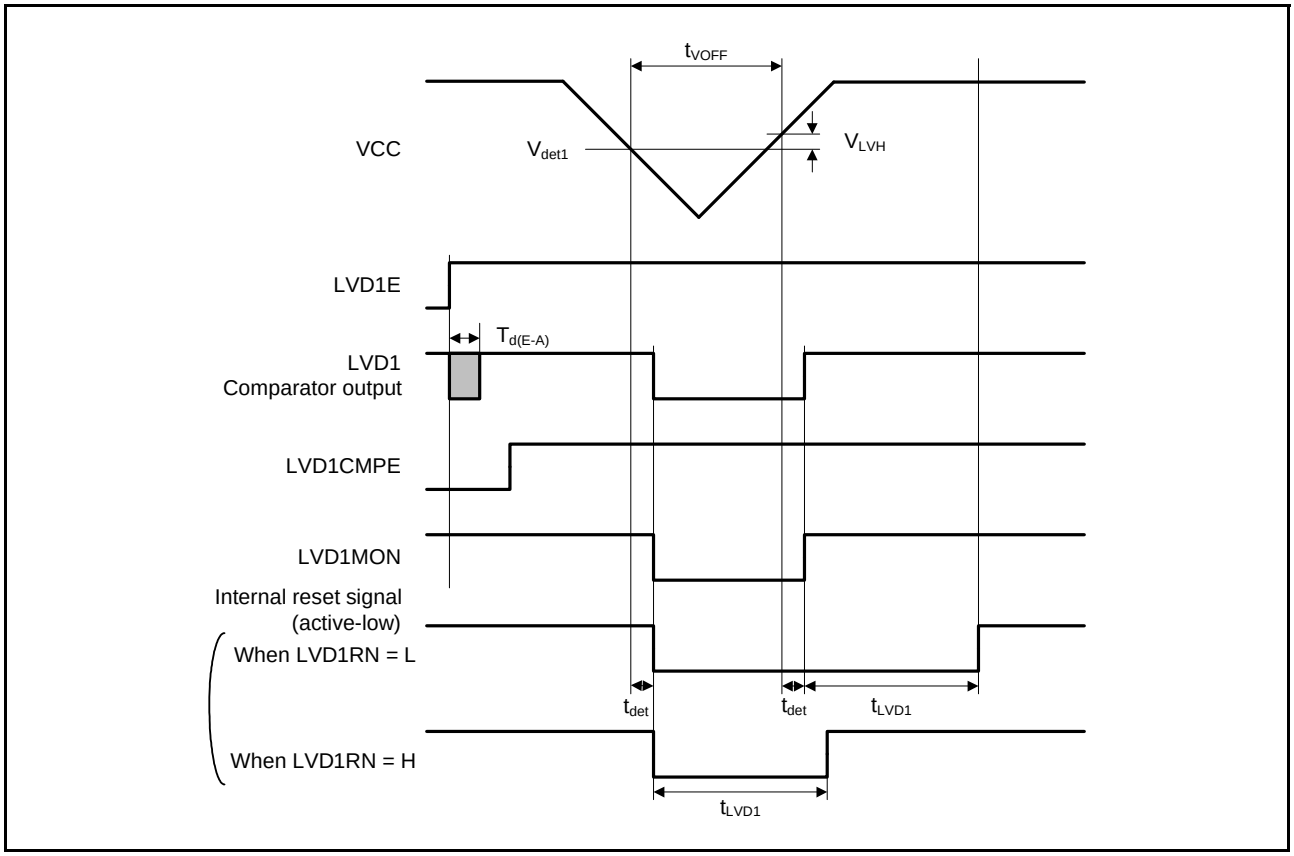



**Figure 5.53 Voltage Detection Circuit Timing ($V_{det1}$)**

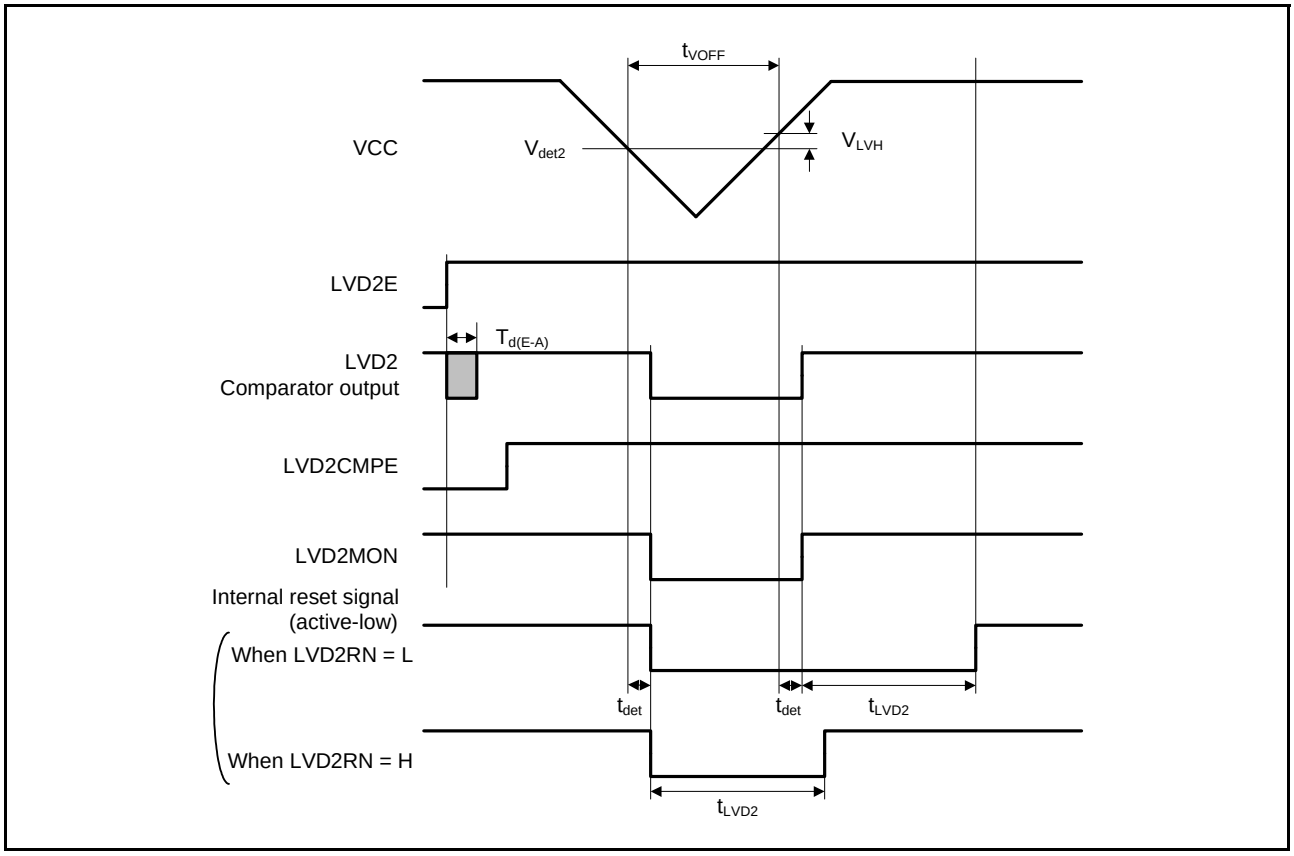
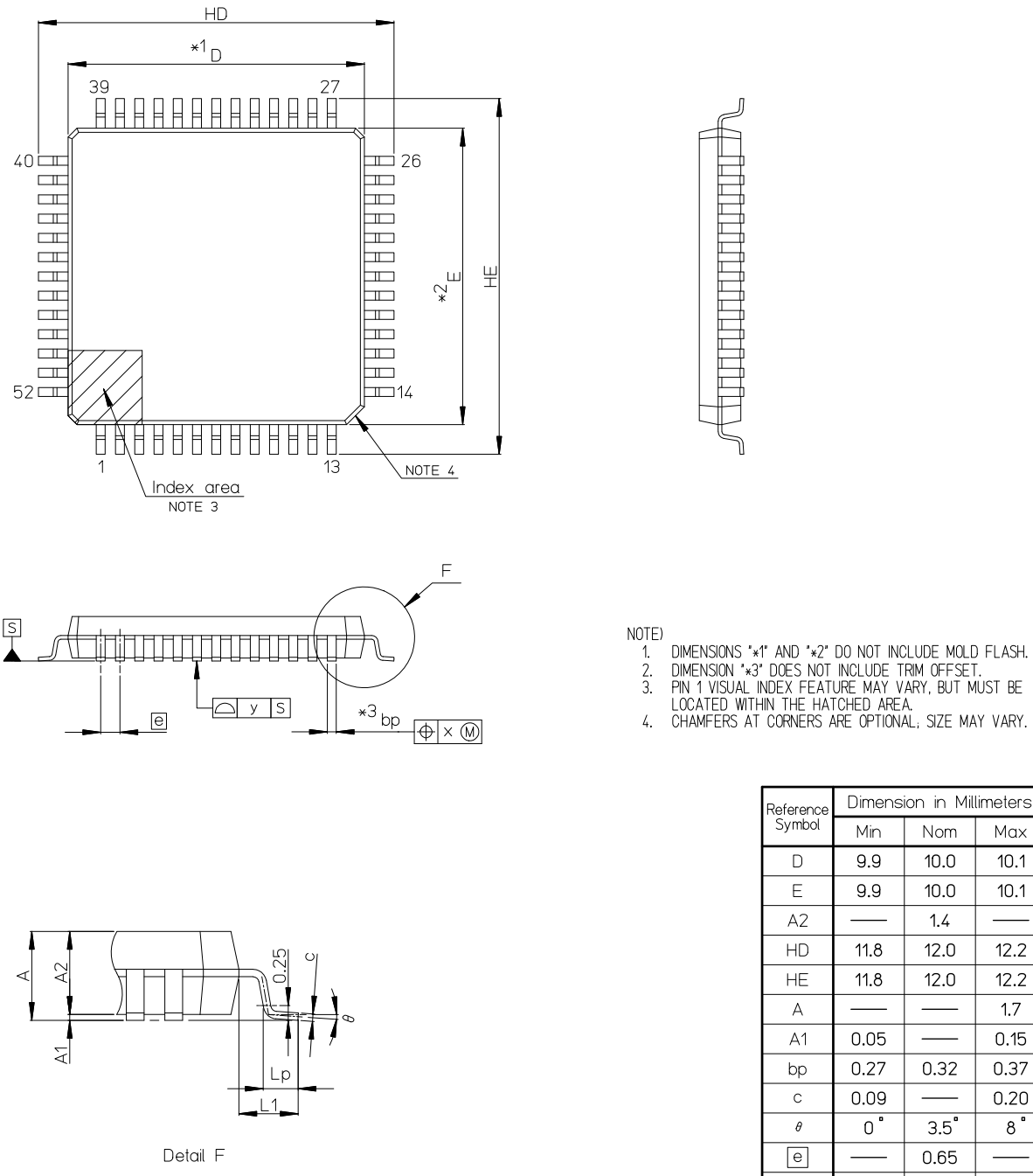



**Figure 5.54 Voltage Detection Circuit Timing ($V_{det2}$)**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP52-10x10-0.65 | PLQP0052JA-B | —— | 0.3g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| A2 | —— | 1.4 | —— |
| HD | 11.8 | 12.0 | 12.2 |
| HE | 11.8 | 12.0 | 12.2 |
| A | —— | —— | 1.7 |
| A1 | 0.05 | —— | 0.15 |
| bp | 0.27 | 0.32 | 0.37 |
| c | 0.09 | —— | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | —— | 0.65 | —— |
| x | —— | —— | 0.13 |
| y | —— | —— | 0.10 |
| Lp | 0.45 | 0.6 | 0.75 |
| L1 | —— | 1.0 | —— |

Figure B 52-Pin LQFP (PLQP0052JA-B)