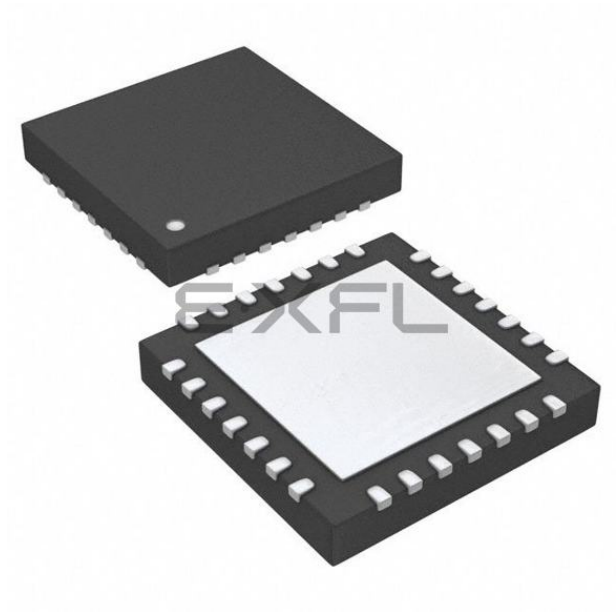

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f24q10-i-ml

4.2.2 Internal Clock Sources

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in Configuration Words to select the INTOSC clock as the default system clock upon a device Reset.
- Write the NOSC<2:0> bits to switch the system clock source to the internal oscillator during run-time.

In INTOSC mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the $\overline{\text{CLKOUTEN}}$ bit in Configuration Words.

The internal oscillator block has two independent oscillators that can produce two internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory-calibrated and operates from 1 to 64 MHz. The frequency of HFINTOSC can be selected through the OSCFRQ Frequency Selection register, and fine-tuning can be done via the OSCTUNE register.
2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is factory-calibrated and operates at 31 kHz.

Related Links

4.3 Clock Switching

4.6.5 OSCFRQ

4.6.6 OSCTUNE

4.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a precision digitally-controlled internal clock source that produces a stable clock up to 64 MHz. The HFINTOSC can be enabled through one of the following methods:

- Programming the RSTOSC<2:0> bits in Configuration Word 1 to '110' (F_{OSC} = 1 MHz) or '000' (F_{OSC} = 64 MHz) to set the oscillator upon device Power-up or Reset.
- Write to the NOSC<2:0> bits during run-time.

The HFINTOSC frequency can be selected by setting the HFFRQ<3:0> bits.

The NDIV<3:0> bits allow for division of the HFINTOSC output from a range between 1:1 and 1:512.

Related Links

4.3 Clock Switching

4.2.2.2 MFINTOSC

The module provides two (500 kHz and 31.25 kHz) constant clock outputs. These clocks are digital divisors of the HFINTOSC clock. Dynamic divider logic is used to provide constant MFINTOSC clock rates for all settings of HFINTOSC.

The MFINTOSC cannot be used to drive the system but it is used to clock certain modules such as the Timers and WWDT.

4.2.2.3 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is a factory-calibrated 31 kHz internal clock source.

The LFINTOSC is the frequency for the Power-up Timer (PWRT), Windowed Watchdog Timer (WWDT) and Fail-Safe Clock Monitor (FSCM).

4.6.4 OSCSTAT

Name: OSCSTAT
Address: 0xED6

Oscillator Status Register 1

Bit	7	6	5	4	3	2	1	0
	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR		PLLR
Access	RO	RO	RO	RO	RO	RO		RO
Reset	q	q	q	q	q	q		q

Bit 7 – EXTOR EXTOSC (external) Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 6 – HFOR HFINTOSC Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 5 – MFOR MFINTOSC Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 4 – LFOR LFINTOSC Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 3 – SOR Secondary (Timer1) Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 2 – ADOR ADC Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 0 – PLLR PLL Ready bit

5.1 Clock Source

The clock source of the reference clock peripheral is selected with the CLK bits. The available clock sources are listed in the following table:

Table 5-1. CLKR Clock Sources

CLK	Clock Source
111-101	Unimplemented
100	SOSC
011	MFINTOSC (500 kHz)
010	LFINTOSC (31 kHz)
001	HFINTOSC
000	F_{OSC}

5.1.1 Clock Synchronization

The CLKR output signal is ensured to be glitch-free when the 5.6.1.1 EN bit is set to start the module and enable the CLKR output.

When the reference clock output is disabled, the output signal will be disabled immediately.

Clock dividers and clock duty cycles can be changed while the module is enabled but doing so may cause glitches to occur on the output. To avoid possible glitches, clock dividers and clock duty cycles should be changed only when the 5.6.1.1 EN bit is clear.

5.2 Programmable Clock Divider

The module takes the clock input and divides it based on the value of the 5.6.1.3 DIV bits.

The following configurations are available:

- Base Fosc value
- F_{OSC} divided by 2
- F_{OSC} divided by 4
- F_{OSC} divided by 8
- F_{OSC} divided by 16
- F_{OSC} divided by 32
- F_{OSC} divided by 64
- F_{OSC} divided by 128

The clock divider values can be changed while the module is enabled. However, in order to prevent glitches on the output, the 5.6.1.3 DIV bits should only be changed when the module is disabled (5.6.1.1 EN = 0).

5.3 Selectable Duty Cycle

The 5.6.1.2 DC bits are used to modify the duty cycle of the output clock. A duty cycle of 0%, 25%, 50%, or 75% can be selected for all clock rates when the 5.6.1.3 DIV value is not 0b000. When DIV=0b000

Table 8-2. $\overline{MCLR}$ Configuration

MCLRE	LVP	$\overline{MCLR}$
x	1	Enabled
1	0	Enabled
0	0	Disabled

8.4.1 $\overline{MCLR}$ Enabled

When $\overline{MCLR}$ is enabled and the pin is held low, the device is held in Reset. The $\overline{MCLR}$ pin is connected to V_{DD} through an internal weak pull-up.

The device has a noise filter in the $\overline{MCLR}$ Reset path. The filter will detect and ignore small pulses.

Important: An internal Reset event (RESET instruction, BOR, WWDT, POR, STKOVF, STKUNF) does not drive the $\overline{MCLR}$ pin low.

8.4.2 $\overline{MCLR}$ Disabled

When $\overline{MCLR}$ is disabled, the $\overline{MCLR}$ becomes input-only and pin functions such as internal weak pull-ups are under software control.

Related Links

15.1 I/O Priorities

8.5 Windowed Watchdog Timer (WWDT) Reset

The Windowed Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period or window set. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register and the $\overline{RWDT}$ bit are changed to indicate a WDT Reset. The $\overline{WDTWV}$ bit indicates if the WDT Reset has occurred due to a timeout or a window violation.

Related Links

10.8.5 STATUS

9. (WWDT) Windowed Watchdog Timer

8.6 RESET Instruction

A RESET instruction will cause a device Reset. The $\overline{RI}$ bit will be set to '0'. See Table 8-3 for default conditions after a RESET instruction has occurred.

8.7 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words.

Related Links

3.7.2 CONFIG2

Figure 10-2. Memory Map and Code Protection Control

Rev. 40-000100B
4/20/2017

Region	Address	Device	
		PIC18F24Q10	PIC18F25Q10
PFM	00 0000h to 00 07FFh	Boot Block 1 KW CP, WRTB, EBTRB	Boot Block 1 KW CP, WRTB, EBTRB
	00 0800h to 00 1FFFh	Block 0 3 KW CP, WRT0, EBTR0	Block 0 3 KW CP, WRT0, EBTR0
	00 2000h to 00 3FFFh	Block 1 4 KW CP, WRT1, EBTR1	Block 1 4 KW CP, WRT1, EBTR1
	00 4000h to 00 5FFFh	Not Present	Block 2 4 KW CP, WRT2, EBTR2
	00 6000h to 00 7FFFh		Block 3 4 KW CP, WRT3, EBTR3
	00 8000h to 00 BFFFh		Not Present
	00 C000h to 00 FFFFh		
	01 0000h to 01 3FFFh		
	01 4000h to 01 7FFFh		
	01 8000h to 01 BFFFh		
	01 C000h to 01 FFFFh		
CONFIG	30 0000h to 30 000Bh	6 Words WRTC	
Data EEPROM	31 0000h to 31 00FFh	256 Words CPD, WRTD	
	31 0100h to 31 01FFh	Unimplemented	

10.1.1 Program Counter

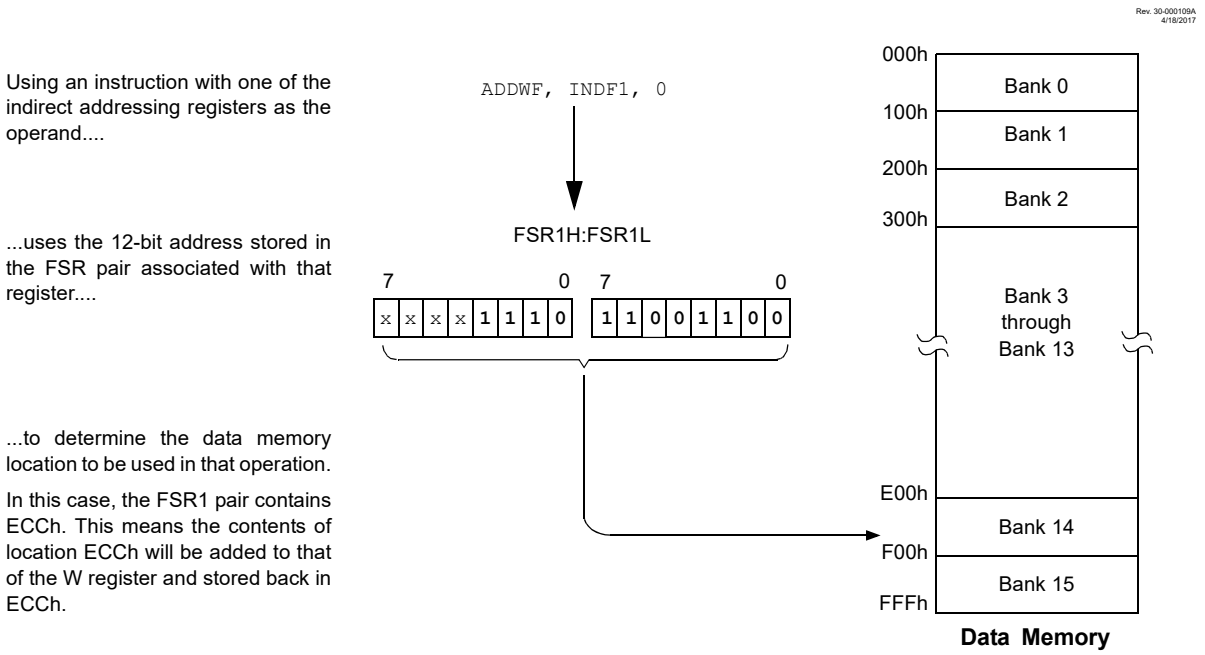
The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21 bits wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly

actually accesses the location to which the associated FSR register pair points, and also performs a specific action on the FSR value. They are:

- POSTDEC: accesses the location to which the FSR points, then automatically decrements the FSR by 1 afterwards
- POSTINC: accesses the location to which the FSR points, then automatically increments the FSR by 1 afterwards
- PREINC: automatically increments the FSR by one, then uses the location to which the FSR points in the operation
- PLUSW: adds the signed value of the W register (range of -127 to 128) to that of the FSR and uses the location to which the result points in the operation.

In this context, accessing an INDF register uses the value in the associated FSR register without changing it. Similarly, accessing a PLUSW register gives the FSR value an offset by that in the W register; however, neither W nor the FSR is actually changed in the operation. Accessing the other virtual registers changes the value of the FSR register.

Figure 10-10. Indirect Addressing



Operations on the FSRs with POSTDEC, POSTINC and PREINC affect the entire register pair; that is, rollovers of the FSRnL register from FFh to 00h carry over to the FSRnH register. On the other hand, results of these operations do not change the value of any flags in the STATUS register (e.g., Z, N, OV, etc.).

The PLUSW register can be used to implement a form of indexed addressing in the data memory space. By manipulating the value in the W register, users can reach addresses that are fixed offsets from pointer addresses. In some applications, this can be used to implement some powerful program control structure, such as software stacks, inside of data memory.

10.4.3.3 Operations by FSRs on FSRs

Indirect addressing operations that target other FSRs or virtual registers represent special cases. For example, using an FSR to point to one of the virtual registers will not result in successful operations. As a

10.8.13 BSR

Name: BSR
Address: 0xFE0

Bank Select Register
The BSR indicates the data memory bank which is bits 11:8 of the GPR address.

Bit	7	6	5	4	3	2	1	0
					BSR[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – BSR[3:0]
Four Most Significant bits of the data memory address

14.13.17 PIE7

Name: PIE7
Address: 0xEC4

Peripheral Interrupt Enable Register 7

Bit	7	6	5	4	3	2	1	0
	SCANIE	CRCIE	NVMIE					CWG1IE
Access	R/W	R/W	R/W					R/W
Reset	0	0	0					0

Bit 7 – SCANIE SCAN Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 6 – CRCIE CRC Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 5 – NVMIE NVM Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 0 – CWG1IE CWG Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

14.13.19 IPR1

Name: IPR1
Address: 0xEB6

Peripheral Interrupt Priority Register 1

Bit	7	6	5	4	3	2	1	0
	OSCFIP	CSWIP					ADTIP	ADIP
Access	R/W	R/W					R/W	R/W
Reset	1	1					1	1

Bit 7 – OSCFIP Oscillator Fail Interrupt Priority bit

Value	Description
1	High priority
0	Low priority

Bit 6 – CSWIP Clock-Switch Interrupt Priority bit

Value	Description
1	High priority
0	Low priority

Bit 1 – ADTIP ADC Threshold Interrupt Priority bit

Value	Description
1	High priority
0	Low priority

Bit 0 – ADIP ADC Interrupt Priority bit

Value	Description
1	High priority
0	Low priority

16.10.8 IOCEN

Name: IOCEN
Address: 0xF23

Interrupt-on-Change Negative Edge Register Example

Bit	7	6	5	4	3	2	1	0
					IOCEN3			
Access					R/W			
Reset					0			

Bit 3 – IOCEN3 Interrupt-on-Change Negative Edge Enable bits(1)

Value	Description
1	Interrupt-on-Change enabled on the IOCA pin for a negative-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin

Note:

1. If MCLRE = 1 or LVP = 1, RE3 port functionality is disabled and IOC on RE3 is not available.

19.14.2 TxGCON

Name: TxGCON
Address: 0xFCF,0xFC9,0xFC3

Timer Gate Control Register

Bit	7	6	5	4	3	2	1	0
	GE	GPOL	GTM	GSPM	GGO/DONE	GVAL		
Access	R/W	R/W	R/W	R/W	R/W	RO		
Reset	0	0	0	0	0	x		

Bit 7 – GE Timer Gate Enable bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Condition	Description
1	19.14.1.4 ON = 1	Timer counting is controlled by the Timer gate function
0	19.14.1.4 ON = 1	Timer is always counting
X	19.14.1.4 ON = 0	This bit is ignored

Bit 6 – GPOL Timer Gate Polarity bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	Timer gate is active-high (Timer counts when gate is high)
0	Timer gate is active-low (Timer counts when gate is low)

Bit 5 – GTM Timer Gate Toggle Mode bit
Timer Gate Flip-Flop Toggles on every rising edge

Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	Timer Gate Toggle mode is enabled
0	Timer Gate Toggle mode is disabled and Toggle flip-flop is cleared

Bit 4 – GSPM Timer Gate Single Pulse Mode bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	Timer Gate Single Pulse mode is enabled and is controlling Timer gate)
0	Timer Gate Single Pulse mode is disabled

Bit 3 – GGO/$\overline{\text{DONE}}$ Timer Gate Single Pulse Acquisition Status bit
This bit is automatically cleared when TxGSPM is cleared.

Reset States: POR/BOR = 0
All Other Resets = u

mechanism to control the flow of data. When this detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

26.3.1 Register Definitions: I²C Mode

The MSSPx module has seven registers for I²C operation.

These are:

- MSSP Status register (SSPxSTAT)
- MSSP Control register 1 (SSPxCON1)
- MSSP Control register 2 (SSPxCON2)
- MSSP Control register 3 (SSPxCON3)
- Serial Receive/Transmit Buffer register (SSPxBUF)
- MSSP Address register (SSPxADD)
- I²C Slave Address Mask register (SSPxMSK)
- MSSP Shift register (SSPSR) – not directly accessible

SSPxCON1, SSPxCON2, SSPxCON3 and SSPxSTAT are the Control and STATUS registers in I²C mode operation. The SSPxCON1, SSPxCON2, and SSPxCON3 registers are readable and writable. The lower six bits of the SSPxSTAT are read-only. The upper two bits of the SSPxSTAT are read/write. SSPSR is the Shift register used for shifting data in or out. SSPxBUF is the buffer register to which data bytes are written to or read from. SSPxADD contains the slave device address when the MSSP is configured in I²C Slave mode. When the MSSP is configured in Master mode, the lower seven bits of SSPxADD act as the Baud Rate Generator reload value.

SSPxMSK holds the slave address mask value when the module is configured for 7-Bit Address Masking mode. While it is a separate register, it shares the same SFR address as SSPxADD; it is only accessible when the SSPM<3:0> bits are specifically set to permit access. In receive operations, SSPSR and SSPxBUF together, create a double-buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPxBUF and the SSPxIF interrupt is set. During transmission, the SSPxBUF is not double-buffered. A write to SSPxBUF will write to both SSPxBUF and SSPSR.

26.4 I²C Mode Operation

All MSSP I²C communication is byte oriented and shifted out MSb first. Six SFR registers and two interrupt flags interface the module with the PIC® microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

26.4.1 Clock Stretching

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

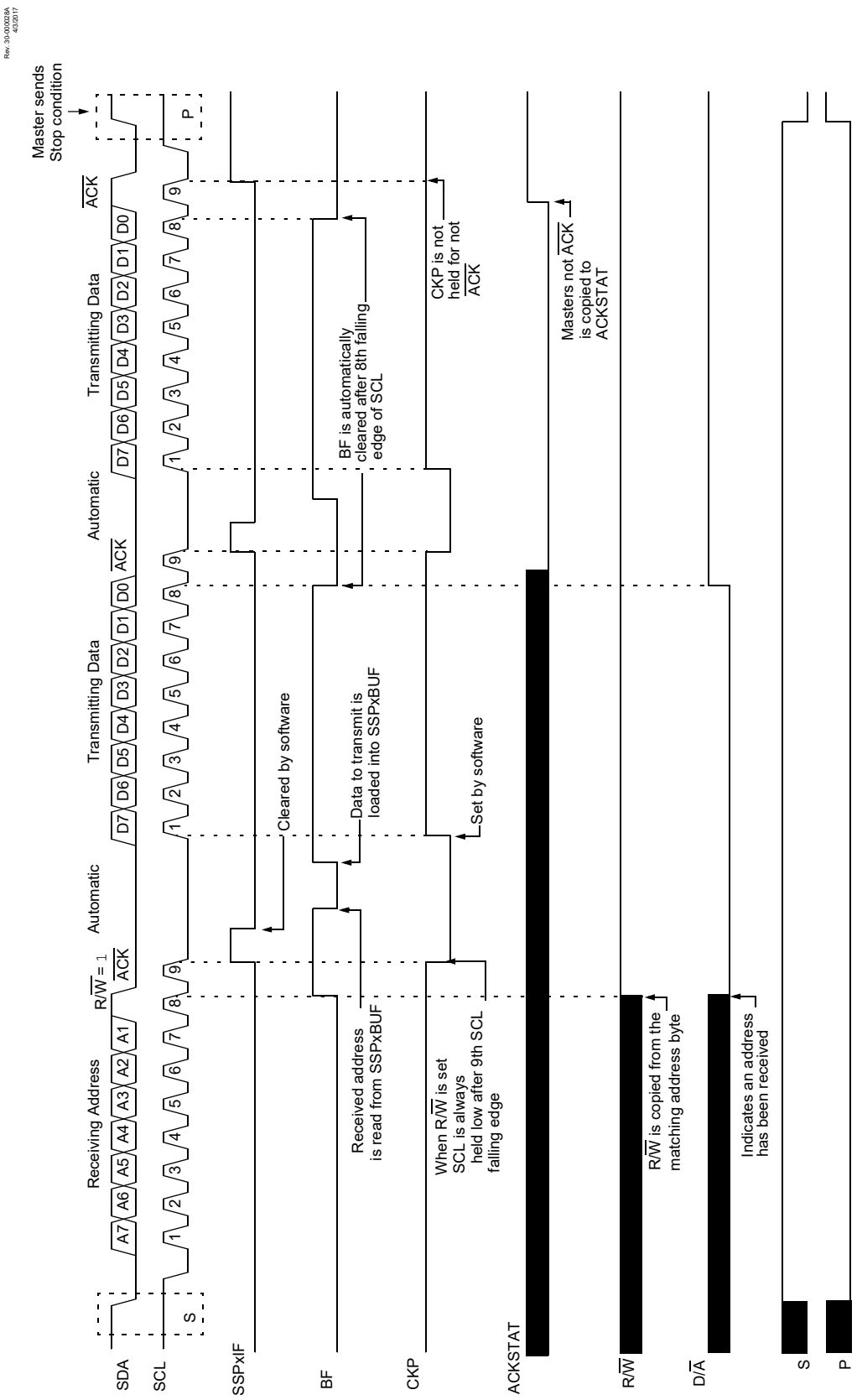


Figure 26-18. I²C Slave, 7-bit Address, Transmission (AHEN = 0)

26.5.4 Slave Mode 10-bit Address Reception

This section describes a standard sequence of events for the MSSP module configured as an I^2C slave in 10-bit Addressing mode.

Figure 26-20 is used as a visual reference for this description.

This is a step by step process of what must be done by slave software to accomplish I^2C communication.

1. Bus starts Idle.
2. Master sends Start condition; 26.9.1.5 S bit is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Master sends matching high address with 26.9.1.6 R/W bit clear; 26.9.1.7 UA bit is set.
4. Slave sends $\overline{\text{ACK}}$ and SSPxIF is set.
5. Software clears the SSPxIF bit.
6. Software reads received address from SSPxBUF clearing the BF flag.
7. Slave loads low address into SSPxADD, releasing SCL.
8. Master sends matching low address byte to the slave; UA bit is set.

Important: Updates to the SSPxADD register are not allowed until after the $\overline{\text{ACK}}$ sequence.

9. Slave sends $\overline{\text{ACK}}$ and SSPxIF is set.

Important: If the low address does not match, SSPxIF and UA are still set so that the slave software can set SSPxADD back to the high address. BF is not set because there is no match. 26.9.2.4 CKP is unaffected.

10. Slave clears SSPxIF.
11. Slave reads the received matching address from SSPxBUF clearing BF.
12. Slave loads high address into SSPxADD.
13. Master clocks a data byte to the slave and clocks out the slaves $\overline{\text{ACK}}$ on the ninth SCL pulse; SSPxIF is set.
14. If 26.9.3.8 SEN bit is set, 26.9.2.4 CKP is cleared by hardware and the clock is stretched.
15. Slave clears SSPxIF.
16. Slave reads the received byte from SSPxBUF clearing BF.
17. If 26.9.3.8 SEN is set the slave sets 26.9.2.4 CKP to release the SCL.
18. Steps 13-17 repeat for each received byte.
19. Master sends Stop to end the transmission.

26.5.5 10-bit Addressing with Address or Data Hold

Reception using 10-bit addressing with 26.9.4.7 AHEN or 26.9.4.8 DHEN set is the same as with 7-bit modes. The only difference is the need to update the SSPxADD register using the 26.9.1.7 UA bit. All

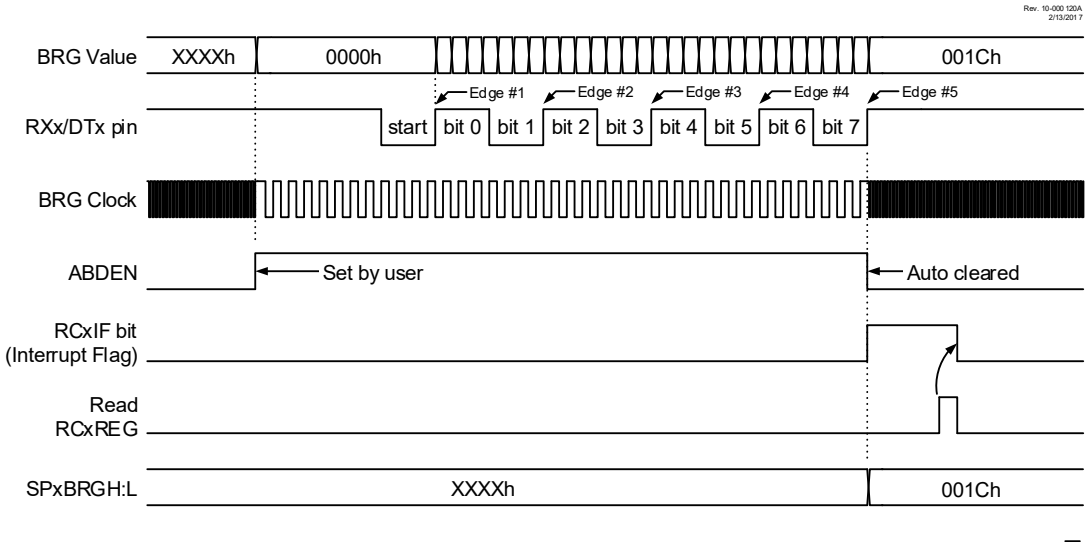
1. If the WUE bit is set with the ABDEN bit, auto-baud detection will occur on the byte following the Break character (see 27.2.3 Auto-Wake-up on Break).
2. It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible.
3. During the auto-baud process, the auto-baud counter starts counting at one. Upon completion of the auto-baud sequence, to achieve maximum accuracy, subtract 1 from the SPxBRGH:SPxBRGL register pair.

Table 27-3. BRG Counter Clock Rates

BRG16	BRGH	BRG Base Clock	BRG ABD Clock
1	1	$F_{OSC}/4$	$F_{OSC}/32$
1	0	$F_{OSC}/16$	$F_{OSC}/128$
0	1	$F_{OSC}/16$	$F_{OSC}/128$
0	0	$F_{OSC}/64$	$F_{OSC}/512$

Note: During the ABD sequence, SPxBRGL and SPxBRGH registers are both used as a 16-bit counter, independent of the BRG16 setting.

Figure 27-6. Automatic Baud Rate Calibration



27.2.2 Auto-Baud Overflow

During the course of automatic baud detection, the ABDOVF bit of the BAUDxCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RXx pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPxBRGH:SPxBRGL register pair. After the ABDOVF bit has been set, the counter continues to count until the fifth rising edge is detected on the RXx pin. Upon detecting the fifth RX edge, the hardware will set the RCxIF interrupt flag and clear the ABDEN bit of the BAUDxCON register. The RCxIF flag can be subsequently cleared by reading the RCxREG register. The ABDOVF flag of the BAUDxCON register can be cleared by software directly.

31.5.9 Double Sample Conversion

Double sampling is enabled by setting the 31.7.2.4 ADDSEN bit. When this bit is set, two conversions are required before the module will calculate threshold error. Each conversion must still be triggered separately when ADCONT = 0. The first conversion will set the 31.7.5.4 ADMATH bit and update ADACC, but will not calculate ADERR or trigger ADTIF. When the second conversion completes, the first value is transferred to ADPREV (depending on the setting of ADPSIS) and the value of the second conversion is placed into ADRES. Only upon the completion of the second conversion is ADERR calculated and ADTIF triggered (depending on the value of ADCALC).

COMF	Complement f			
Status Affected:	N, Z			
Encoding:	0001	11da	ffff	ffff
Description:	The contents of register ‘f’ are complemented. If ‘d’ is ‘0’, the result is stored in W. If ‘d’ is ‘1’, the result is stored back in register ‘f’ (default). If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank. If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See 36.2.3 Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode for details.			
Words:	1			
Cycles:	1			

Q Cycle Activity:			
Q1	Q2	Q3	Q4
Decode	Read register ‘f’	Process Data	Write to destination

Example:	COMF	REG,	0, 0
Before Instruction REG = 13h After Instruction REG = 13h W = ECh			

CPFSEQ	Compare f with W, skip if f = W			
Syntax:	CPFSEQ f {,a}			
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]			
Operation:	(f) – (W), skip if (f) = (W) (unsigned comparison)			
Status Affected:	None			
Encoding:	0110	001a	ffff	ffff

INCF	Increment f			
	If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See 36.2.3 Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode for details.			
Words:	1			
Cycles:	1			

Q Cycle Activity:			
Q1	Q2	Q3	Q4
Decode	Read register ‘f’	Process Data	Write to destination

Example:	INCF	CNT,	1, 0
Before Instruction CNT = FFh Z = 0 C = ? DC = ? After Instruction CNT = 00h Z = 1 C = 1 DC = 1			

INCFSZ	Increment f, skip if 0			
Syntax:	INCFSZ f {,d {,a}}			
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]			
Operation:	(f) + 1 → dest, skip if result = 0			
Status Affected:	None			
Encoding:	0011	11da	ffff	ffff

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions
			—	2.75	—	V	HLVDSEL=b'0101'
			—	2.90	—	V	HLVDSEL=b'0110'
			—	3.15	—	V	HLVDSEL=b'0111'
			—	3.35	—	V	HLVDSEL=b'1000'
			—	3.60	—	V	HLVDSEL=b'1001'
			—	3.75	—	V	HLVDSEL=b'1010'
			—	4.00	—	V	HLVDSEL=b'1011'
			—	4.20	—	V	HLVDSEL=b'1100'
			—	4.35	—	V	HLVDSEL=b'1101'
			—	4.65	—	V	HLVDSEL=b'1110'

38.4.7 Analog-To-Digital Converter (ADC) Accuracy Specifications(1,2)

Table 38-13.

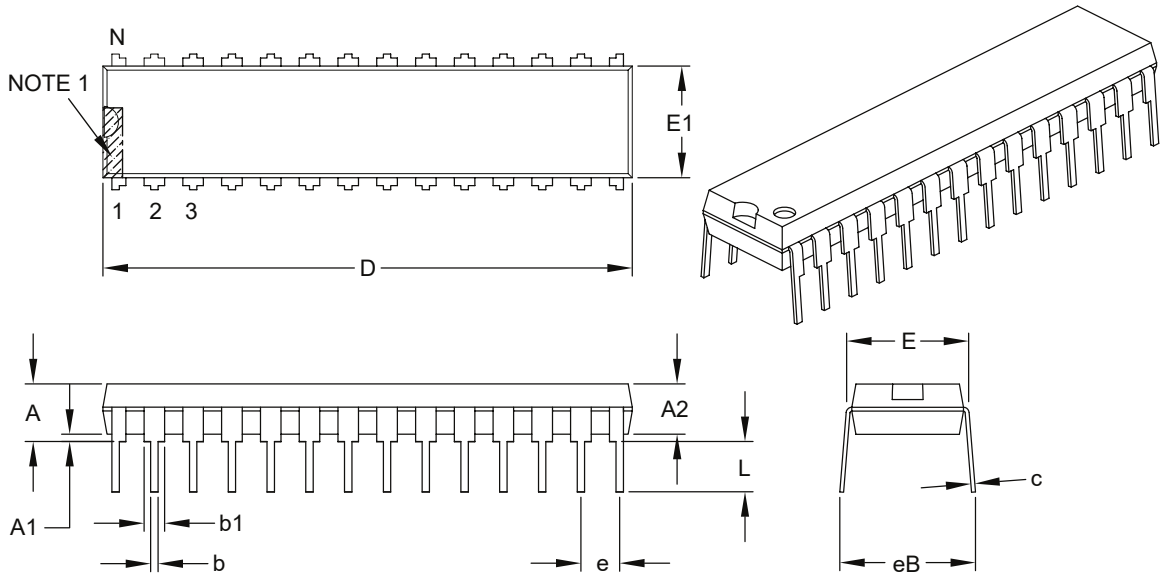
Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C, T_{AD} = 1µs							
Param No.	Sym.	Characteristic	Min.	Typ. †	Max.	Units	Conditions
AD01	N_R	Resolution	—	—	10	bit	
AD02	E_{IL}	Integral Error	—	±0.1	±1.0	LSb	ADC_{REF}+=3.0V, ADC_{REF}- = 0V
AD03	E_{DL}	Differential Error	—	±0.1	±1.0	LSb	ADC_{REF}+=3.0V, ADC_{REF}- = 0V
AD04	E_{OFF}	Offset Error	—	0.5	±2.0	LSb	ADC_{REF}+=3.0V, ADC_{REF}- = 0V
AD05	E_{GN}	Gain Error	—	±0.2	±1.0	LSb	ADC_{REF}+=3.0V, ADC_{REF}- = 0V
AD06	V_{ADREF}	ADC Reference Voltage (AD_{REF}+ - AD_{REF}-)	1.8	—	V_{DD}	V	
AD07	V_{AIN}	Full-Scale Range	AD_{REF}-	—	AD_{REF}+	V	
AD08	Z_{AIN}	Recommended Impedance of Analog Voltage Source	—	10	—	kΩ	
AD09	R_{VREF}	ADC Voltage Reference Ladder Impedance	—	50	—	kΩ	(**Note 3**)

* - These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B