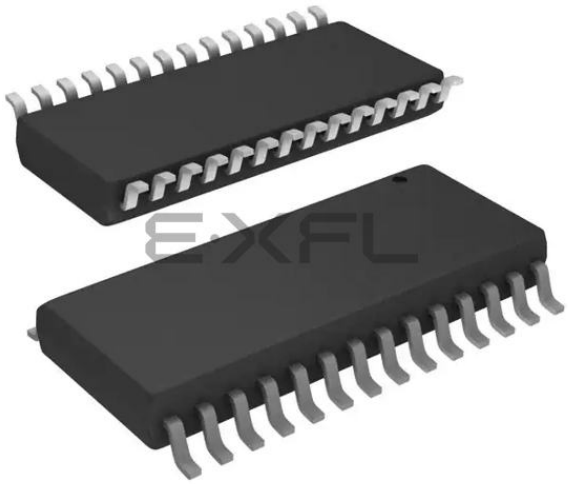

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f24q10-i-so

3.7.3 CONFIG3

Name: CONFIG3
Address: 0x300004

Configuration Word 3

Windowed Watchdog Timer

Bit	15	14	13	12	11	10	9	8
			WDTCCS[2:0]			WDTCWS[2:0]		
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
		WDTE[1:0]		WDTCPS[4:0]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	1	1	1	1	1

Bits 13:11 – WDTCCS[2:0] WDT Input Clock Selector bits

Value	Condition	Description
x	3.7.3.1 WDTE=00	These bits have no effect
111	3.7.3.1 WDTE≠00	Software Control
110 to 010	3.7.3.1 WDTE≠00	Reserved (Default to LFINTOSC)
001	3.7.3.1 WDTE≠00	WDT reference clock is the 31.25 kHz MFINTOSC
000	3.7.3.1 WDTE≠00	WDT reference clock is the 31.0 kHz LFINTOSC (default value)

Bits 10:8 – WDTCWS[2:0] WDT Window Select bits

WDTCWS	WDTCON1[WINDOW] at POR			Software control of WINDOW	Keyed access required?
	Value	Window delay Percent of time	Window opening Percent of time		
111	111	n/a	100	Yes	No
110	110	n/a	100	No	Yes
101	101	25	75		
100	100	37.5	62.5		
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

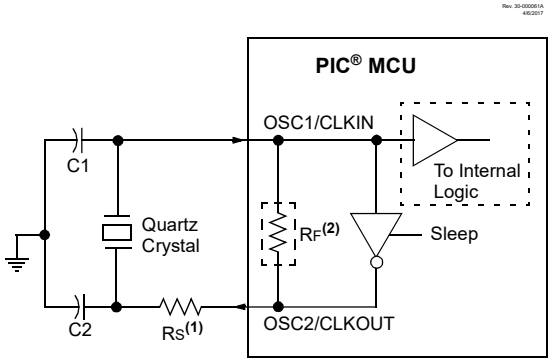
Bits 6:5 – WDTE[1:0] WDT Operating Mode bits

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification (above 500 kHz - 8 MHz).

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting (above 8 MHz).

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

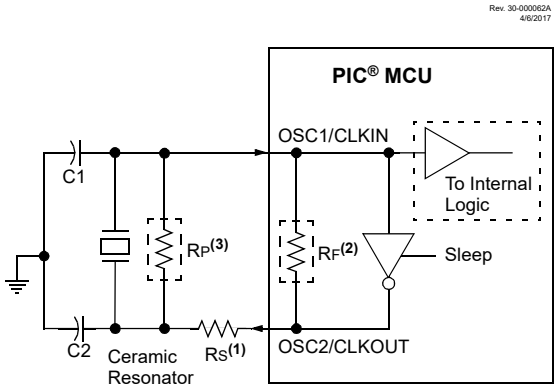
Figure 4-3. Quartz Crystal Operation (LP, XT or HS Mode)



Note:

1. A series resistor (R_S) may be required for quartz crystals with low drive level.
2. The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

Figure 4-4. Ceramic Resonator Operation (XT or HS Mode)



Note:

1. A series resistor (R_S) may be required for ceramic resonators with low drive level.
2. The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).
3. An additional parallel feedback resistor (R_P) may be required for proper ceramic resonator operation.

4.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR), or a wake-up from Sleep. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

5.6.2 CLKRCLK

Name: CLKRCLK
Address: 0xF3A

Clock Reference Clock Selection MUX

Bit	7	6	5	4	3	2	1	0
						CLK[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

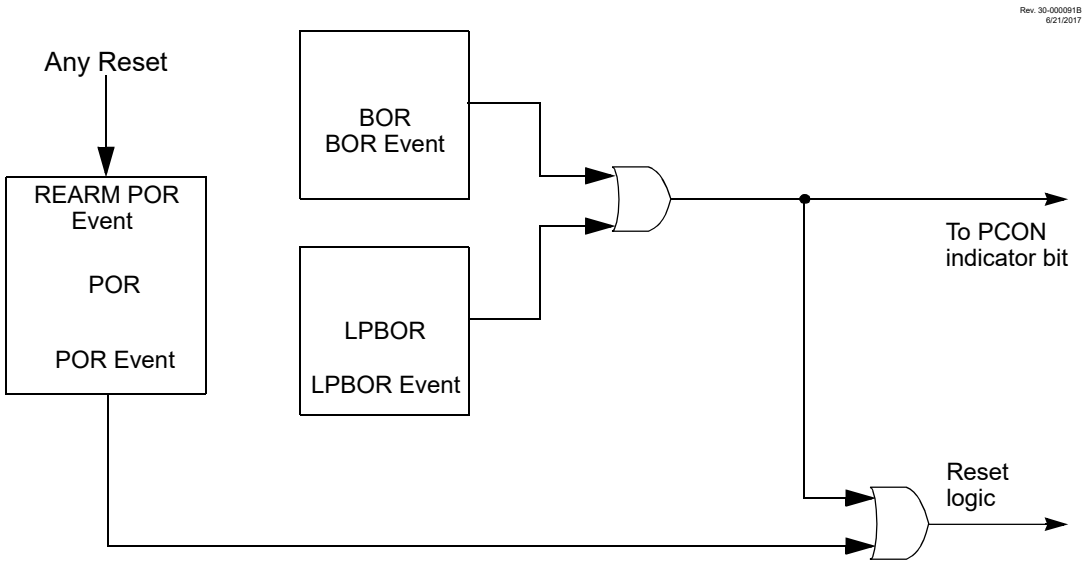
Bits 2:0 – CLK[2:0] CLKR Clock Selection bits
See the Clock Sources table.

8.3 Low-Power Brown-out Reset (LPBOR)

The Low-Power Brown-out Reset (LPBOR) provides an additional BOR circuit for low-power operation. Refer to the figure below to see how the BOR interacts with other modules.

The LPBOR is used to monitor the external V_{DD} pin. When too low of a voltage is detected, the device is held in Reset.

Figure 8-3. LPBOR, BOR, POR Relationship



8.3.1 Enabling LPBOR

The LPBOR is controlled by the $\overline{\text{LPBOREN}}$ bit of Configuration Word 2. When the device is erased, the LPBOR module defaults to disabled.

Related Links

3.7.2 CONFIG2

8.3.1.1 LPBOR Module Output

The output of the LPBOR module is a signal indicating whether or not a Reset is to be asserted. This signal is OR'd together with the Reset signal of the BOR module to provide the generic $\overline{\text{BOR}}$ signal, which goes to the PCON0 register and to the power control block.

8.4 $\overline{\text{MCLR}}$ Reset

The $\overline{\text{MCLR}}$ is an optional external input that can reset the device. The $\overline{\text{MCLR}}$ function is controlled by the MCLRE bit of Configuration Words and the LVP bit of Configuration Words (see table below). The $\overline{\text{RMCLR}}$ bit in the PCON0 register will be set to '0' if a $\overline{\text{MCLR}}$ has occurred.

9. (WWDT) Windowed Watchdog Timer

The Watchdog Timer (WDT) is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events. The Windowed Watchdog Timer (WWDT) differs in that CLRWDT instructions are only accepted when they are performed within a specific window during the time-out period.

The WWDT has the following features:

- Selectable clock source
- Multiple operating modes
  - WWDT is always on
  - WWDT is off when in Sleep
  - WWDT is controlled by software
  - WWDT is always off
- Configurable time-out period is from 1 ms to 256s (nominal)
- Configurable window size from 12.5% to 100% of the time-out period
- Multiple Reset conditions

13.12.1 CRCCON0

Name: CRCCON0
Address: 0xF77
Reset: 0

CRC Control Register 0

Bit	7	6	5	4	3	2	1	0
	EN	GO	BUSY	ACCM			SHIFTM	FULL
Access	R/W	R/W	RO	R/W			R/W	RO
Reset	0	0	0	0			0	0

Bit 7 – EN CRC Enable bit

Value	Description
1	CRC module is released from Reset
0	CRC is disabled and consumes no operating current

Bit 6 – GO CRC Start bit

Value	Description
1	Start CRC serial shifter
0	CRC serial shifter turned off

Bit 5 – BUSY CRC Busy bit

Value	Description
1	Shifting in progress or pending
0	All valid bits in shifter have been shifted into accumulator and EMPTY = 1

Bit 4 – ACCM Accumulator Mode bit

Value	Description
1	Data is augmented with zeros
0	Data is not augmented with zeros

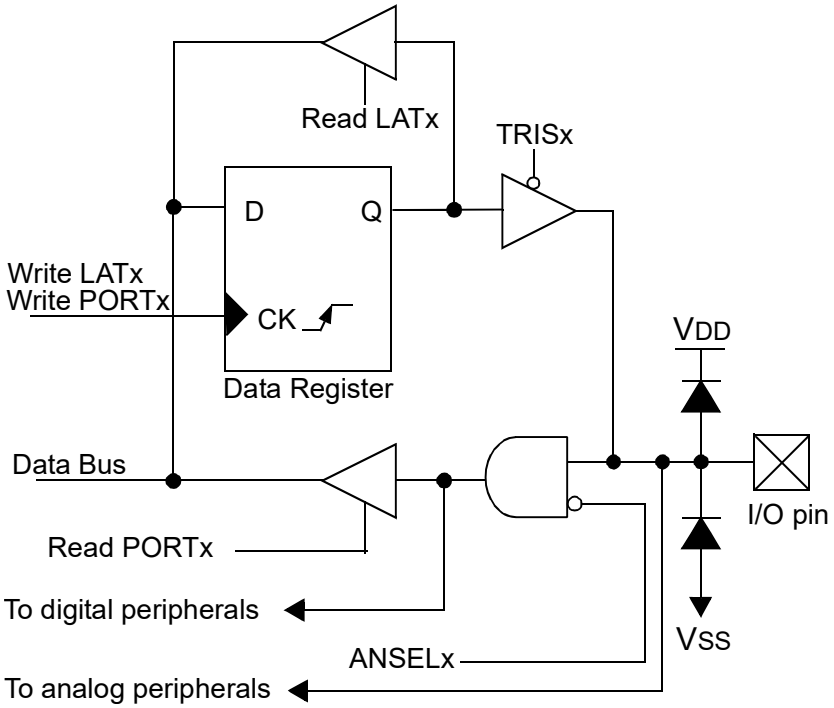
Bit 1 – SHIFTM Shift Mode bit

Value	Description
1	Shift right (LSb)
0	Shift left (MSb)

Bit 0 – FULL Data Path Full Indicator bit

Value	Description
1	CRCDATH/L registers are full
0	CRCDATH/L registers have shifted their data into the shifter

Figure 15-1. Generic I/O Port Operation



15.1 I/O Priorities

Each pin defaults to the PORT data latch after Reset. Other functions are selected with the peripheral pin select logic. See *"Peripheral Pin Select (PPS) Module"* for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx register. Digital output functions may continue to control the pin when it is in Analog mode.

Analog outputs, when enabled, take priority over digital outputs and force the digital output driver into a high-impedance state.

The pin function priorities are as follows:

1. Configuration bits
2. Analog outputs (disable the input buffers)
3. Analog inputs
4. Port inputs and outputs from PPS

Related Links

17. (PPS) Peripheral Pin Select Module

15.2 PORTx Registers

In this section the generic names such as PORTx, LATx, TRISx, etc. can be associated with all ports. For availability of PORTD refer to Table 15-1. The functionality of PORTE is different compared to other ports and is explained in a separate section.

Address	Name	Bit Pos.								
0x0F8C	PORTA	7:0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
0x0F8D	PORTB	7:0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
0x0F8E	PORTC	7:0	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
0x0F8F	Reserved									
0x0F90	PORTE	7:0					RE3			

15.5 Register Definitions: Port Control

15.5.7 TRISC

Name: TRISC
Address: 0xF89

Tri-State Control Register

Bit	7	6	5	4	3	2	1	0
	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – TRISCn TRISC Port I/O Tri-state Control bits

Value	Description
1	Port output driver is disabled
0	Port output driver is enabled

15.5.16 WPUC

Name: WPUC
Address: 0xF1B

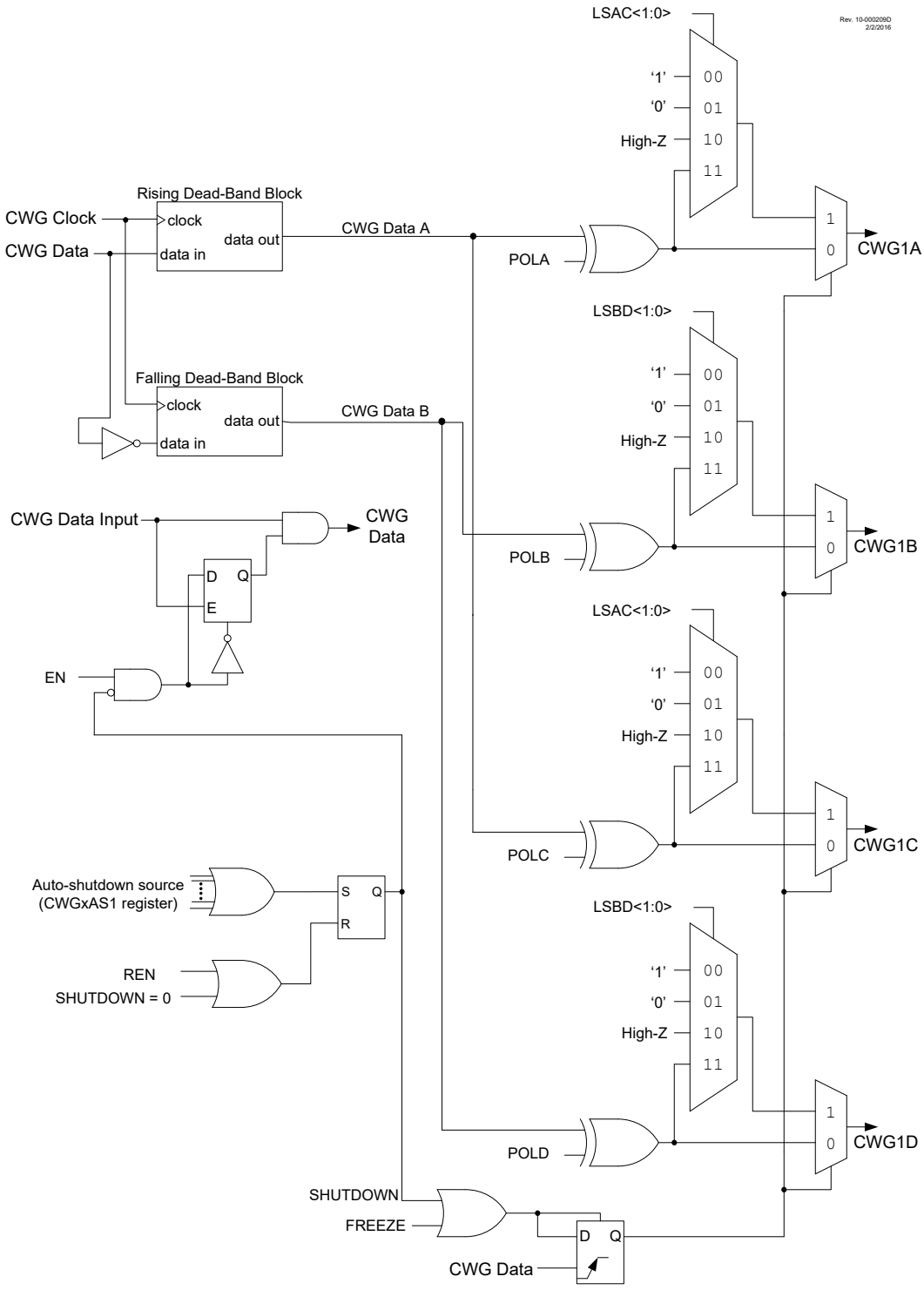
Weak Pull-up Register

Bit	7	6	5	4	3	2	1	0
	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – WPUCn Weak Pull-up PORTC Control bits

Value	Description
1	Weak Pull-up enabled
0	Weak Pull-up disabled

Figure 24-2. Simplified CWG Block Diagram (Half-Bridge Mode, MODE<2:0> = 100)



24.2.2 Push-Pull Mode

In Push-Pull mode, two output signals are generated, alternating copies of the input as illustrated in Figure 24-3. This alternation creates the push-pull effect required for driving some transformer-based

25.9 Effects of a Reset

Upon any device Reset, the DSM module is disabled. The user's firmware is responsible for initializing the module before enabling the output. All the registers are reset to their default values.

25.10 Peripheral Module Disable

The DSM module can be completely disabled using the PMD module to achieve maximum power saving. When the DSMMD bit of PMDx register is set, the DSM module is completely disabled. This puts the module in its lowest power consumption state. When enabled again all the registers of the DSM module default to POR status.

Related Links

7.4 Register Definitions: Peripheral Module Disable

Value	Mode	Description
x	SPI	Reserved
1	I²C	Start bit was detected last
0	I²C	Start bit was not detected last

Bit 2 – R/$\overline{W}$
Read/$\overline{Write}$ Information bit(2,3)

Value	Mode	Description
x	SPI	Reserved
1	I²C Slave	Read
0	I²C Slave	Write
1	I²C Master	Transmit is in progress
0	I²C Master	Transmit is not in progress

Bit 1 – UA Update Address bit (10-Bit Slave mode only)

Value	Mode	Description
x	All other modes	Reserved
1	I²C 10-bit Slave	Indicates that the user needs to update the address in the SSPxADD register
0	I²C 10-bit Slave	Address does not need to be updated

Bit 0 – BF
Buffer Full Status bit(5)

Value	Mode	Description
1	I²C Transmit	Character written to SSPxBUF has not been sent
0	I²C Transmit	SSPxBUF is ready for next character
1	SPI and I²C Receive	Received character in SSPxBUF has not been read
0	SPI and I²C Receive	Received character in SSPxBUF has been read

Note:

1. This bit is cleared on Reset and when SSPEN is cleared.
2. In I²C Slave mode this bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not $\overline{ACK}$ bit.
3. ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Active mode.
4. Polarity of clock state is set by the CKP bit.
5. I²C receive status does not include $\overline{ACK}$ and Stop bits.

recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. See the 27.1.2.4 Receive Framing Error section for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the EUSART receive FIFO and the RCxIF interrupt flag bit of the PIRx register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCxREG register.

Important: If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. See the 27.1.2.5 Receive Overrun Error section for more information.

27.1.2.3 Receive Interrupts

The RCxIF interrupt flag bit of the PIRx register is set whenever the EUSART receiver is enabled and there is an unread character in the receive FIFO. The RCxIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCxIF interrupts are enabled by setting all of the following bits:

- RCxIE, Interrupt Enable bit of the PIEx register
- PEIE, Peripheral Interrupt Enable bit of the INTCON register
- GIE, Global Interrupt Enable bit of the INTCON register

The RCxIF interrupt flag bit will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

27.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCxSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCxREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCxSTA register which resets the EUSART. Clearing the CREN bit of the RCxSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Important: If all receive characters in the receive FIFO have framing errors, repeated reads of the RCxREG will not clear the FERR bit.

27.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCxSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCxSTA register or by resetting the EUSART by clearing the SPEN bit of the RCxSTA register.

32.4.1 Comparator Output Synchronization

The output from a comparator can be synchronized with Timer1 by setting the SYNC bit.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Figure 32-2 Comparator Block Diagram and the Timer1 Block Diagram for more information.

Related Links

19. Timer1 Module with Gate Control

32.5 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator; a rising edge detector and a falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (CxINTP and/or CxINTN bits), the Corresponding Interrupt Flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, the following bits must be set:

- EN and POL bits
- CxIE bit of the PIE2 register
- INTP bit (for a rising edge detection)
- INTN bit (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

Important: Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the CxPOL bit, or by switching the comparator on or off with the CxEN bit.

32.6 Comparator Positive Input Selection

Configuring the 32.15.4.1 PCH bits direct an internal voltage reference or an analog pin to the non-inverting input of the comparator:

PCH	Positive Input Source
111	AVSS
110	FVR_Buffer2
101	DAC_Output
100	CxPCH not connected
011	CxPCH not connected
010	CxPCH not connected

32.15.3 CMxNCH

Name: CMxNCH
Address: 0xF36,0xF32

Comparator x Inverting Channel Select Register

Bit	7	6	5	4	3	2	1	0
						NCH[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – NCH[2:0] Comparator Inverting Input Channel Select bits

NCH	Negative Input Sources
111	AVSS
110	FVR_Buffer2
101	CxNCH not connected
100	CxNCH not connected
011	CxIN3-
010	CxIN2-
001	CxIN1-
000	CxIN0-

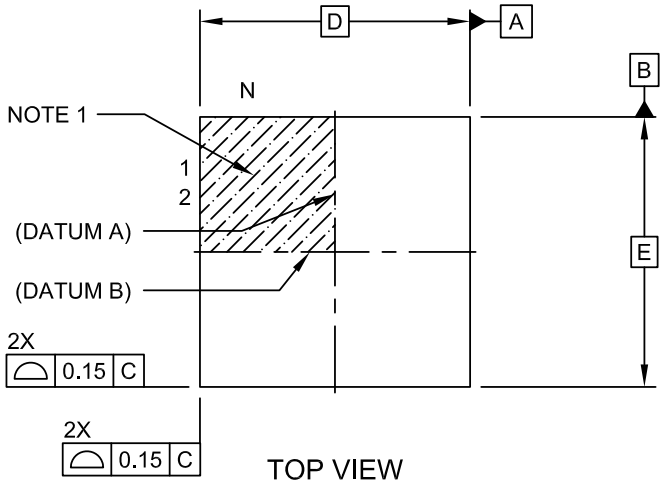
Address	Name	Bit Pos.								
0x0FB2	T6CLKCON	7:0					CS[3:0]			
0x0FB3	T6RST	7:0					RSEL[3:0]			
0x0FB4	T4TMR	7:0	TxTMR[7:0]							
0x0FB5	T4PR	7:0	TxPR[7:0]							
0x0FB6	T4CON	7:0	ON		CKPS[2:0]		OUTPS[3:0]			
0x0FB7	T4HLT	7:0	PSYNC	CPOL	CSYNC	MODE[4:0]				
0x0FB8	T4CLKCON	7:0					CS[3:0]			
0x0FB9	T4RST	7:0					RSEL[3:0]			
0x0FBA	T2TMR	7:0	TxTMR[7:0]							
0x0FBB	T2PR	7:0	TxPR[7:0]							
0x0FBC	T2CON	7:0	ON		CKPS[2:0]		OUTPS[3:0]			
0x0FBD	T2HLT	7:0	PSYNC	CPOL	CSYNC	MODE[4:0]				
0x0FBE	T2CLKCON	7:0					CS[3:0]			
0x0FBF	T2RST	7:0					RSEL[3:0]			
0x0FC0	TMR5	7:0	TMRxL[7:0]							
		15:8	TMRxH[7:0]							
0x0FC2	T5CON	7:0			CKPS[1:0]			$\overline{\text{SYNC}}$	RD16	ON
0x0FC3	T5GCON	7:0	GE	GPOL	GTM	GSPM	GGO/DONE	GVAL		
0x0FC4	TMR5GATE	7:0					GSS[3:0]			
0x0FC5	TMR5CLK	7:0					CS[3:0]			
0x0FC6	TMR3	7:0	TMRxL[7:0]							
		15:8	TMRxH[7:0]							
0x0FC8	T3CON	7:0			CKPS[1:0]			$\overline{\text{SYNC}}$	RD16	ON
0x0FC9	T3GCON	7:0	GE	GPOL	GTM	GSPM	GGO/DONE	GVAL		
0x0FCA	TMR3GATE	7:0					GSS[3:0]			
0x0FCB	TMR3CLK	7:0					CS[3:0]			
0x0FCC	TMR1	7:0	TMRxL[7:0]							
		15:8	TMRxH[7:0]							
0x0FCE	T1CON	7:0			CKPS[1:0]			$\overline{\text{SYNC}}$	RD16	ON
0x0FCF	T1GCON	7:0	GE	GPOL	GTM	GSPM	GGO/DONE	GVAL		
0x0FD0	TMR1GATE	7:0					GSS[3:0]			
0x0FD1	TMR1CLK	7:0					CS[3:0]			
0x0FD2	TMR0L	7:0	TMR0L[7:0]							
0x0FD3	TMR0H	7:0	TMR0H[7:0]							
0x0FD4	T0CON0	7:0	T0EN		T0OUT	T016BIT	T0OUTPS[3:0]			
0x0FD5	T0CON1	7:0	T0CS[2:0]			T0ASYNC	T0CKPS[3:0]			
0x0FD6	PCON1	7:0						$\overline{\text{RVREG}}$		$\overline{\text{RCM}}$
0x0FD7	PCON0	7:0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
0x0FD8	STATUS	7:0		$\overline{\text{TO}}$	$\overline{\text{PD}}$	N	OV	Z	DC	C
0x0FD9	FSR2	7:0	FSRL[7:0]							
		15:8					FSRH[3:0]			
0x0FDB	PLUSW2	7:0	PLUSW[7:0]							
0x0FDC	PREINC2	7:0	PREINC[7:0]							
0x0FDD	POSTDEC2	7:0	POSTDEC[7:0]							
0x0FDE	POSTINC2	7:0	POSTINC[7:0]							
0x0FDF	INDF2	7:0	INDF[7:0]							

REG = 35h

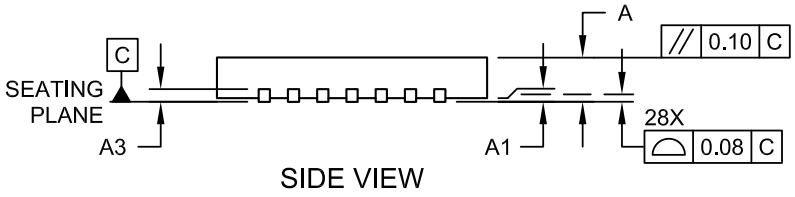
TBLRD	Table Read			
Syntax:	TBLRD (*; *+; *-; +*)			
Operands:	None			
Operation:	if TBLRD *, (Prog Mem (TBLPTR)) → TABLAT; TBLPTR – No Change; if TBLRD *+, (Prog Mem (TBLPTR)) → TABLAT; (TBLPTR) + 1 → TBLPTR; if TBLRD *-, (Prog Mem (TBLPTR)) → TABLAT; (TBLPTR) – 1 → TBLPTR; if TBLRD +*, (TBLPTR) + 1 → TBLPTR; (Prog Mem (TBLPTR)) → TABLAT;			
Status Affected:	None			
Encoding:	0000	0000	0000	10nn nn=0 * =1 *+ =2 *- =3 +*
Description:	This instruction is used to read the contents of Program Memory (P.M.). To address the program memory, a pointer called Table Pointer (TBLPTR) is used. The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-Mbyte address range. TBLPTR[0] = 0: Least Significant Byte of Program Memory Word TBLPTR[0] = 1: Most Significant Byte of Program Memory Word The TBLRD instruction can modify the value of TBLPTR as follows: • no change • post-increment • post-decrement • pre-increment			

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN]
With 0.55 mm Terminal Length

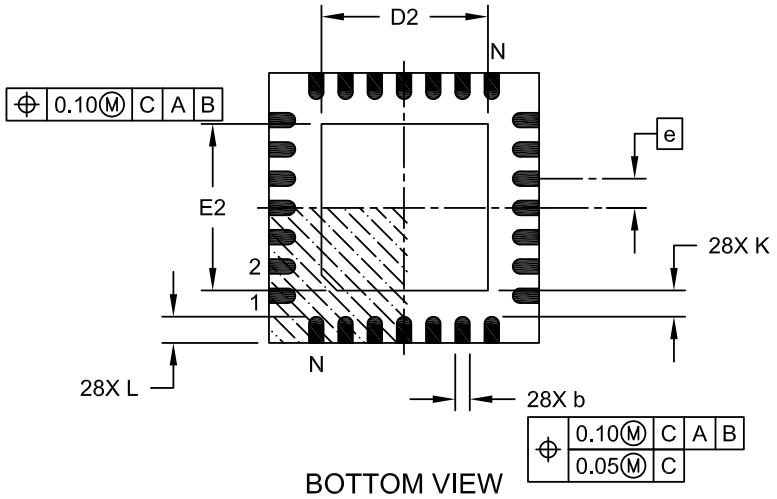
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Microchip Technology Drawing C04-105C Sheet 1 of 2

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