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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 64MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 24x10b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f25q10-i-ss |

| Value | Description |
|---|---|
| f | Reset Value is determined by fuse setting |
| g | Reset Value at POR for PPS re-mappable signals |

## 4.5 Register Summary - OSC

| Address | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0ED3 | OSCCON1 | 7:0 | | NOSC[2:0] | | | NDIV[3:0] | | | |
| 0x0ED4 | OSCCON2 | 7:0 | | COSC[2:0] | | | CDIV[3:0] | | | |
| 0x0ED5 | OSCCON3 | 7:0 | CSWHOLD | SOSCPWR | | ORDY | NOSCR | | | |
| 0x0ED6 | OSCSTAT | 7:0 | EXTOR | HFOR | MFOR | LFOR | SOR | ADOR | | PLLR |
| 0x0ED7 | OSCEN | 7:0 | EXTOEN | HFOEN | MFOEN | LFOEN | SOSCEN | ADOEN | | |
| 0x0ED8 | OSCTUNE | 7:0 | | | HFTUN[5:0] | | | | | |
| 0x0ED9 | OSCFRQ | 7:0 | | | | | HFFRQ[3:0] | | | |

## 4.6 Register Definitions: Oscillator Control

### 4.6.4 OSCSTAT

**Name:** OSCSTAT
**Address:** 0xED6

Oscillator Status Register 1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | EXTOR | HFOR | MFOR | LFOR | SOR | ADOR | | PLLR |
| Access | RO | RO | RO | RO | RO | RO | | RO |
| Reset | q | q | q | q | q | q | | q |

**Bit 7 – EXTOR** EXTOSC (external) Oscillator Ready bit

| Value | Description |
|---|---|
| 1 | The oscillator is ready to be used |
| 0 | The oscillator is not enabled, or is not yet ready to be used |

**Bit 6 – HFOR** HFINTOSC Oscillator Ready bit

| Value | Description |
|---|---|
| 1 | The oscillator is ready to be used |
| 0 | The oscillator is not enabled, or is not yet ready to be used |

**Bit 5 – MFOR** MFINTOSC Oscillator Ready bit

| Value | Description |
|---|---|
| 1 | The oscillator is ready to be used |
| 0 | The oscillator is not enabled, or is not yet ready to be used |

**Bit 4 – LFOR** LFINTOSC Oscillator Ready bit

| Value | Description |
|---|---|
| 1 | The oscillator is ready to be used |
| 0 | The oscillator is not enabled, or is not yet ready to be used |

**Bit 3 – SOR** Secondary (Timer1) Oscillator Ready bit

| Value | Description |
|---|---|
| 1 | The oscillator is ready to be used |
| 0 | The oscillator is not enabled, or is not yet ready to be used |

**Bit 2 – ADOR** ADC Oscillator Ready bit

| Value | Description |
|---|---|
| 1 | The oscillator is ready to be used |
| 0 | The oscillator is not enabled, or is not yet ready to be used |

**Bit 0 – PLLR** PLL Ready bit

### 5.6.1 CLKRCON

**Name:** CLKRCON
**Address:** 0xF39

Reference Clock Control Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | EN | | | DC[1:0] | | DIV[2:0] | | |
| Access | R/W | | | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | | | 1 | 0 | 0 | 0 | 0 |

**Bit 7 – EN**
Reference Clock Module Enable bit

| Value | Description |
|---|---|
| 1 | Reference clock module enabled |
| 0 | Reference clock module is disabled |

**Bits 4:3 – DC[1:0]**
Reference Clock Duty Cycle bits(1)

| Value | Description |
|---|---|
| 11 | Clock outputs duty cycle of 75% |
| 10 | Clock outputs duty cycle of 50% |
| 01 | Clock outputs duty cycle of 25% |
| 00 | Clock outputs duty cycle of 0% |

**Bits 2:0 – DIV[2:0]**
Reference Clock Divider bits

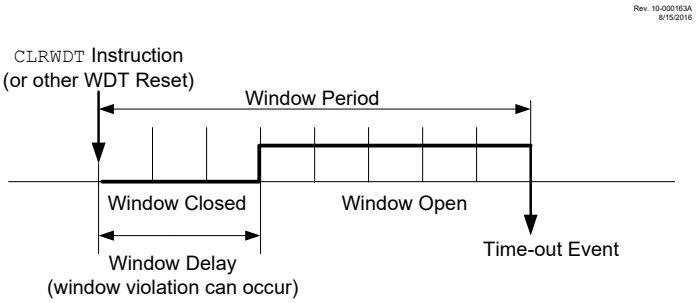
| Value | Description |
|---|---|
| 111 | Base clock value divided by 128 |
| 110 | Base clock value divided by 64 |
| 101 | Base clock value divided by 32 |
| 100 | Base clock value divided by 16 |
| 011 | Base clock value divided by 8 |
| 010 | Base clock value divided by 4 |
| 001 | Base clock value divided by 2 |
| 000 | Base clock value |

**Note:**

1. Bits are valid for reference clock divider values of two or larger, the base clock cannot be further divided.

| Conditions | WWDT |
|---|---|
| WDTE = 10 and enter Sleep | |
| CLRWDT Command | |
| Oscillator Fail Detected | |
| Exit Sleep + System Clock = SOSC, EXTRC, INTOSC, EXTCLK | |
| Exit Sleep + System Clock = XT, HS, LP | Cleared until the end of OST |
| Change INTOSC divider (IRCF bits) | Unaffected |

**Figure 9-2. Window Period and Delay**




**Related Links**

4.2.1.3 Oscillator Start-up Timer (OST)

10.8.5 STATUS

8.14.2 PCON0

10. Memory Organization

### 13.12.4 CRCACC

**Name:** CRCACC
**Address:** 0xF71
**Reset:** 0

CRC Accumulator Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | CRCACCH[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CRCACCL[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 15:8 – CRCACCH[7:0]** CRC Accumulator Register most significant byte
Writing to this register writes the Most Significant Byte of the CRC accumulator register. Reading from this register reads the Most Significant Byte of the CRC accumulator.

**Bits 7:0 – CRCACCL[7:0]** CRC Accumulator Register least significant byte
Writing to this register writes the Least Significant Byte of the CRC accumulator register. Reading from this register reads the Least Significant Byte of the CRC accumulator.

### 14.13.7 PIR5

**Name:** PIR5
**Address:** 0xECA

Peripheral Interrupt Request (Flag) Register 5

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | TMR5GIF | TMR3GIF | TMR1GIF |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 0 | 0 | 0 |

**Bit 2 – TMR5GIF** TMR5 Gate Interrupt Flag bit

| Value | Description |
|---|---|
| 1 | TMR5 gate interrupt occurred (must be cleared in software) |
| 0 | No TMR5 gate occurred |

**Bit 1 – TMR3GIF** TMR3 Gate Interrupt Flag bit

| Value | Description |
|---|---|
| 1 | TMR3 gate interrupt occurred (must be cleared in software) |
| 0 | No TMR3 gate occurred |

**Bit 0 – TMR1GIF** TMR1 Gate Interrupt Flag bit

| Value | Description |
|---|---|
| 1 | TMR1 gate interrupt occurred (must be cleared in software) |
| 0 | No TMR1 gate occurred |

### 14.13.16 PIE6

**Name:** PIE6
**Address:** 0xEC3

Peripheral Interrupt Enable Register 6

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | CCP2IE | CCP1IE |
| Access | | | | | | | R/W | R/W |
| Reset | | | | | | | 0 | 0 |

**Bit 1 – CCP2IE** ECCP2 Interrupt Enable bit

| Value | Description |
|---|---|
| 1 | Enabled |
| 0 | Disabled |

**Bit 0 – CCP1IE** ECCP1 Interrupt Enable bit

| Value | Description |
|---|---|
| 1 | Enabled |
| 0 | Disabled |

### 15.5.4 PORTE

**Name:** PORTE
**Address:** 0xF90

PORTE Register
**Note:** Writes to PORTE are actually written to the corresponding LATE register.
Reads from PORTE register return actual I/O pin values.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | RE3 | | | |
| Access | | | | | R/W | | | |
| Reset | | | | | x | | | |

**Bit 3 – RE3** Port I/O Value bits
**Note:** Bit RE3 is read-only, and will read ‘1’ when MCLRE = 1 (Master Clear enabled).

Reset States: POR/BOR = x
All Other Resets = u

| Value | Description |
|---|---|
| 1 | Port pin is ≥ $V_{IH}$ |
| 0 | Port pin is ≤ $V_{IL}$ |

### 15.5.7 TRISC

**Name:** TRISC
**Address:** 0xF89

Tri-State Control Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 0, 1, 2, 3, 4, 5, 6, 7 – TRISCn** TRISC Port I/O Tri-state Control bits

| Value | Description |
|---|---|
| 1 | Port output driver is disabled |
| 0 | Port output driver is enabled |

### 21.6.4 CCPTMRS

**Name:** CCPTMRS
**Address:** 0xFAD

CCP Timers Control Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P4TSEL[1:0] | | P3TSEL[1:0] | | C2TSEL[1:0] | | C1TSEL[1:0] | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

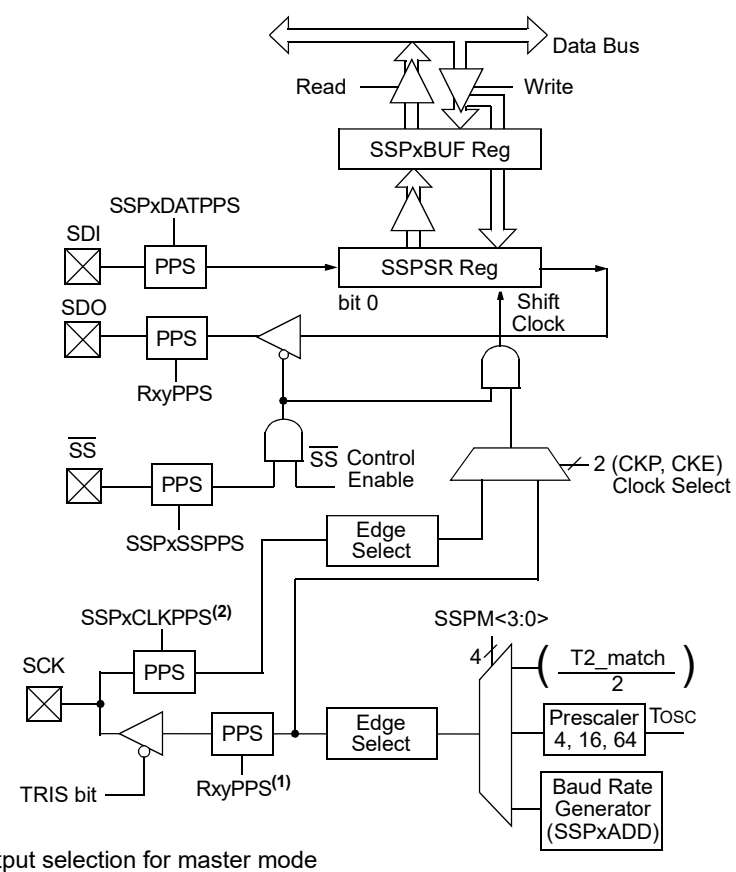
**Bits 4:5, 6:7 – PnTSEL** PWMn Timer Selection bits

| Value | Description |
|---|---|
| 11 | PWMn based on Timer6 |
| 10 | PWMn based on Timer4 |
| 01 | PWMn based on Timer2 |
| 00 | Reserved |

**Bits 0:1, 2:3 – CnTSEL** CCPn Timer Selection bits

| Value | Description |
|---|---|
| 11 | CCPn is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode |
| 10 | CCPn is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode |
| 01 | CCPn is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode |
| 00 | Reserved |

**Figure 26-1. MSSP Block Diagram (SPI mode)**




**Note 1:** Output selection for master mode

**2:** Input selection for slave and master mode

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

The figure below shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

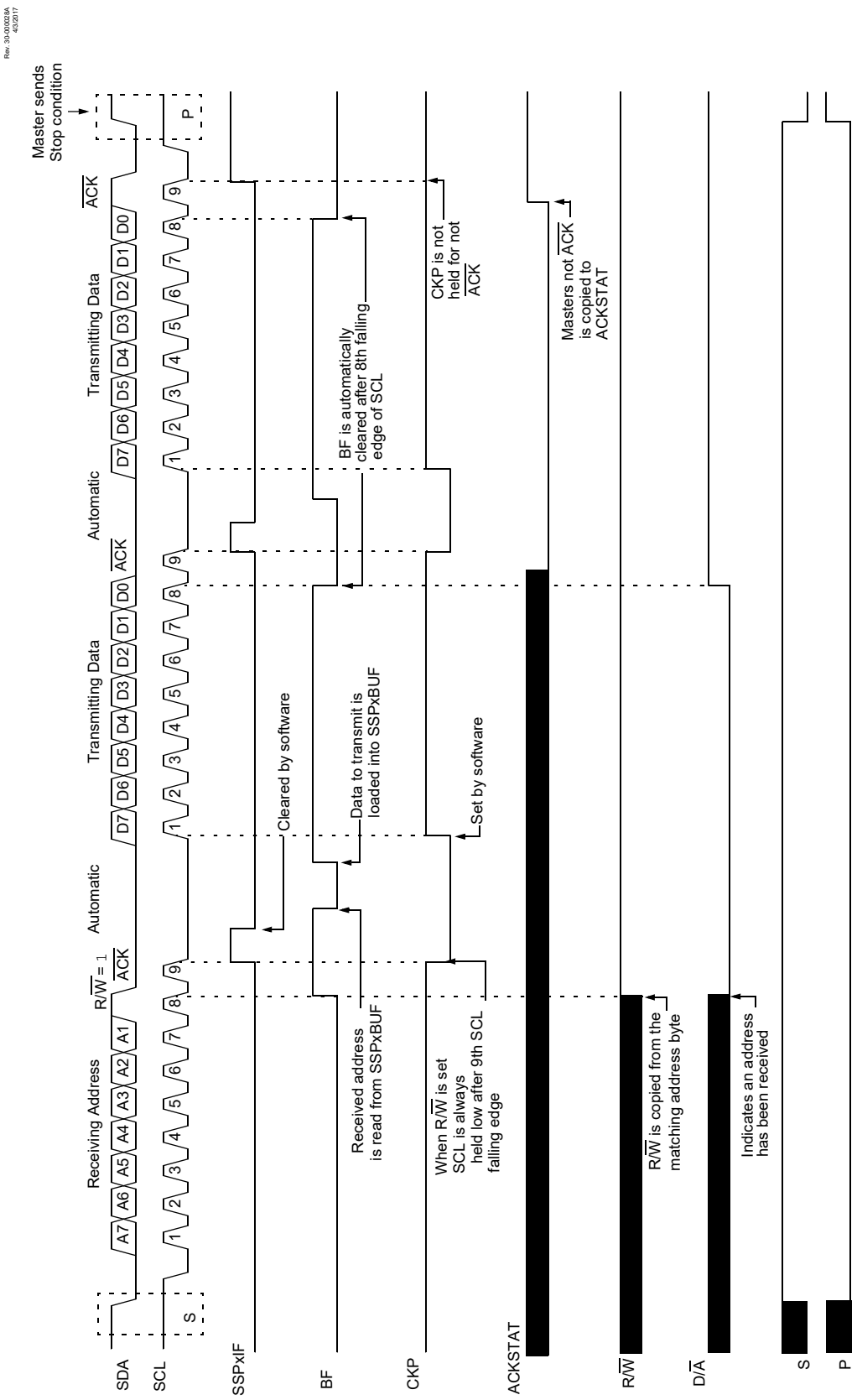
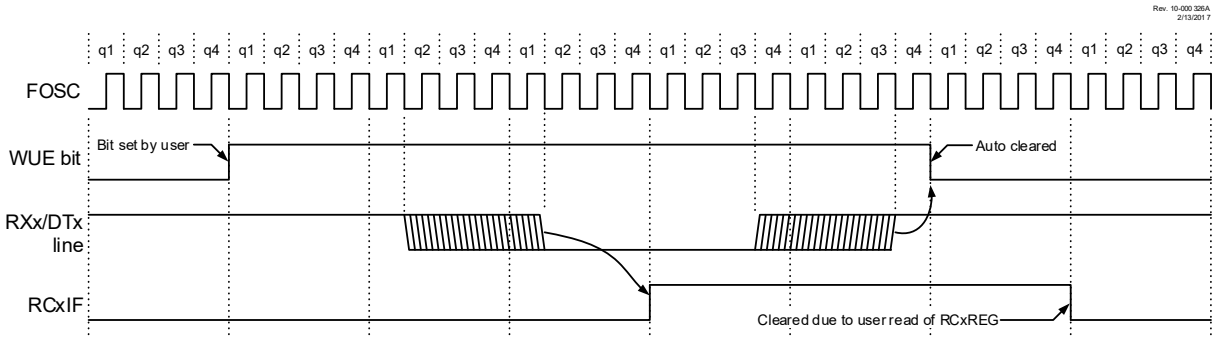


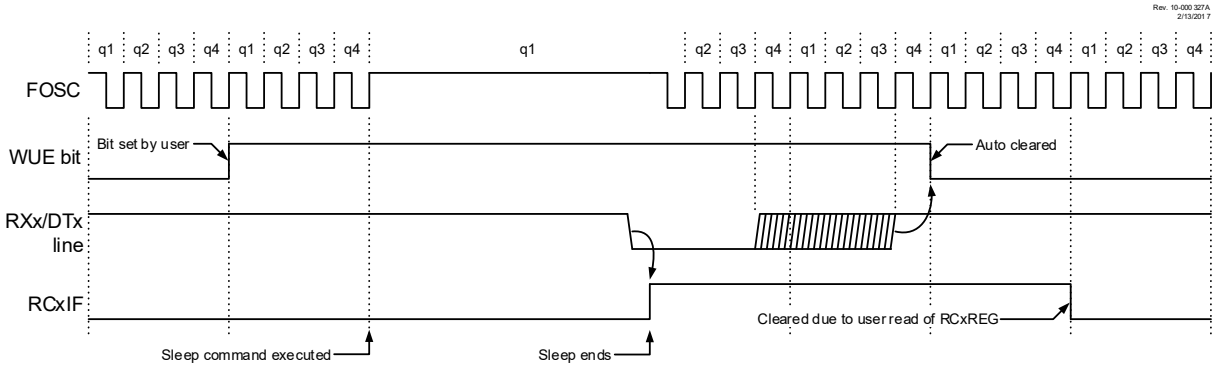

**Figure 26-18. I²C Slave, 7-bit Address, Transmission (AHEN = 0)**

**Figure 27-7. Auto-Wake-up Bit (WUE) Timing During Normal Operation**




**Note 1:** The EUSART remains in idle while the WUE bit is set.

**Figure 27-8. Auto-Wake-up Bit (WUE) Timings During Sleep**




**Note 1:** The EUSART remains in idle while the WUE bit is set.

### 27.2.4 Break Character Sequence

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. A Break character consists of a Start bit, followed by 12 '0' bits and a Stop bit.

To send a Break character, set the SENDB and TXEN bits of the TXxSTA register. The Break character transmission is then initiated by a write to the TXxREG. The value of data written to TXxREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

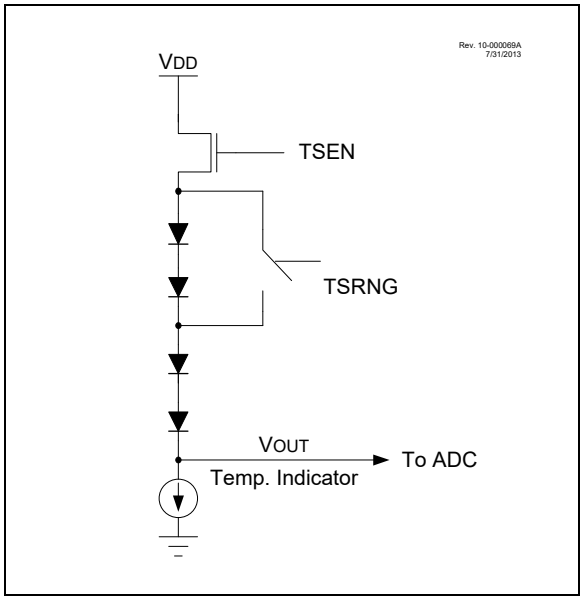
The TRMT bit of the TXxSTA register indicates when the transmit operation is active or idle, just as it does during normal transmission. See Figure 27-9 for more detail.

#### 27.2.4.1 Break and Sync Transmit Sequence

The following sequence will start a message frame header made up of a Break, followed by an auto-baud Sync byte. This sequence is typical of a LIN bus master.

1. Configure the EUSART for the desired mode.
2. Set the TXEN and SENDB bits to enable the Break sequence.
3. Load the TXxREG with a dummy character to initiate transmission (the value is ignored).

**Figure 29-1. Temperature Circuit Diagram**




**Related Links**

28. (FVR) Fixed Voltage Reference

## 29.2 Minimum Operating $V_{DD}$

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, $V_{DD}$, must be high enough to ensure that the temperature circuit is correctly biased.

Table 29-1 shows the recommended minimum $V_{DD}$ vs. range setting.

**Table 29-1. Recommended $V_{DD}$ vs. Range**

| Min. $V_{DD}$, TSRNG = 1 | Min. $V_{DD}$, TSRNG = 0 |
|---|---|
| 3.6V | 1.8V |

## 29.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to *"Analog-to-Digital Converter with Computation (ADC$^2$) Module"* chapter for detailed information.

**Related Links**

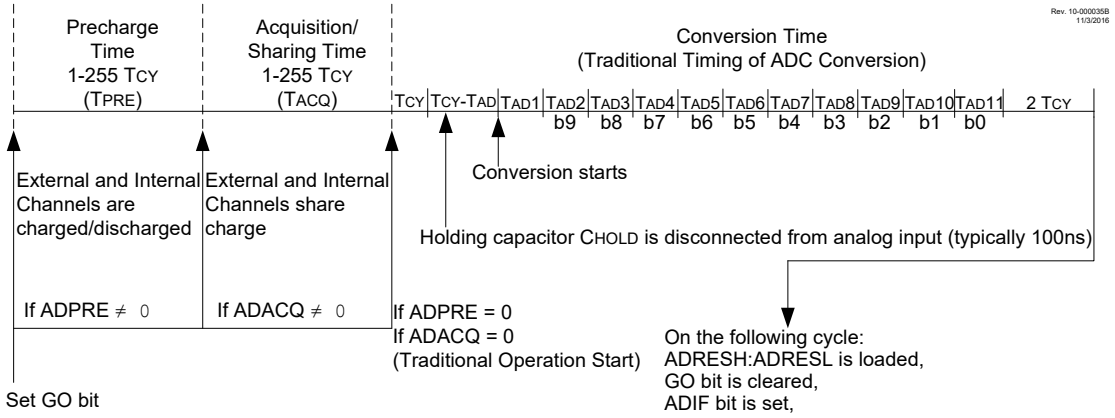
31. (ADC2) Analog-to-Digital Converter with Computation Module

| ADC Clock Period ($T_{AD}$) | | Device Frequency ($F_{OSC}$) | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ADC Clock Source | ADCLK | 64 MHz | 32 MHz | 20 MHz | 16 MHz | 8 MHz | 4 MHz | 1 MHz |
| $F_{OSC}$/128 | 111111 | 2.0 µs | 4.0 µs | 6.4 µs | 8.0 µs | 16.0 µs(3) | 32.0 µs(2) | 128.0 µs(2) |
| FRC | ADCS=1 | 1.0-6.0 µs | 1.0-6.0 µs | 1.0-6.0 µs | 1.0-6.0 µs | 1.0-6.0 µs | 1.0-6.0 µs | 1.0-6.0 µs |

**Note:**

1. See $T_{AD}$ parameter in the "Electrical Specifications" section for FRC source typical $T_{AD}$ value.
2. These values violate the required $T_{AD}$ time.
3. Outside the recommended $T_{AD}$ time.
4. The ADC clock period ($T_{AD}$) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock $F_{OSC}$. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

**Figure 31-2. Analog-to-Digital Conversion $T_{AD}$ Cycles**




**Related Links**

38.4.8 Analog-to-Digital Converter (ADC) Conversion Timing Specifications

### 31.1.5 Interrupts

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital Conversion. The ADC Interrupt Flag is the ADIF bit in the PIRx register. The ADC Interrupt Enable is the ADIE bit in the PIEx register. The ADIF bit must be cleared in software.

**Important:**

1. The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.
2. The ADC operates during Sleep only when the FRC oscillator is selected.

| Address | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0EF4 | RC2PPS | 7:0 | | | | PPS[4:0] | | | | |
| 0x0EF5 | RC3PPS | 7:0 | | | | PPS[4:0] | | | | |
| 0x0EF6 | RC4PPS | 7:0 | | | | PPS[4:0] | | | | |
| 0x0EF7 | RC5PPS | 7:0 | | | | PPS[4:0] | | | | |
| 0x0EF8 | RC6PPS | 7:0 | | | | PPS[4:0] | | | | |
| 0x0EF9 | RC7PPS | 7:0 | | | | PPS[4:0] | | | | |
| 0x0EFA ... 0x0F04 | Reserved | | | | | | | | | |
| 0x0F05 | IOCAF | 7:0 | IOCAF7 | IOCAF6 | IOCAF5 | IOCAF4 | IOCAF3 | IOCAF2 | IOCAF1 | IOCAF0 |
| 0x0F06 | IOCAN | 7:0 | IOCAN7 | IOCAN6 | IOCAN5 | IOCAN4 | IOCAN3 | IOCAN2 | IOCAN1 | IOCAN0 |
| 0x0F07 | IOCAP | 7:0 | IOCAP7 | IOCAP6 | IOCAP5 | IOCAP4 | IOCAP3 | IOCAP2 | IOCAP1 | IOCAP0 |
| 0x0F08 | INLVLA | 7:0 | INLVLA7 | INLVLA6 | INLVLA5 | INLVLA4 | INLVLA3 | INLVLA2 | INLVLA1 | INLVLA0 |
| 0x0F09 | SLRCONA | 7:0 | SLRA7 | SLRA6 | SLRA5 | SLRA4 | SLRA3 | SLRA2 | SLRA1 | SLRA0 |
| 0x0F0A | ODCONA | 7:0 | ODCA7 | ODCA6 | ODCA5 | ODCA4 | ODCA3 | ODCA2 | ODCA1 | ODCA0 |
| 0x0F0B | WPUA | 7:0 | WPUA7 | WPUA6 | WPUA5 | WPUA4 | WPUA3 | WPUA2 | WPUA1 | WPUA0 |
| 0x0F0C | ANSELA | 7:0 | ANSELA7 | ANSELA6 | ANSELA5 | ANSELA4 | ANSELA3 | ANSELA2 | ANSELA1 | ANSELA0 |
| 0x0F0D | IOCBF | 7:0 | IOCBF7 | IOCBF6 | IOCBF5 | IOCBF4 | IOCBF3 | IOCBF2 | IOCBF1 | IOCBF0 |
| 0x0F0E | IOCBN | 7:0 | IOCBN7 | IOCBN6 | IOCBN5 | IOCBN4 | IOCBN3 | IOCBN2 | IOCBN1 | IOCBN0 |
| 0x0F0F | IOCBP | 7:0 | IOCBP7 | IOCBP6 | IOCBP5 | IOCBP4 | IOCBP3 | IOCBP2 | IOCBP1 | IOCBP0 |
| 0x0F10 | INLVLB | 7:0 | INLVLB7 | INLVLB6 | INLVLB5 | INLVLB4 | INLVLB3 | INLVLB2 | INLVLB1 | INLVLB0 |
| 0x0F11 | SLRCONB | 7:0 | SLRB7 | SLRB6 | SLRB5 | SLRB4 | SLRB3 | SLRB2 | SLRB1 | SLRB0 |
| 0x0F12 | ODCONB | 7:0 | ODCB7 | ODCB6 | ODCB5 | ODCB4 | ODCB3 | ODCB2 | ODCB1 | ODCB0 |
| 0x0F13 | WPUB | 7:0 | WPUB7 | WPUB6 | WPUB5 | WPUB4 | WPUB3 | WPUB2 | WPUB1 | WPUB0 |
| 0x0F14 | ANSELB | 7:0 | ANSELB7 | ANSELB6 | ANSELB5 | ANSELB4 | ANSELB3 | ANSELB2 | ANSELB1 | ANSELB0 |
| 0x0F15 | IOCCF | 7:0 | IOCCF7 | IOCCF6 | IOCCF5 | IOCCF4 | IOCCF3 | IOCCF2 | IOCCF1 | IOCCF0 |
| 0x0F16 | IOCCN | 7:0 | IOCCN7 | IOCCN6 | IOCCN5 | IOCCN4 | IOCCN3 | IOCCN2 | IOCCN1 | IOCCN0 |
| 0x0F17 | IOCCP | 7:0 | IOCCP7 | IOCCP6 | IOCCP5 | IOCCP4 | IOCCP3 | IOCCP2 | IOCCP1 | IOCCP0 |
| 0x0F18 | INLVLC | 7:0 | INLVLC7 | INLVLC6 | INLVLC5 | INLVLC4 | INLVLC3 | INLVLC2 | INLVLC1 | INLVLC0 |
| 0x0F19 | SLRCONC | 7:0 | SLRC7 | SLRC6 | SLRC5 | SLRC4 | SLRC3 | SLRC2 | SLRC1 | SLRC0 |
| 0x0F1A | ODCONC | 7:0 | ODCC7 | ODCC6 | ODCC5 | ODCC4 | ODCC3 | ODCC2 | ODCC1 | ODCC0 |
| 0x0F1B | WPUC | 7:0 | WPUC7 | WPUC6 | WPUC5 | WPUC4 | WPUC3 | WPUC2 | WPUC1 | WPUC0 |
| 0x0F1C | ANSELC | 7:0 | ANSELC7 | ANSELC6 | ANSELC5 | ANSELC4 | ANSELC3 | ANSELC2 | ANSELC1 | ANSELC0 |
| 0x0F1D ... 0x0F21 | Reserved | | | | | | | | | |
| 0x0F22 | IOCEF | 7:0 | | | | | IOCEF3 | | | |
| 0x0F23 | IOCEN | 7:0 | | | | | IOCEN3 | | | |
| 0x0F24 | IOCEP | 7:0 | | | | | IOCEP3 | | | |
| 0x0F25 | INLVLE | 7:0 | | | | | INLVLE3 | | | |
| 0x0F26 ... 0x0F27 | Reserved | | | | | | | | | |
| 0x0F28 | WPUE | 7:0 | | | | | WPUE3 | | | |
| 0x0F29 | Reserved | | | | | | | | | |
| 0x0F2A | HLVDCON0 | 7:0 | EN | | OUT | RDY | | | INTH | INTL |

**Table 36-2. Instruction Set**

| Mnemonic, Operands | | Description | Cycles | 16-Bit Instruction Word | | | | Status Affected | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MSb | | | LSb | | |
| BYTE-ORIENTED OPERATIONS | | | | | | | | | |
| ADDWF | f, d, a | Add WREG and f | 1 | 0010 | 01da | ffff | ffff | C, DC, Z, OV, N | 1, 2 |
| ADDWFC | f, d, a | Add WREG and CARRY bit to f | 1 | 0010 | 00da | ffff | ffff | C, DC, Z, OV, N | 1, 2 |
| ANDWF | f, d, a | AND WREG with f | 1 | 0001 | 01da | ffff | ffff | Z, N | 1, 2 |
| CLRF | f, a | Clear f | 1 | 0110 | 101a | ffff | ffff | Z | 2 |
| COMF | f, d, a | Complement f | 1 | 0001 | 11da | ffff | ffff | Z, N | 1, 2 |
| CPFSEQ | f, a | Compare f with WREG, skip = | 1 (2 or 3) | 0110 | 001a | ffff | ffff | None | 4 |
| CPFSGT | f, a | Compare f with WREG, skip > | 1 (2 or 3) | 0110 | 010a | ffff | ffff | None | 4 |
| CPFSLT | f, a | Compare f with WREG, skip < | 1 (2 or 3) | 0110 | 000a | ffff | ffff | None | 1, 2 |
| DECF | f, d, a | Decrement f | 1 | 0000 | 01da | ffff | ffff | C, DC, Z, OV, N | 1, 2, 3, 4 |
| DECFSZ | f, d, a | Decrement f, Skip if 0 | 1 (2 or 3) | 0010 | 11da | ffff | ffff | None | 1, 2, 3, 4 |
| DCFSNZ | f, d, a | Decrement f, Skip if Not 0 | 1 (2 or 3) | 0100 | 11da | ffff | ffff | None | 1, 2 |
| INCF | f, d, a | Increment f | 1 | 0010 | 10da | ffff | ffff | C, DC, Z, OV, N | 1, 2, 3, 4 |
| INCFSZ | f, d, a | Increment f, Skip if 0 | 1 (2 or 3) | 0011 | 11da | ffff | ffff | None | 4 |
| INFSNZ | f, d, a | Increment f, Skip if Not 0 | 1 (2 or 3) | 0100 | 11da | ffff | ffff | None | 1, 2 |
| IORWF | f, d, a | Inclusive OR WREG with f | 1 | 0001 | 00da | ffff | ffff | Z, N | 1, 2 |
| MOVF | f, d, a | Move f | 1 | 0101 | 00da | ffff | ffff | Z, N | 1 |
| MOVFF | $f_s$, $f_d$ | Move $f_s$ (source) to 1st word | 2 | 1100 | ffff | ffff | ffff | None | |

### 36.1.1 Standard Instruction Set

| ADDLW | ADD literal to W | | | |
|---|---|---|---|---|
| Syntax: | ADDLW k | | | |
| Operands: | 0 ≤ k ≤ 255 | | | |
| Operation: | (W) + k → W | | | |
| Status Affected: | N, OV, C, DC, Z | | | |
| Encoding: | 0000 | 1111 | kkkk | kkkk |
| Description: | The contents of W are added to the 8-bit literal ‘k’ and the result is placed in W. | | | |
| Words: | 1 | | | |
| Cycles: | 1 | | | |

| Q Cycle Activity: | | | |
|---|---|---|---|
| Q1 | Q2 | Q3 | Q4 |
| Decode | Read literal ‘k’ | Process Data | Write to W |

| Example: | ADDLW | 15h |
|---|---|---|
| Before Instruction<br>W = 10h<br>After Instruction<br>W = 25h | | |

| ADDWF | ADD W to f | | | |
|---|---|---|---|---|
| Syntax: | ADDWF f {,d {,a}} | | | |
| Operands: | 0 ≤ f ≤ 255<br>d ∈ [0,1]<br>a ∈ [0,1] | | | |
| Operation: | (W) + (f) → dest | | | |
| Status Affected: | N, OV, C, DC, Z | | | |
| Encoding: | 0010 | 01da | ffff | ffff |
| Description: | Add W to register ‘f’. If ‘d’ is ‘0’, the result is stored in W. If ‘d’ is ‘1’, the result is stored back in register ‘f’ (default).<br>If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank. | | | |

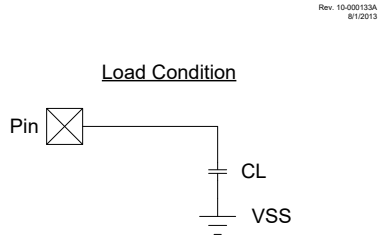
| Standard Operating Conditions (unless otherwise stated) | | | | | |
|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Typ.** | **Units** | **Conditions** |
| | | | 24 | °C/W | 28-pin SSOP package |
| | | | 24 | °C/W | 28-pin UQFN 4x4mm package |
| | | | 24 | °C/W | 28-pin QFN 6x6mm package |
| TH03 | $T_{JMAX}$ | Maximum Junction Temperature | 150 | °C | |
| TH04 | PD | Power Dissipation | — | W | $PD=P_{INTERNAL}+P_{I/O}$ (3) |
| TH05 | $P_{INTERNAL}$ | Internal Power Dissipation | — | W | $P_{INTERNAL}=I_{DD}xV_{DD}$ (1) |
| TH06 | $P_{I/O}$ | I/O Power Dissipation | — | W | $P_{I/O}=\Sigma(I_{OL}*V_{OL})+\Sigma(I_{OH}*(V_{DD}-V_{OH}))$ |
| TH07 | $P_{DER}$ | Derated Power | — | W | $P_{DER}=PD_{MAX}\ (T_J-T_A)/\theta_{JA}$ (2) |

**Note:**

1. $I_{DD}$ is current to run the chip alone without driving any load on the output pins.
2. $T_A$ = Ambient Temperature, $T_J$ = Junction Temperature.
3. See *"Absolute Maximum Ratings"* for total power dissipation.

## 38.4 AC Characteristics

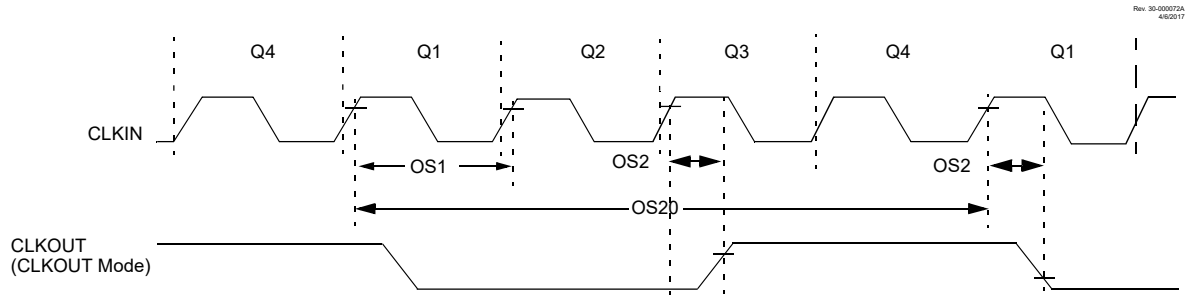
**Figure 38-3. Load Conditions**




**Legend:** CL=50 pF for all pins

### 38.4.1 External Clock/Oscillator Timing Requirements

**Figure 38-4. Clock Timing**




**Note:** See table below.