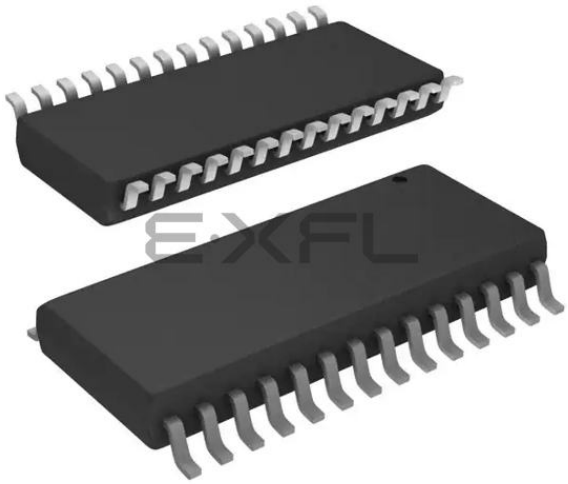

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f25q10t-i-so

  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if external clock stops
- Oscillator Start-up Timer (OST)

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

PIC18F24/25Q10 Family Types

Table 1. Devices included in this data sheet

Device	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	I/O Pins	16-bit Timers	Comparators	10-bit ADC^2 with Computation (ch)	5-bit DAC	Zero-Cross Detect	CCP/10-bit PWM	CWG	CLC	Low Voltage Detect (LVD)	8-bit TMR with HLT	Windowed Watchdog Timer	CRC with Memory Scan	EUSART	I^{2}C/SPI	PPS	Peripheral Module Disable	Temperature Indicator	Debug(1)
PIC18F24Q10	16k	1024	256	25	4	2	24	1	1	2/2	1	0	1	3	Y	Y	1	1	Y	Y	Y	I
PIC18F25Q10	32k	2048	256	25	4	2	24	1	1	2/2	1	0	1	3	Y	Y	1	1	Y	Y	Y	I

Table 2. Devices not included in this data sheet

Device	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	I/O Pins	16-bit Timers	Comparators	10-bit ADC^2 with Computation (ch)	5-bit DAC	Zero-Cross Detect	CCP/10-bit PWM	CWG	CLC	Low Voltage Detect (LVD)	8-bit TMR with HLT	Windowed Watchdog Timer	CRC with Memory Scan	EUSART	I^{2}C/SPI	PPS	Peripheral Module Disable	Temperature Indicator	Debug(1)
PIC18F26Q10	64k	3615	1024	25	4	2	24	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18F27Q10	128k	3615	1024	25	4	2	24	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18F45Q10	32k	2048	256	36	4	2	35	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18F46Q10	64k	3615	1024	36	4	2	35	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18F47Q10	128k	3615	1024	36	4	2	35	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I

Note: Debugging Methods: (I) – Integrated on Chip.

Data Sheet Index:

1. DS40001996 Data Sheet, 28/40-Pin, 8-bit Flash Microcontrollers
2. DS(TBD) Data Sheet, 28/40-Pin, 8-bit Flash Microcontrollers

3.7.5 CONFIG5

Name: CONFIG5
Address: 0x300008

Configuration Word 5

Code Protection

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							$\overline{CPD}$	$\overline{CP}$
Access							RO	RO
Reset							1	1

Bit 1 – $\overline{CPD}$ Data NVM (DFM) Memory Code Protection bit

Value	Description
1	Data NVM code protection disabled
0	Data NVM code protection enabled

Bit 0 – $\overline{CP}$ User NVM Program Memory Code Protection bit

Value	Description
1	User NVM code protection disabled
0	User NVM code protection enabled

5. Reference Clock Output Module

The reference clock output module provides the ability to send a clock signal to the clock reference output pin (CLKR). The reference clock output can also be routed internally as a signal for other peripherals, such as the Data Signal Modulator (DSM), Memory Scanner, and Timer module.

The reference clock output module has the following features:

- Selectable Clock Source Using the CLKRCLK Register
- Programmable Clock Divider
- Selectable Duty Cycle

Figure 5-1. Clock Reference Block Diagram

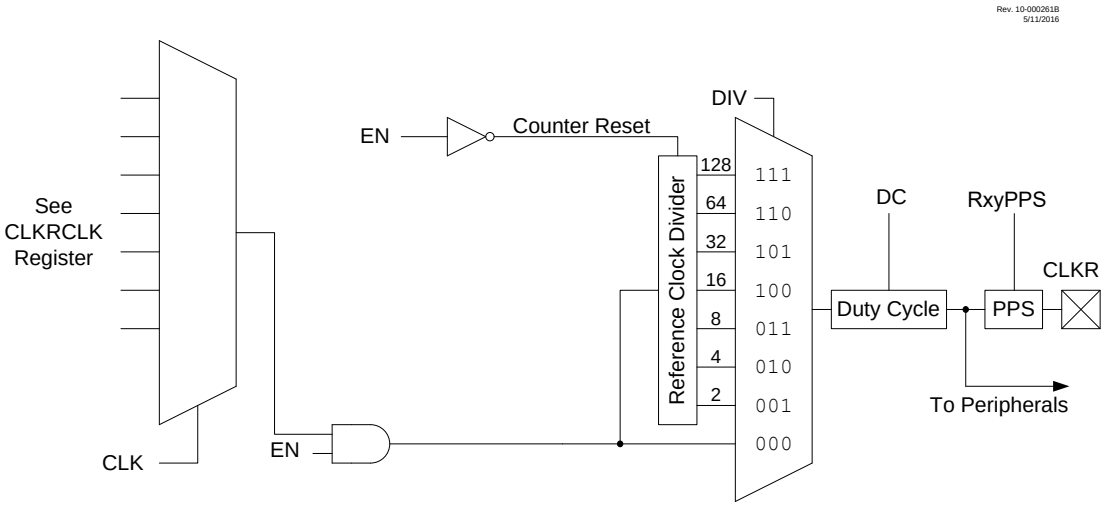
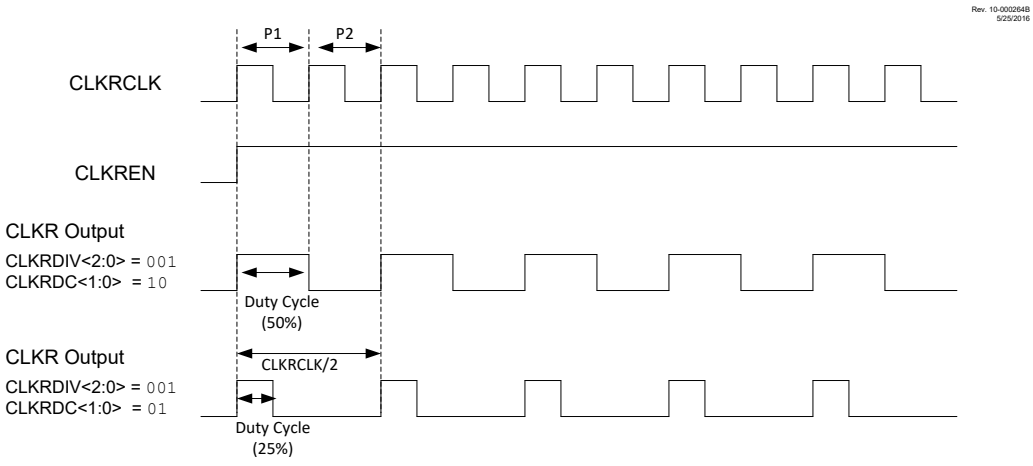


Figure 5-2. Clock Reference Timing



7.4.6 PMD5

Name: PMD5
Address: 0xEE1

PMD Control Register 5

Bit	7	6	5	4	3	2	1	0
								DSMMD
Access								R/W
Reset								0

Bit 0 – DSMMD Disable Data Signal Modulator bit

Value	Description
1	DSM module disabled
0	DSM module enabled

14.13.9 PIR7

Name: PIR7
Address: 0xECC

Peripheral Interrupt Request (Flag) Register 7

Bit	7	6	5	4	3	2	1	0
	SCANIF	CRCIF	NVMIF					CWG1IF
Access	R/W	R/W	R/W					R/W
Reset	0	0	0					0

Bit 7 – SCANIF SCAN Interrupt Flag bit

Value	Description
1	SCAN interrupt has occurred (must be cleared in software)
0	SCAN interrupt has not occurred or has not been started

Bit 6 – CRCIF CRC Interrupt Flag bit

Value	Description
1	CRC interrupt has occurred (must be cleared in software)
0	CRC interrupt has not occurred or has not been started

Bit 5 – NVMIF NVM Interrupt Flag bit

Value	Description
1	NVM interrupt has occurred (must be cleared in software)
0	NVM interrupt has not occurred or has not been started

Bit 0 – CWG1IF CWG Interrupt Flag bit

Value	Description
1	CWG interrupt has occurred (must be cleared in software)
0	CWG interrupt has not occurred or has not been started

16.10.12 IOCEP

Name: IOCEP
Address: 0xF24

Interrupt-on-Change Positive Edge Register

Bit	7	6	5	4	3	2	1	0
					IOCEP3			
Access					R/W			
Reset					0			

Bit 3 – IOCEP3 Interrupt-on-Change Positive Edge Enable bit(1)

Value	Description
1	Interrupt-on-Change enabled on the IOCE pin for a positive-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin.

Note:

1. If MCLRE = 1 or LVP = 1, RE3 port functionality is disabled and IOC on RE3 is not available.

20.1.3 Monostable Mode

Monostable modes are similar to One-Shot modes except that the ON bit is not cleared and the timer can be restarted by an external Reset event.

20.2 Timer2 Output

The Timer2 module's primary output is TMR2_postscaled, which pulses for a single TMR2_clk period upon each match of the postscaler counter and the OUTPS bits of the T2CON register. The postscaler is incremented each time the T2TMR value matches the T2PR value. This signal can be selected as an input to several other input modules:

- The ADC module, as an auto-conversion trigger
- CWG, as an auto-shutdown source
- The CRC memory scanner, as a trigger for triggered mode
- Gate source for odd numbered timers (Timer1, Timer3, etc.)
- Alternate SPI clock
- Reset signals for other instances of even numbered timers (Timer2, Timer4, etc.)

In addition, the Timer2 is also used by the CCP module for pulse generation in PWM mode. See *"PWM Overview"* and *"Pulse-width Modulation"* sections for more details on setting up Timer2 for use with the CCP and PWM modules.

Related Links

21.4 PWM Overview

22. (PWM) Pulse-Width Modulation

20.3 External Reset Sources

In addition to the clock source, the Timer2 also takes in an external Reset source. This external Reset source is selected for each timer with the corresponding TxRST register. This source can control starting and stopping of the timer, as well as resetting the timer, depending on which mode the timer is in. Reset source selections are shown in the following table.

Table 20-2. External Reset Sources

RSEL<3:0>	Reset Source		
	TMR2	TMR4	TMR6
1011-1111	Reserved	Reserved	Reserved
1010	ZCD_OUT	ZCD_OUT	ZCD_OUT
1001	CMP2OUT	CMP2OUT	CMP2OUT
1000	CMP1OUT	CMP1OUT	CMP1OUT
0111	PWM4OUT	PWM4OUT	PWM4OUT
0110	PWM3OUT	PWM3OUT	PWM3OUT
0101	CCP2OUT	CCP2OUT	CCP2OUT
0100	CCP1OUT	CCP1OUT	CCP1OUT

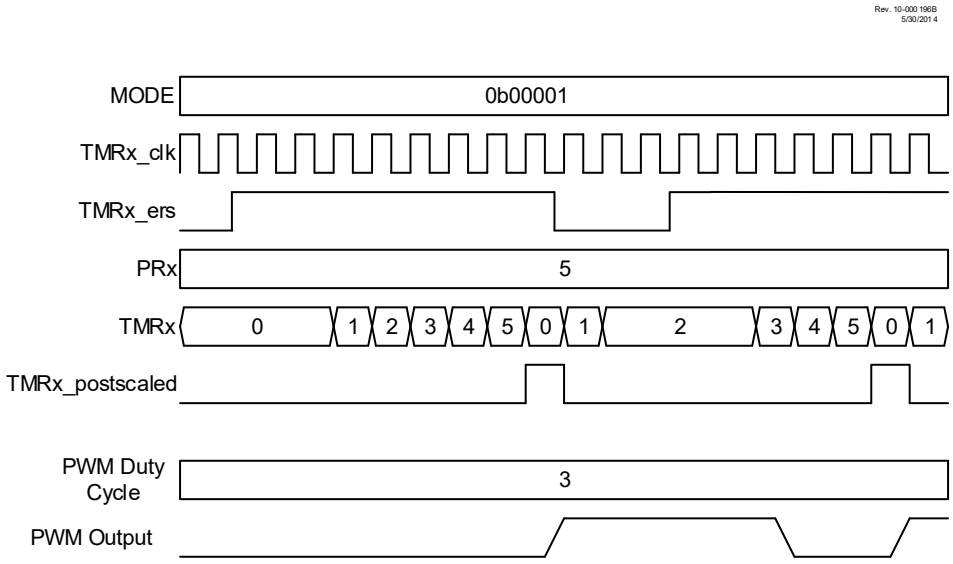
20.6.2 Hardware Gate Mode

The Hardware Gate modes operate the same as the Software Gate mode except the TMRx_ers external signal can also gate the timer. When used with the CCP, the gating extends the PWM period. If the timer is stopped when the PWM output is high, then the duty cycle is also extended.

When MODE<4:0> = 00001 then the timer is stopped when the external signal is high. When MODE<4:0> = 00010, then the timer is stopped when the external signal is low.

Figure 20-4 illustrates the Hardware Gating mode for MODE<4:0> = 00001 in which a high input level starts the counter.

Figure 20-4. Hardware Gate Mode Timing Diagram (MODE = 00001)



Related Links

21.4 PWM Overview

22. (PWM) Pulse-Width Modulation

20.6.3 Edge-Triggered Hardware Limit Mode

In Hardware Limit mode, the timer can be reset by the TMRx_ers external signal before the timer reaches the period count. Three types of Resets are possible:

- Reset on rising or falling edge (MODE<4:0>= 00011)
- Reset on rising edge (MODE<4:0> = 00100)
- Reset on falling edge (MODE<4:0> = 00101)

When the timer is used in conjunction with the CCP in PWM mode then an early Reset shortens the period and restarts the PWM pulse after a two clock delay. Refer to Figure 20-5.

20.9.5 TxCLKCON

Name: TxCLKCON
Address: 0xFBE,0xFB8,0xFB2

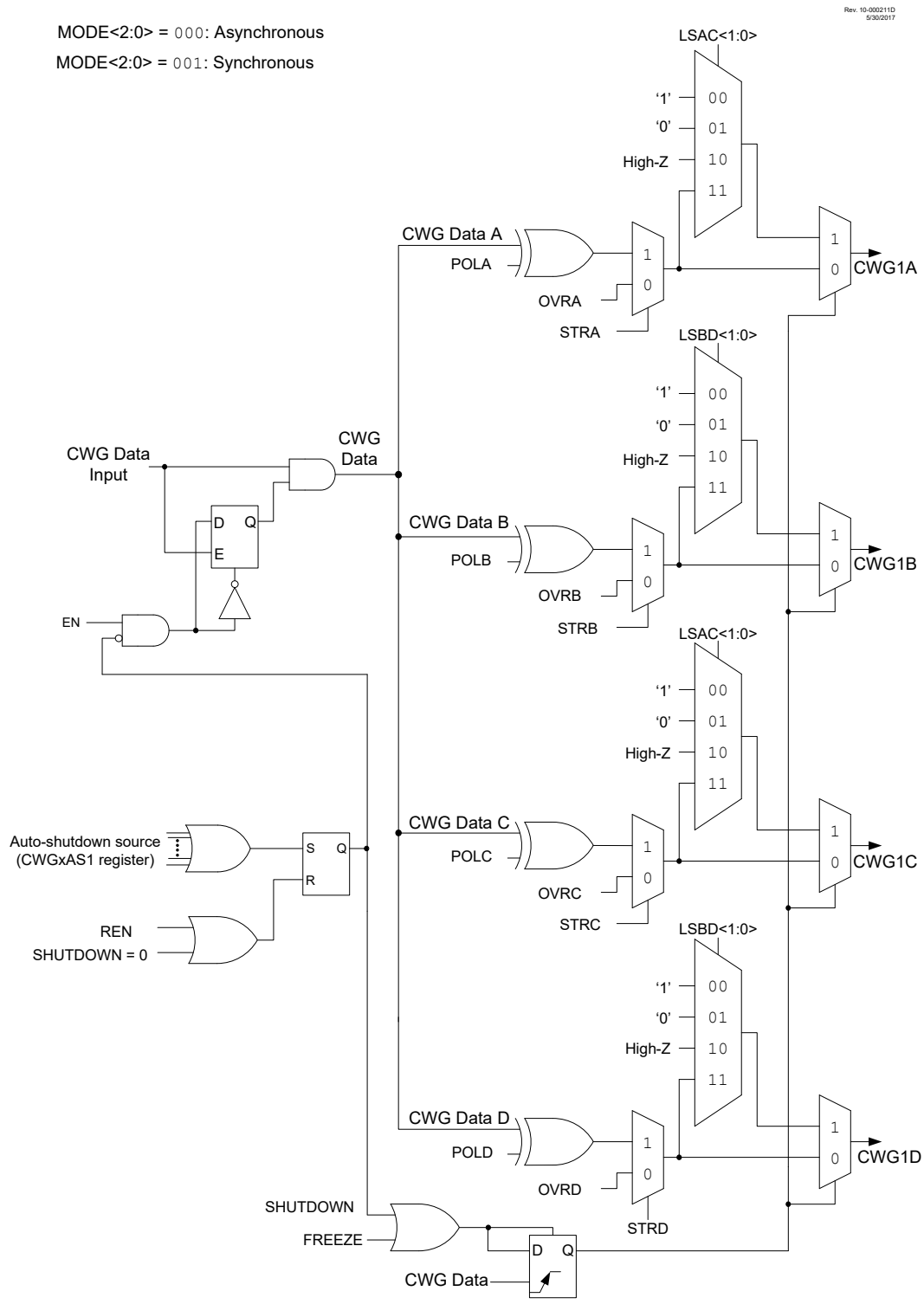
Timer Clock Source Selection Register

Bit	7	6	5	4	3	2	1	0
					CS[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – CS[3:0] Timer Clock Source Selection bits

Value	Description
n	See Clock Source Selection table

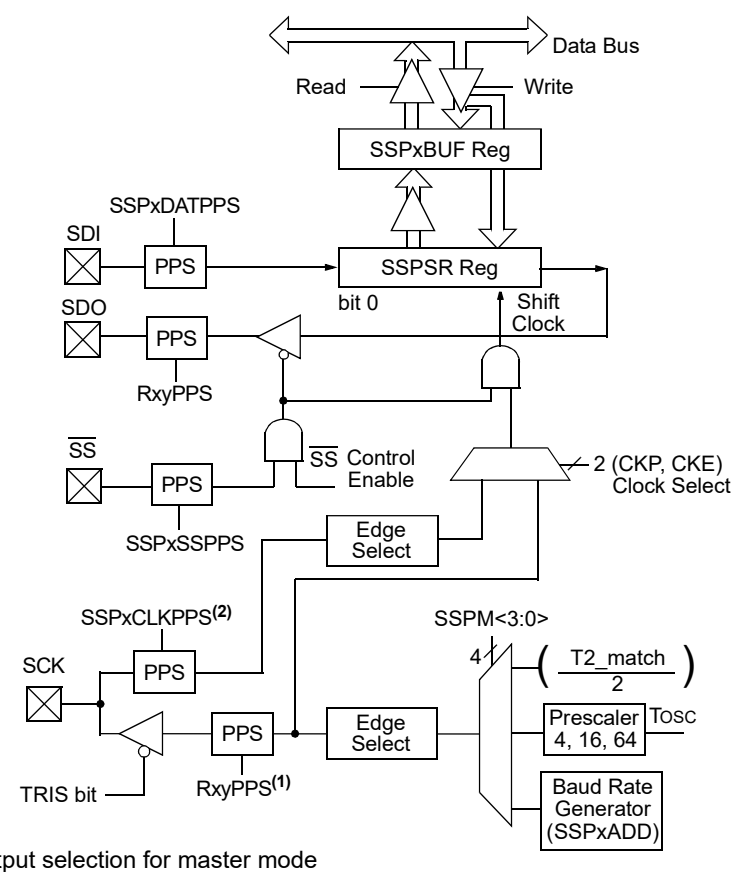
Figure 24-9. Simplified CWG Block Diagram (Output Steering Modes)



For example, when STRA = 0 then the corresponding pin is held at the level defined by OVRA. When STRA = 1, then the pin is driven by the modulated input signal.

The POLy bits control the signal polarity only when STRy = 1.

Figure 26-1. MSSP Block Diagram (SPI mode)



Note 1: Output selection for master mode

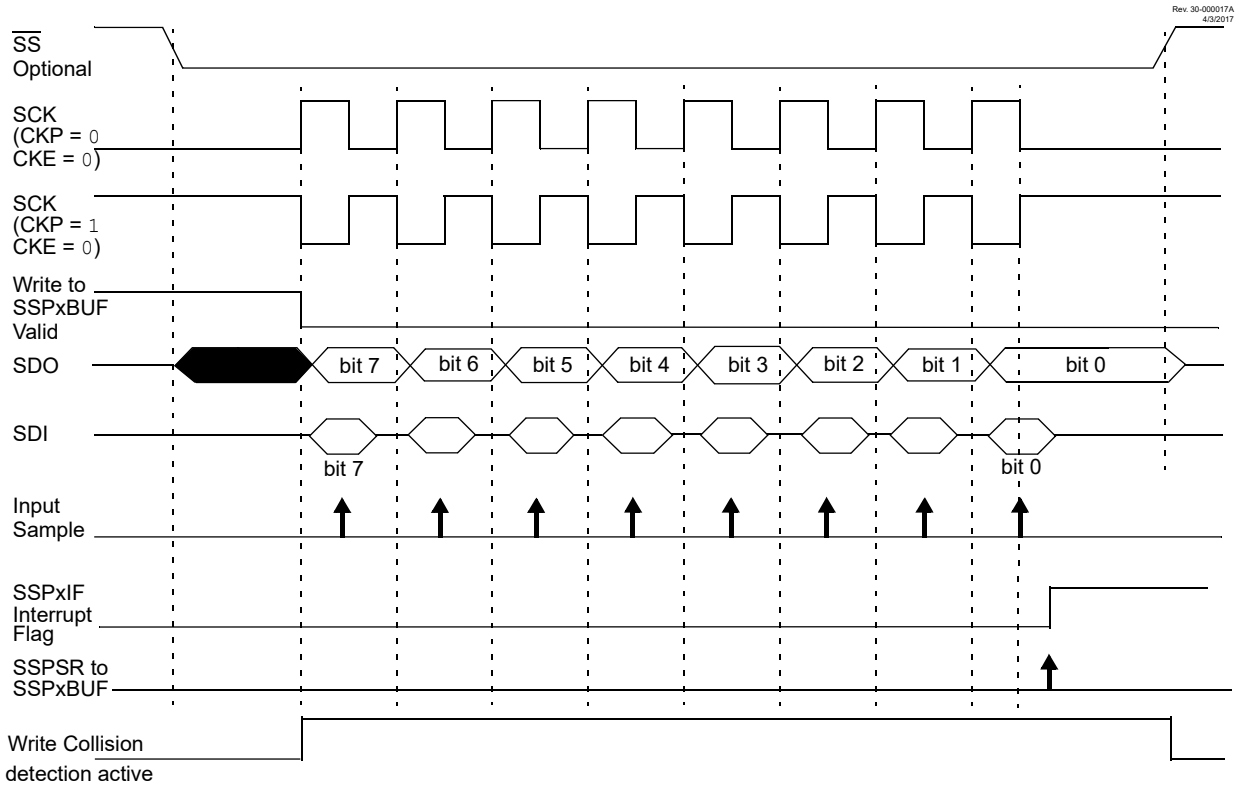
2: Input selection for slave and master mode

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

The figure below shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Figure 26-7. SPI Mode Waveform (Slave Mode with CKE = 0)



26.6.1 I²C Master Mode Operation

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the 26.9.1.6 R/W bit. In this case, the 26.9.1.6 R/W bit will be logic '0'. Serial data is transmitted eight bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

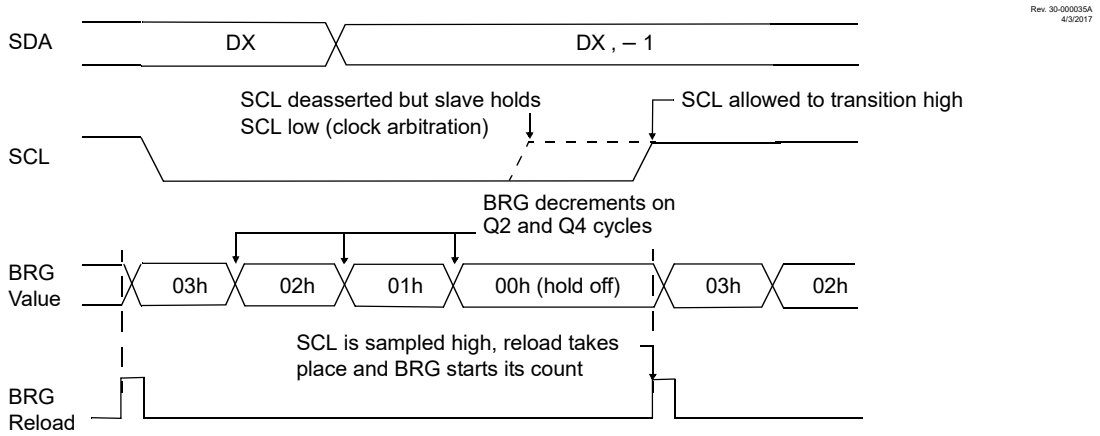
In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/$\overline{W}$ bit. In this case, the R/$\overline{W}$ bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received eight bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

A Baud Rate Generator is used to set the clock frequency output on SCL. See 26.7 Baud Rate Generator for more detail.

26.6.2 Clock Arbitration

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of 26.9.6 SSPxADD and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device as shown in the following figure.

Figure 26-25. Baud Rate Generator Timing with Clock Arbitration



26.6.3 WCOL Status Flag

If the user writes the SSPxBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the 26.9.2.1 WCOL bit is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPxBUF was attempted while the module was not idle.

26.9.3 SSPxCON2

Name: SSPxCON2
Address: 0x0F96

Control Register for I²C Operation Only

MSSP Control Register 2

Bit	7	6	5	4	3	2	1	0
	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
Access	R/W	R/W/HC	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – GCEN
General Call Enable bit (Slave mode only)

Value	Mode	Description
x	Master mode	Don't care
1	Slave mode	General call is enabled
0	Slave mode	General call is not enabled

Bit 6 – ACKSTAT Acknowledge Status bit (Master Transmit mode only)

Value	Description
1	Acknowledge was not received from slave
0	Acknowledge was received from slave

Bit 5 – ACKDT
Acknowledge Data bit (Master Receive mode only)**(1)**

Value	Description
1	Not Acknowledge
0	Acknowledge

Bit 4 – ACKEN
Acknowledge Sequence Enable bit**(2)**

Value	Description
1	Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; automatically cleared by hardware
0	Acknowledge sequence is Idle

Bit 3 – RCEN
Receive Enable bit (Master Receive mode only)**(2)**

Value	Description
1	Enables Receive mode for I²C
0	Receive is Idle

Bit 2 – PEN
Stop Condition Enable bit (Master mode only)**(2)**

- The mode of the CALL or RETURN instructions (specified by ‘s’)
- The mode of the table read and table write instructions (specified by ‘m’)
- No operand required (specified by ‘—’)

All instructions are a single word, except for four double-word instructions. These instructions were made double-word to contain the required information in 32 bits. In the second word, the four MSbs are ‘1’s. If this second word is executed as an instruction (by itself), it will execute as a NOP.

All single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP.

The double-word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true, or the Program Counter is changed as a result of an instruction, the instruction execution time is 2 µs. Two-word branch instructions (if true) would take 3 µs.

Figure 36-1 shows the general formats that the instructions can have. All examples use the convention ‘nnh’ to represent a hexadecimal number.

The Instruction Set Summary, shown in Table 36-2, lists the standard instructions recognized by the Microchip Assembler (MPASM™).

36.1.1 Standard Instruction Set
provides a description of each instruction.

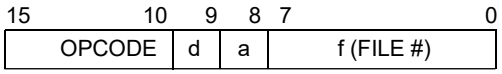
Table 36-1. Opcode Field Descriptions

Field	Description
a	RAM access bit a = 0: RAM location in Access RAM (BSR register is ignored) a = 1: RAM bank is specified by BSR register
bbb	Bit address within an 8-bit file register (0 to 7).
BSR	Bank Select Register. Used to select the current RAM bank.
C, DC, Z, OV, N	ALU Status bits: Carry, Digit Carry, Zero, Overflow, Negative.
d	Destination select bit d = 0: store result in WREG d = 1: store result in file register f
dest	Destination: either the WREG register or the specified register file location.
f	8-bit Register file address (00h to FFh) or 2-bit FSR designator (0h to 3h).
f_s	12-bit Register file address (000h to FFFh). This is the source address.

Figure 36-1. General Format for Instructions

Byte-oriented file register operations

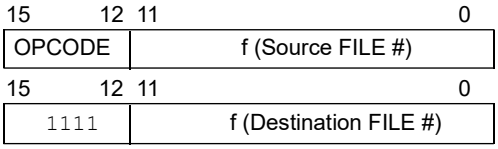
Example Instruction




```
ADDWF MYREG, W, B
```

d = 0 for result destination to be WREG register
d = 1 for result destination to be file register (f)
a = 0 to force Access Bank
a = 1 for BSR to select bank
f = 8-bit file register address

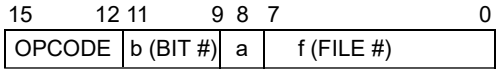
Byte to Byte move operations (2-word)




```
MOVFF MYREG1, MYREG2
```

f = 12-bit file register address

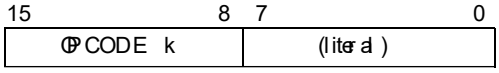
Bit-oriented file register operations




```
BSF MYREG, bit, B
```

b = 3-bit position of bit in file register (f)
a = 0 to force Access Bank
a = 1 for BSR to select bank
f = 8-bit file register address

Literal operations

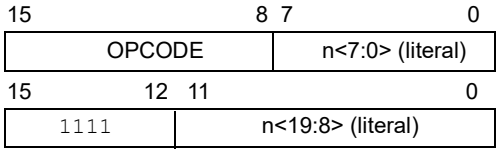



```
MOVLW 7Fh
```

k = 8-bit immediate value

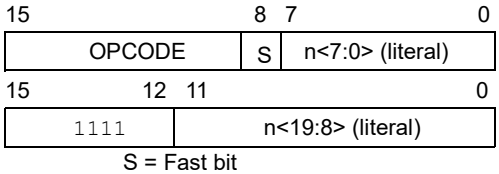
Control operations

CALL, GOTO and Branch operations



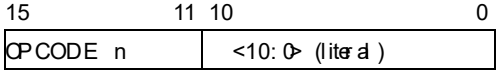

```
GOTO Label
```

n = 20-bit immediate value

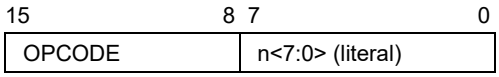



```
CALL MYFUNC
```

S = Fast bit




```
BRA MYFUNC
```




```
BC MYFUNC
```

Example:	HERE	BC	5
Before Instruction PC = address (HERE) After Instruction If CARRY = 1; PC = address (HERE + 12) If CARRY = 0; PC = address (HERE + 2)			

BCF	Bit Clear f			
Syntax:	BCF f, b {,a}			
Operands:	0 ≤ f ≤ 255 0 ≤ b ≤ 7 a ∈ [0,1]			
Operation:	0 → f<b>			
Status Affected:	None			
Encoding:	1001	bbba	ffff	ffff
Description:	Bit ‘b’ in register ‘f’ is cleared. If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank. If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See 36.2.3 Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode for details.			
Words:	1			
Cycles:	1			

Q Cycle Activity:			
Q1	Q2	Q3	Q4
Decode	Read register ‘f’	Process Data	Write register ‘f’

Example:	BCF	FLAG_REG, 7, 0
Before Instruction FLAG_REG = C7h After Instruction		

If NEGATIVE = 0; PC = address (HERE + 2)

BNC	Branch if Not Carry			
Syntax:	BNC n			
Operands:	-128 ≤ n ≤ 127			
Operation:	if CARRY bit is ‘0’ (PC) + 2 + 2n → PC			
Status Affected:	None			
Encoding:	1110	0011	nnnn	nnnn
Description:	If the CARRY bit is ‘0’, then the program will branch. The 2’s complement number ‘2n’ is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.			
Words:	1			
Cycles:	1(2)			

Q Cycle Activity: If Jump:			
Q1	Q2	Q3	Q4
Decode	Read literal ‘n’	Process Data	Write to PC
No operation	No operation	No operation	No operation
If No Jump:			
Q1	Q2	Q3	Q4
Decode	Read literal ‘n’	Process Data	No operation

Example:	HERE	BNC	Jump
Before Instruction PC = address (HERE) After Instruction If CARRY = 0; PC = address (Jump)			

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Characteristic	Min.	Typ. †	Max.	Units	Conditions
OS56	$T_{LFOSCST}$	LFINTOSC Wake-up from Sleep Start-up Time	—	0.2	—	ms	

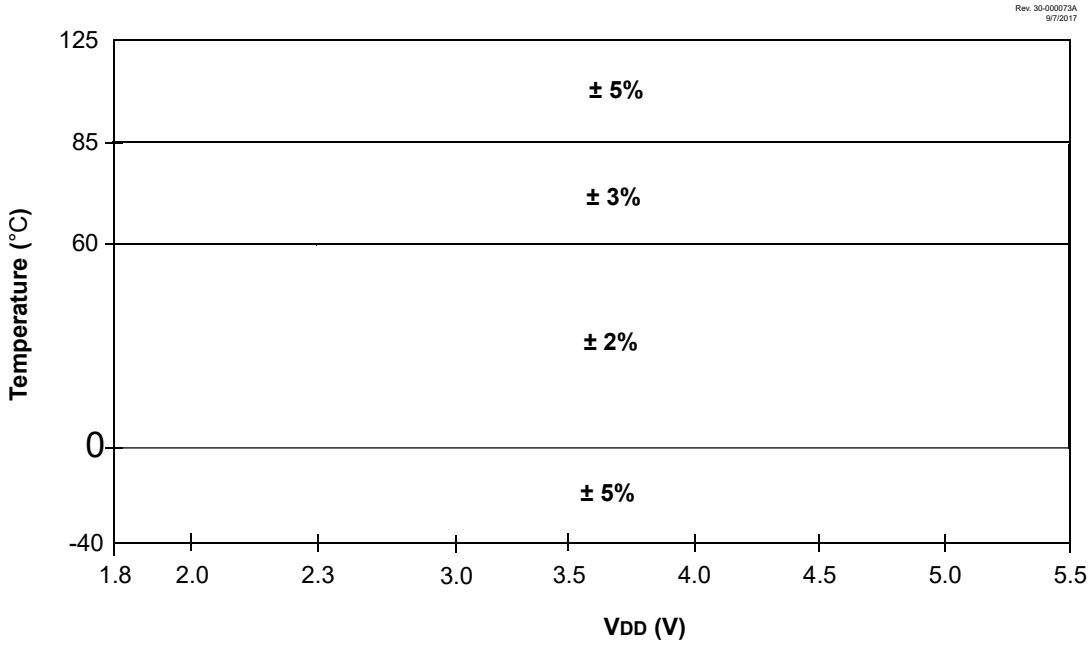
* - These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

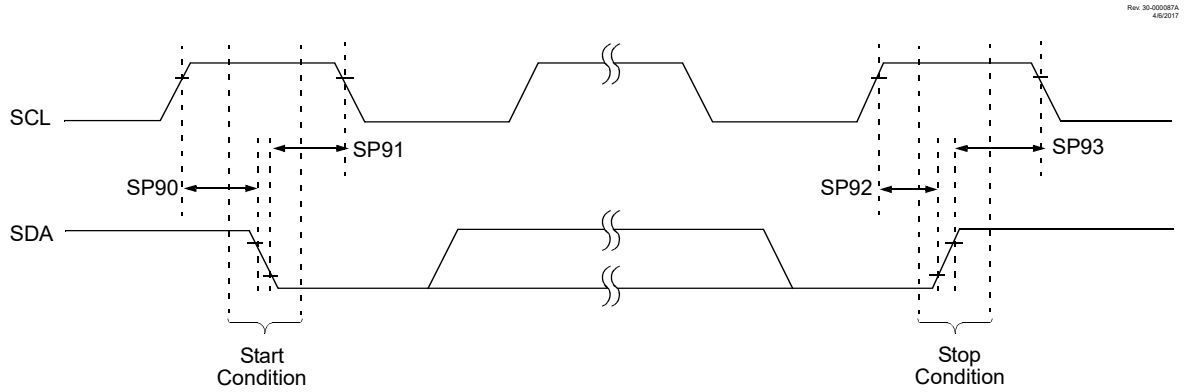
1. To ensure these oscillator frequency tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.
2. See the figure below.

Figure 38-5. Precision Calibrated HFINTOSC Frequency Accuracy Over Device V_{DD} and Temperature



Standard Operating Conditions (unless otherwise stated)								
Param. No.	Sym.	Characteristic		Min.	Typ. †	Max.	Units	Conditions
			400 kHz mode	600	—	—		
* - These parameters are characterized but not tested.								

Figure 38-19. I²C Bus Start/Stop Bits Timing



Note: Refer to Figure 38-3 for load conditions.

38.4.19 I²C Bus Data Requirements

Table 38-25.

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic		Min.	Max.	Units	Conditions
SP100*	T_{HIGH}	Clock high time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	$1.5T_{CY}$	—		
SP101*	T_{LOW}	Clock low time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz