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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36074gfzwv

Table 3.5 SFR Information (5) (1)

Address	Register Name	Symbol	After Reset
00100h			
00101h			
00102h			
00103h			
00104h			
00105h			
00106h			
00107h			
00108h			
00109h			
0010Ah			
0010Bh			
0010Ch			
0010Dh			
0010Eh			
0010Fh			
00110h			
00111h			
00112h			
00113h			
00114h			
00115h			
00116h			
00117h			
00118h			
00119h			
0011Ah			
0011Bh			
0011Ch			
0011Dh			
0011Eh			
0011Fh			
00120h			
00121h			
00122h			
00123h			
00124h			
00125h			
00126h			
00127h			
00128h			
00129h			
0012Ah			
0012Bh			
0012Ch			
0012Dh			
0012Eh			
0012Fh			
00130h			
00131h			
00132h			
00133h			
00134h			
00135h			
00136h			
00137h			
00138h			
00139h			
0013Ah			
0013Bh			
0013Ch			
0013Dh			
0013Eh			
0013Fh			

Note:
1. The blank areas are reserved. No access is allowed.

8.2 Registers

Table 8.2 lists the Watchdog Timer Register Configuration.

Table 8.2 Watchdog Timer Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Watchdog Timer Function Register	RISR	(Note 1)	00030h	8
Watchdog Timer Reset Register	WDTR	XXh	00031h	8
Watchdog Timer Start Register	WDTS	XXh	00032h	8
Watchdog Timer Control Register	WDTC	01XXXXXXb	00033h	8
Count Source Protection Mode Register	CSPR	(Note 1)	00034h	8
Periodic Timer Interrupt Control Register	WDTIR	00h	00035h	8

Note:
1. See the description of the individual registers.

8.2.1 Watchdog Timer Function Register (RISR)

Address 00030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RIS	UFIF	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 0.							
After Reset	0	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	UFIF	WDT underflow detection flag	0: No watchdog timer underflow 1: Watchdog timer underflow (1)	R/W
b7	RIS	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (2)	R/W

Notes:
1. After reading this bit as 1, wait at least one cycle of the count source before writing 0 to it.
2. The RIS bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.
   When the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), the RIS bit is automatically set to 1.

   Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the RISR register.

UFIF Bit (WDT underflow detection flag)

[Condition for setting to 0]
• When 0 is written to this bit.
[Conditions for setting to 1]
• When the watchdog timer underflows while the RIS bit is 0 (watchdog timer interrupt).
• When a refresh is executed during the period other than the acceptance period (illegal refresh) while the RIS bit is 0 (watchdog timer interrupt).

11.9.5 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) When Returning from Wait Mode or Stop Mode to Standard Mode

When a transition is made to wait mode or stop mode with the WCKSTP bit in the CKSTPR register set to 1 (system clock stopped in wait mode) while in use of the $\overline{\text{INTi}}$ input filter, the $\overline{\text{INTi}}$ interrupt cannot be used to return to standard operating mode.

When the $\overline{\text{INTi}}$ interrupt is used to return, set the WCKSTP bit to 1 and bits INTiF1 to INTiF0 in the INTF0 register to 00b (no filter) before a transition is made to wait mode or stop mode. When the $\overline{\text{INTi}}$ input filter is used again, select the sampling clock with bits INTiF0 to INTiF1 to enable the INTiEN bit in the INTEN register.

Figure 11.14 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used.

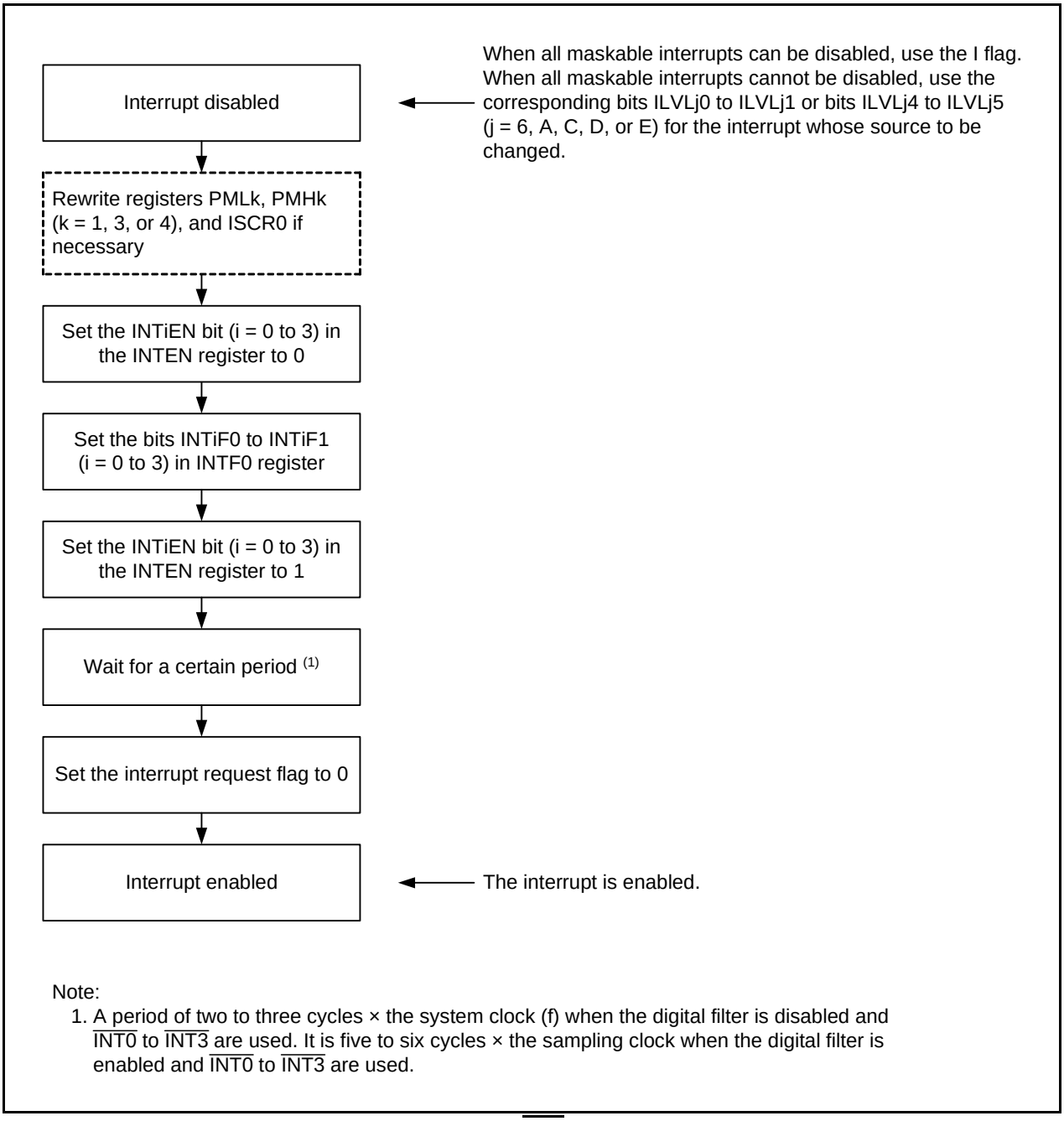


Figure 11.14 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used

11.9.7 Changing Interrupt Priority Levels and Flag Registers

(a) The interrupt priority level and the flag register must be changed only while no interrupt requests are generated. If an interrupt may be generated, using the I flag to disable the interrupt before changing the interrupt priority level and the flag register.

(b) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the interrupt priority level and the flag register are changed due to effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instruction to separate the interrupt priority level and the flag register operation, and I flag operation.

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #0CFH, ILVLE    ; Set INT0 interrupt priority level 0
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #0CFH, ILVLE    ; Set INT0 interrupt priority level 0
    MOV.W   MEM, R0         ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #0CFH, ILVLE    ; Set INT0 interrupt priority level 0
    POPC    FLG             ; Enable interrupts
```

12.3.1 Port P1 Direction Register (PD1)

Address 000A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD1_7	PD1_6	PD1_5	PD1_4	PD1_3	PD1_2	PD1_1	PD1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD1_0	Port P1_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PD1_1	Port P1_1 direction bit		R/W
b2	PD1_2	Port P1_2 direction bit		R/W
b3	PD1_3	Port P1_3 direction bit		R/W
b4	PD1_4	Port P1_4 direction bit		R/W
b5	PD1_5	Port P1_5 direction bit		R/W
b6	PD1_6	Port P1_6 direction bit		R/W
b7	PD1_7	Port P1_7 direction bit		R/W

The PD1 register is used to select whether I/O ports are used as input or output.
Each bit in the PD1 register corresponds to individual ports.

12.3.2 Port P1 Register (P1)

Address 000AFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P1_0	Port P1_0 bit	0: Low level 1: High level	R/W
b1	P1_1	Port P1_1 bit		R/W
b2	P1_2	Port P1_2 bit		R/W
b3	P1_3	Port P1_3 bit		R/W
b4	P1_4	Port P1_4 bit		R/W
b5	P1_5	Port P1_5 bit		R/W
b6	P1_6	Port P1_6 bit		R/W
b7	P1_7	Port P1_7 bit		R/W

The P1 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P1 register. The P1 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pins. Each bit in the P1 register corresponds to individual ports.

12.6.1 Port PA Direction Register (PDA)

Address 000ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	PDA_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDA_0	Port PA_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The PDA register is used to select whether PA_0 is used as input or output.

12.6.2 Port PA Register (PA)

Address 000B3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	PA_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PA_0	Port PA_0 bit	0: Low level 1: High level	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The PA register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the PA register. The PA register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pin.

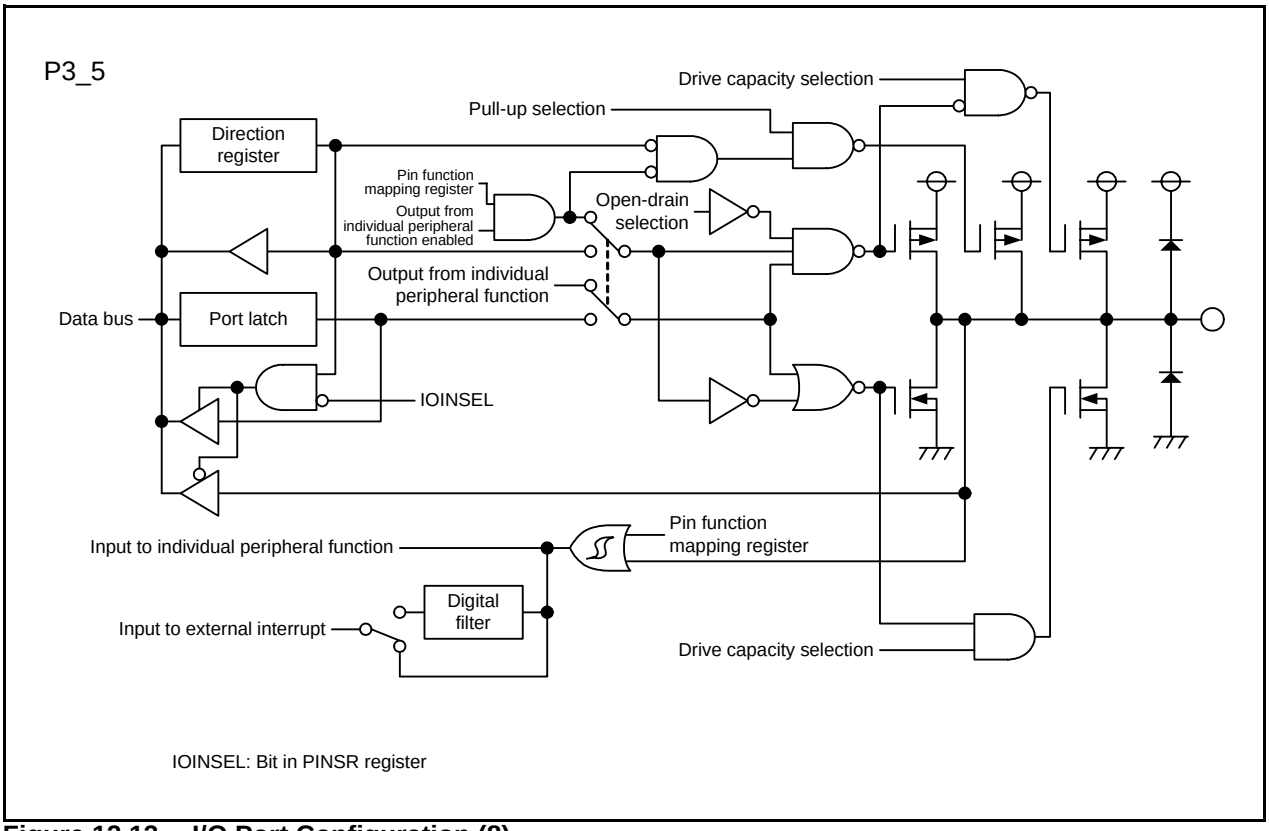


Figure 12.13 I/O Port Configuration (8)

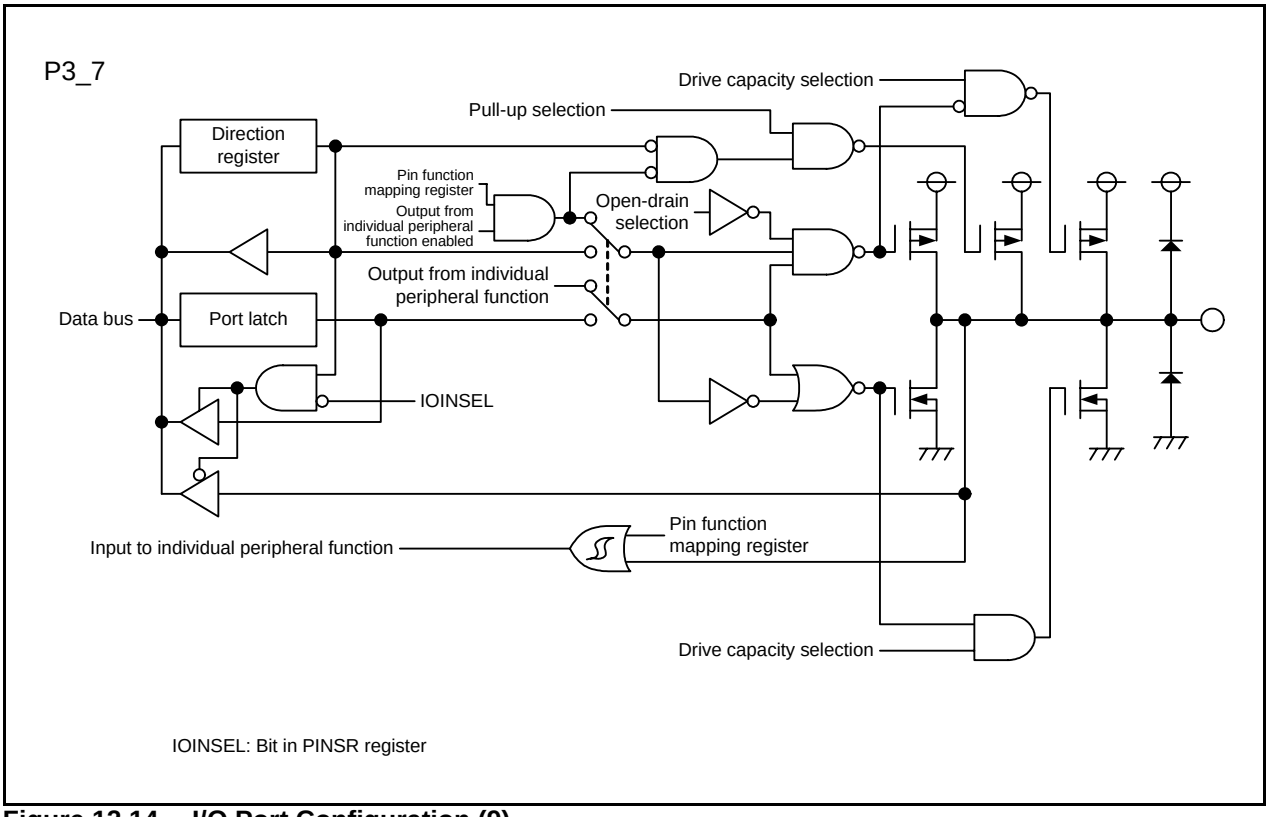


Figure 12.14 I/O Port Configuration (9)

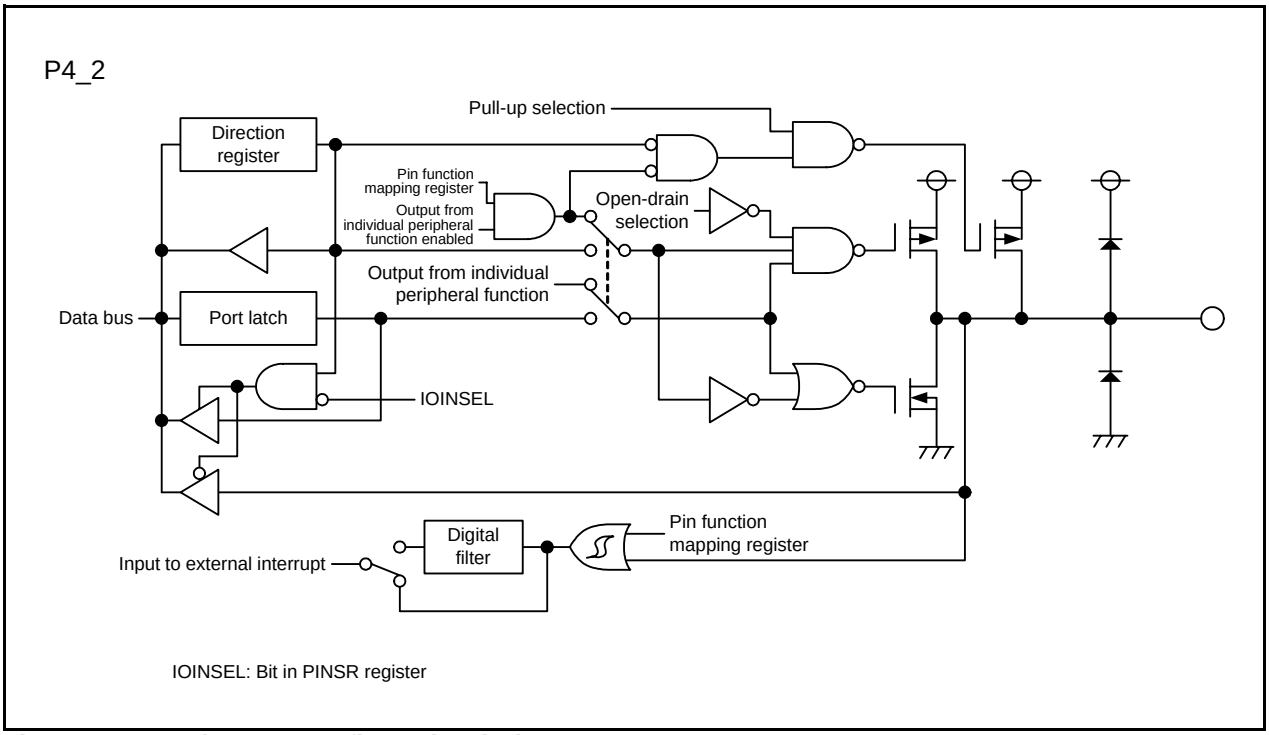


Figure 12.15 I/O Port Configuration (10)

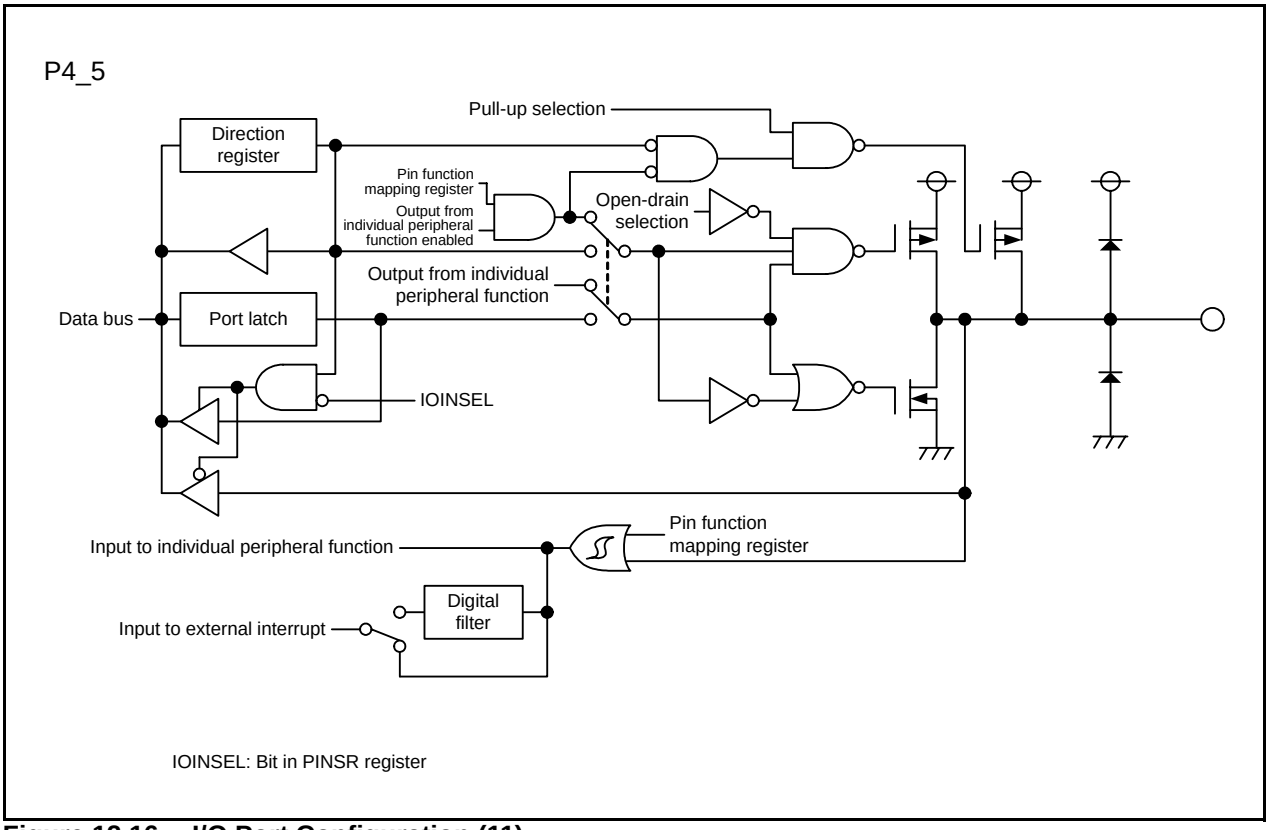


Figure 12.16 I/O Port Configuration (11)

13.4.2 Timer Mode

In this mode, the counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register.

The count value is decremented by 1 each time the count source is input, and an underflow occurs if the next count source is input after the count value reaches 0000h. The TRJIF bit in the TRJIR register is set to 1 (interrupt requested) at that time and the value set in the reload register is loaded simultaneously. When the TRJIE bit in the TRJIR register is 1 (interrupt enabled), an interrupt request signal is generated to the CPU.

Figure 13.3 shows an Operation Example in Timer Mode.

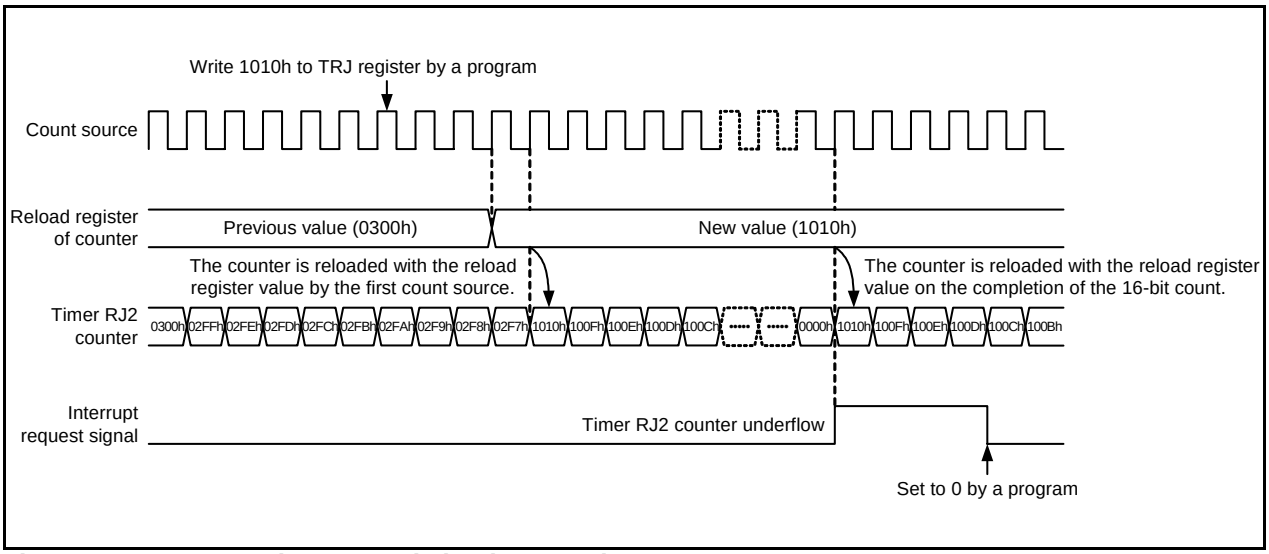
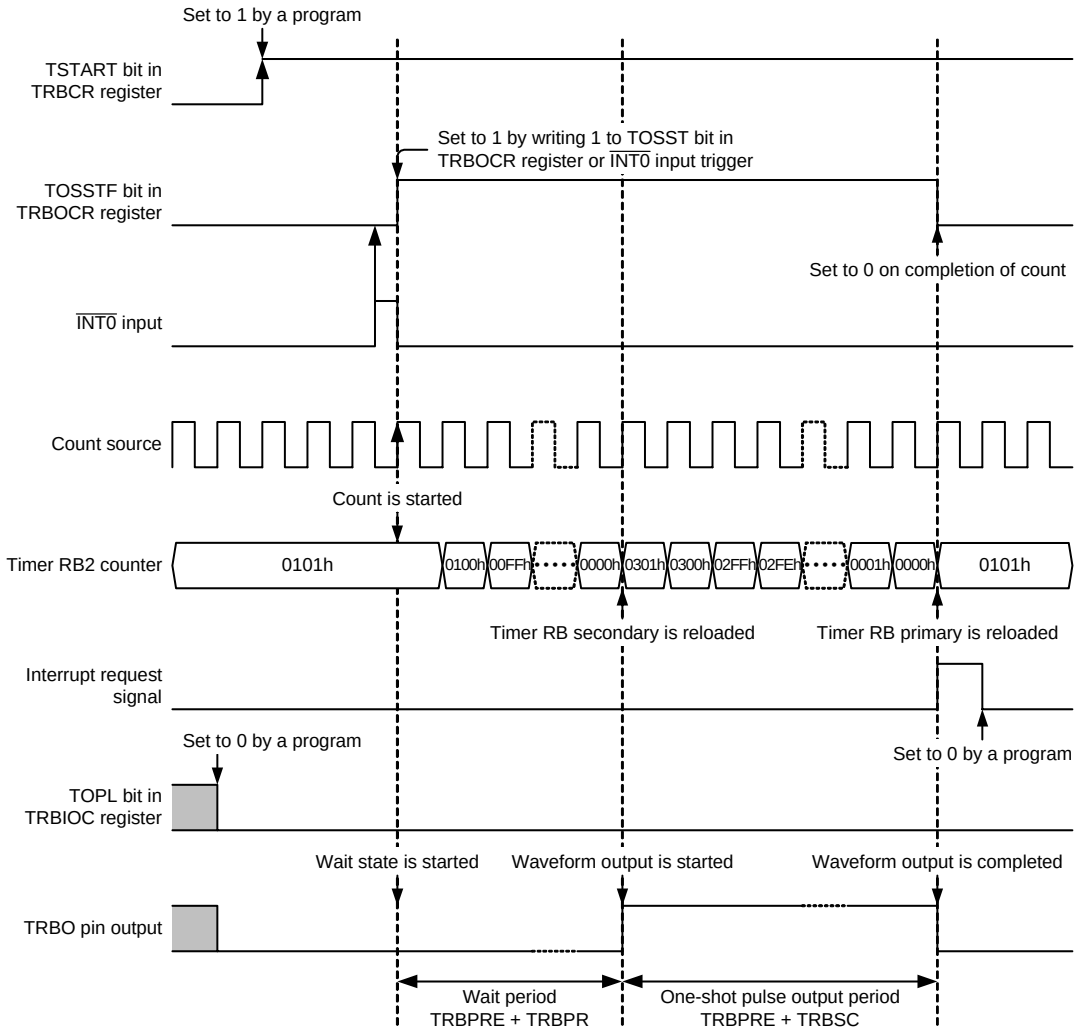


Figure 13.3 Operation Example in Timer Mode



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 03h
- TOPL bit = 0, TOCNT bit = 0 (waveform output),
  INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

Figure 14.8 Example of 16-Bit Timer Operation in Programmable Wait One-Shot Generation Mode

Figure 15.10 shows an Example of Buffer Operation in PWM Mode. In this example, the TRCIOB pin is set to PWM mode and the TRCGRD register is set as the buffer register for the TRCGRB register. The TRCCNT register is cleared by compare match A, and output is set to low at compare match A and high at compare match B.
Since buffer operation is set, the output is changed when compare match B occurs, and the value in the buffer register TRCGRD is transferred to the TRCGRB register at the same time. This operation is repeated each time compare match B occurs.

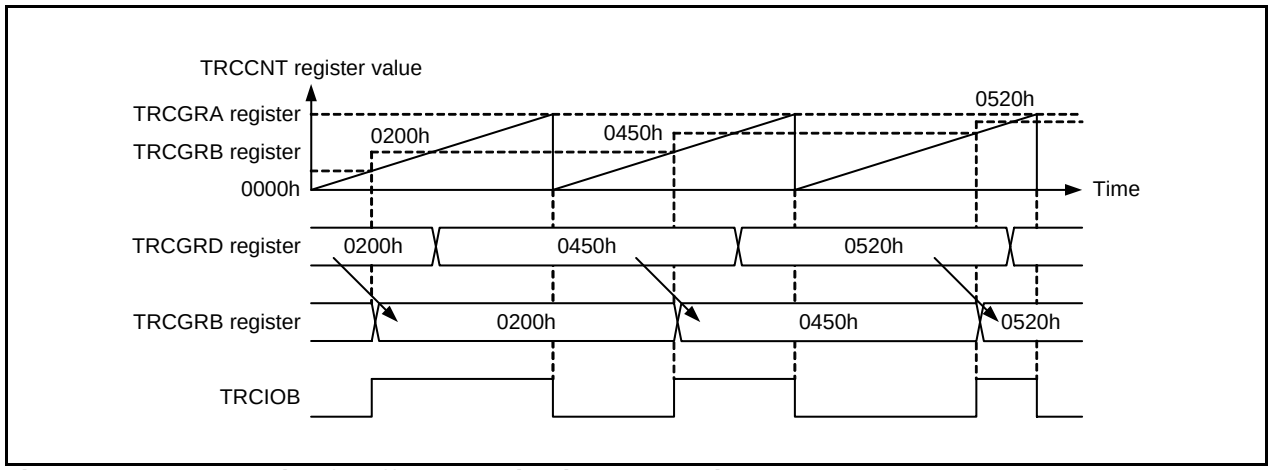
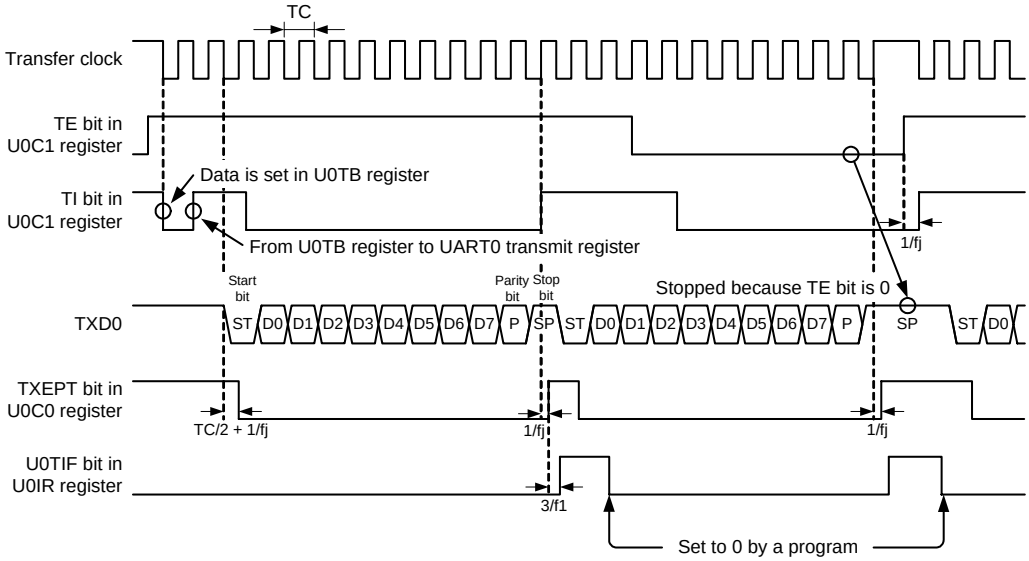


Figure 15.10 Example of Buffer Operation in PWM Mode

16.3.2.1 Operation Examples

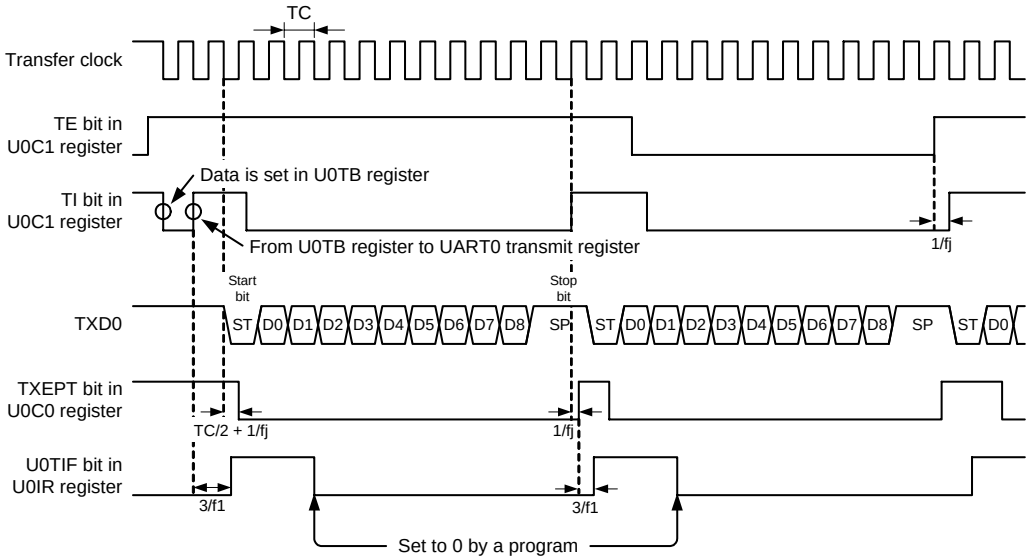
• When transfer data is 8 bits long (parity enabled, one stop bit)



The above diagram applies for the following settings:
- STPS bit in U0MR register = 0 (one stop bit)
- PRYE bit in U0MR register = 1 (parity enabled)
- U0IRS bit in U0C1 register = 1 (transmission is completed)

TC = 16 (n + 1)/fj or 16 (n + 1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, or f32)
fEXT: Frequency of U0BRG count source (external clock)
n: Value set in U0BRG register

• When transfer data is 9 bits long (parity disabled, two stop bits)



The above diagram applies for the following settings:
- STPS bit in U0MR register = 1 (two stop bits)
- PRYE bit in U0MR register = 0 (parity disabled)
- U0IRS bit in U0C1 register = 0 (transmit buffer is empty)

TC = 16 (n + 1)/fj or 16 (n + 1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, or f32)
fEXT: Frequency of U0BRG count source (external clock)
n: Value set in U0BRG register

Figure 16.6 Transmit Timing in Clock Asynchronous Serial I/O Mode

17. A/D Converter

This MCU features a 10-bit successive approximation A/D converter that can process analog inputs for up to six channels.

17.1 Overview

Table 17.1 lists the A/D Converter Specifications. Figure 17.1 shows the A/D Converter Block Diagram.

Table 17.1 A/D Converter Specifications

Item	Specification
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage	0 V to AVCC
Input channels	6 channels (AN0 to AN4, AN7)
Resolution	10 bits
A/D conversion clock	f1, f2, f4, f8, or fAD
Conversion time	2.2 μs (A/D conversion clock = 20 MHz)
A/D operating modes	• One-shot mode: A/D conversion is performed on the specified single channel for a single round. • Repeat mode: A/D conversion is performed on the specified single channel repeatedly. • Single sweep mode: A/D conversion is performed on the specified two channels for a single round. • Repeat sweep mode: A/D conversion is performed on the specified two channels repeatedly.
A/D conversion data register (× 2)	16-bit data register corresponding to each channel group where the A/D conversion result is stored (valid data length: 10 bits).
A/D conversion start conditions	• Software trigger • Conversion start trigger from timer RC • External trigger
Interrupt source	An A/D conversion interrupt is generated when A/D conversion completes.
Others	The A/D converter is set to standby by the MSTAD bit in the MSTCR register.

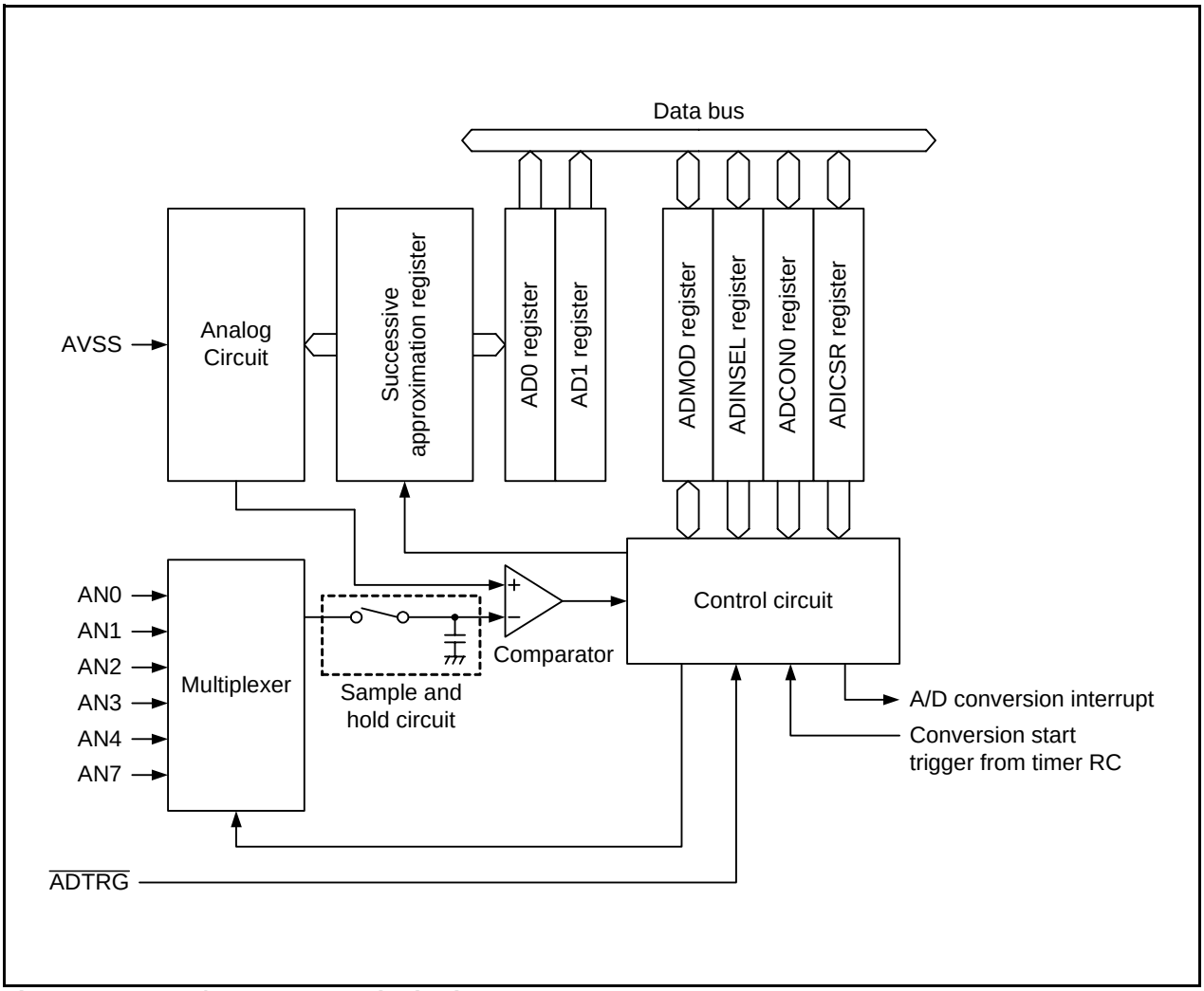


Figure 17.1 A/D Converter Block Diagram

Table 17.2 lists the A/D Converter Pin Configuration.
Pins AVCC and AVSS are used for the power supply to the analog block in the A/D converter.
The six analog input pins are divided into three channel groups.

Table 17.2 A/D Converter Pin Configuration

Pin Name	Assigned Pin	I/O	Function
AVCC	VCC	I	Power supply input for the A/D converter
AVSS	VSS	I	
AN0	P1_0	I	Analog input for channel group 0
AN1	P1_1	I	
AN2	P1_2	I	Analog input for channel group 1
AN3	P1_3	I	
AN4	P1_4	I	Analog input for channel group 2
AN7	P1_7	I	
$\overline{\text{ADTRG}}$	P3_7	I	External trigger input for starting A/D conversion

17.2.5 A/D Interrupt Control Status Register (ADICSR)

Address 0009Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADF	ADIE	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

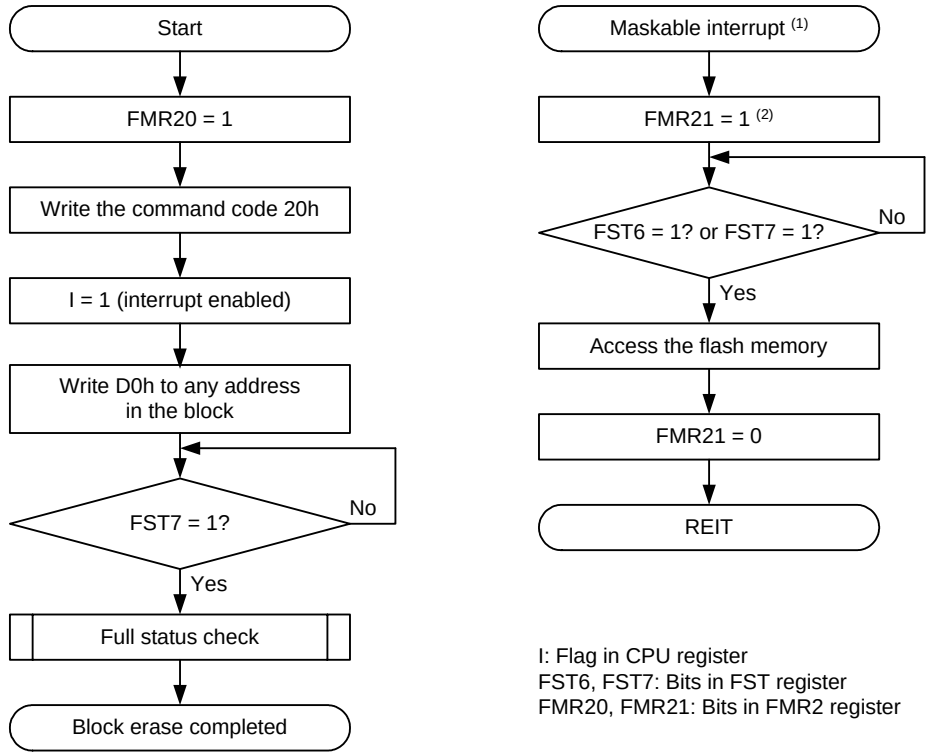
Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	ADIE	A/D conversion interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b7	ADF	A/D conversion interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)

Note:
1. Only 0 (no interrupt requested) can be written to the ADF bit.

ADF Bit (A/D conversion interrupt request bit)

This bit indicates whether an A/D conversion interrupt is requested. It also indicates whether A/D conversion has completed.

[Conditions for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Conditions for setting to 1]
• When A/D conversion is completed in one-shot mode or single sweep mode.
• When A/D conversion is completed on all the selected channels in repeat mode or repeat sweep mode.



Notes:
1. The interrupt vector table and interrupt routine to be used must be allocated to an area other than the erase-target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.

Figure 19.13 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

(8) When the TEDGSEL bit in the TRJIOC register is set to 0 (count on rising edge) and the external signal (TRJIO) is counted in event counter mode, the signal may not be counted correctly depending on the state of the TSTART bit in the TRJCR register (see Figure 21.4).
If the TRJIO pin is set to low before the TSTART bit is set to 1 (count is started) and a valid event is input after the TSTART bit is set to 1, the signal is not counted on the first rising edge of the TRJIO input.
Thus, the number of counted events is obtained as follows:
Number of counted events = {(initial value in the counter – value in the counter on completion of the valid event + 1) + 1}
To avoid this, set the TRJIO pin to low after setting the TSTART bit to 1 (count is started) (see Figure 21.5).

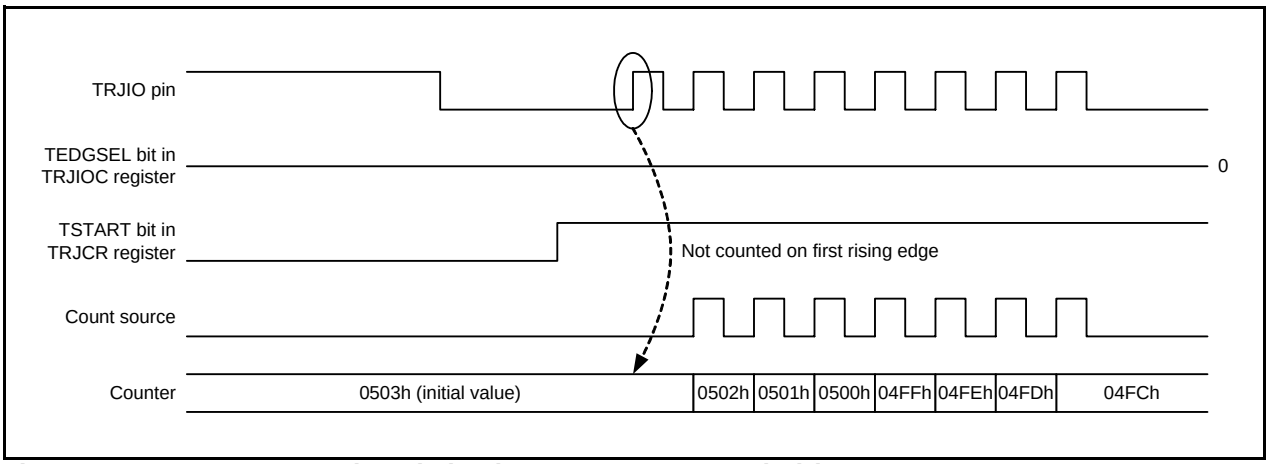


Figure 21.4 TSTART Setting Timing in Event Counter Mode (1)

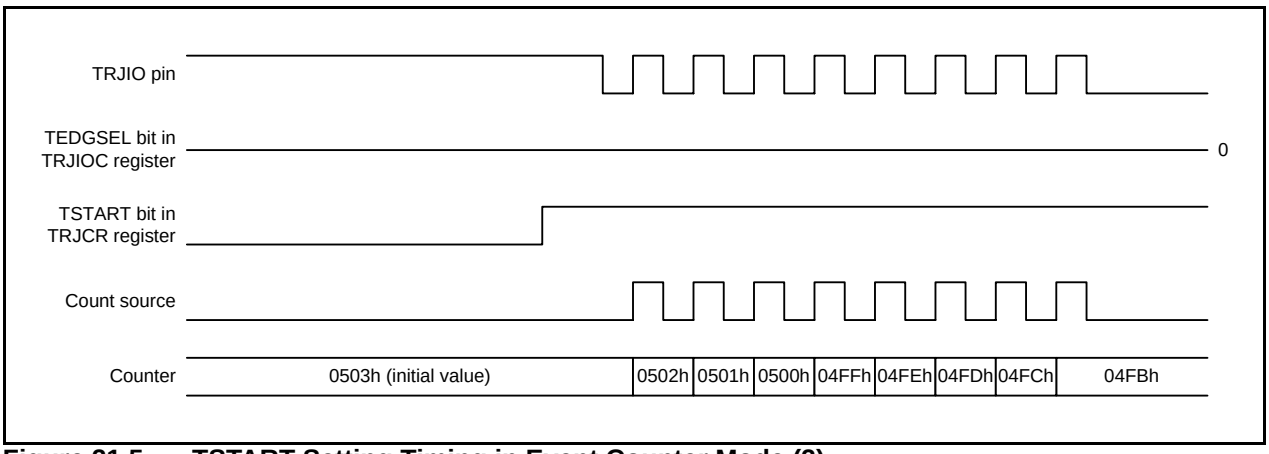


Figure 21.5 TSTART Setting Timing in Event Counter Mode (2)

R8C/M11A Group, R8C/M12A Group User's Manual: Hardware

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