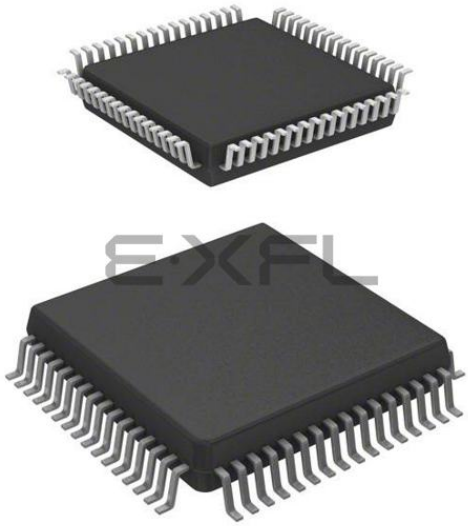

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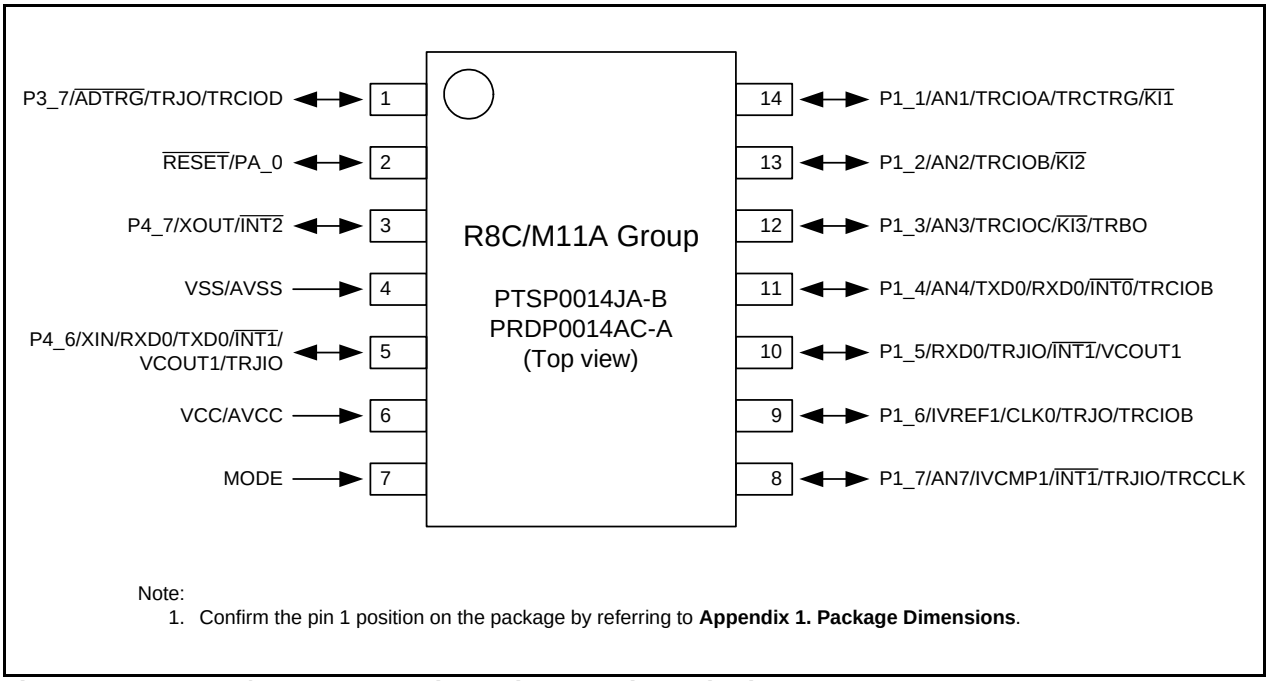
Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36074ghv

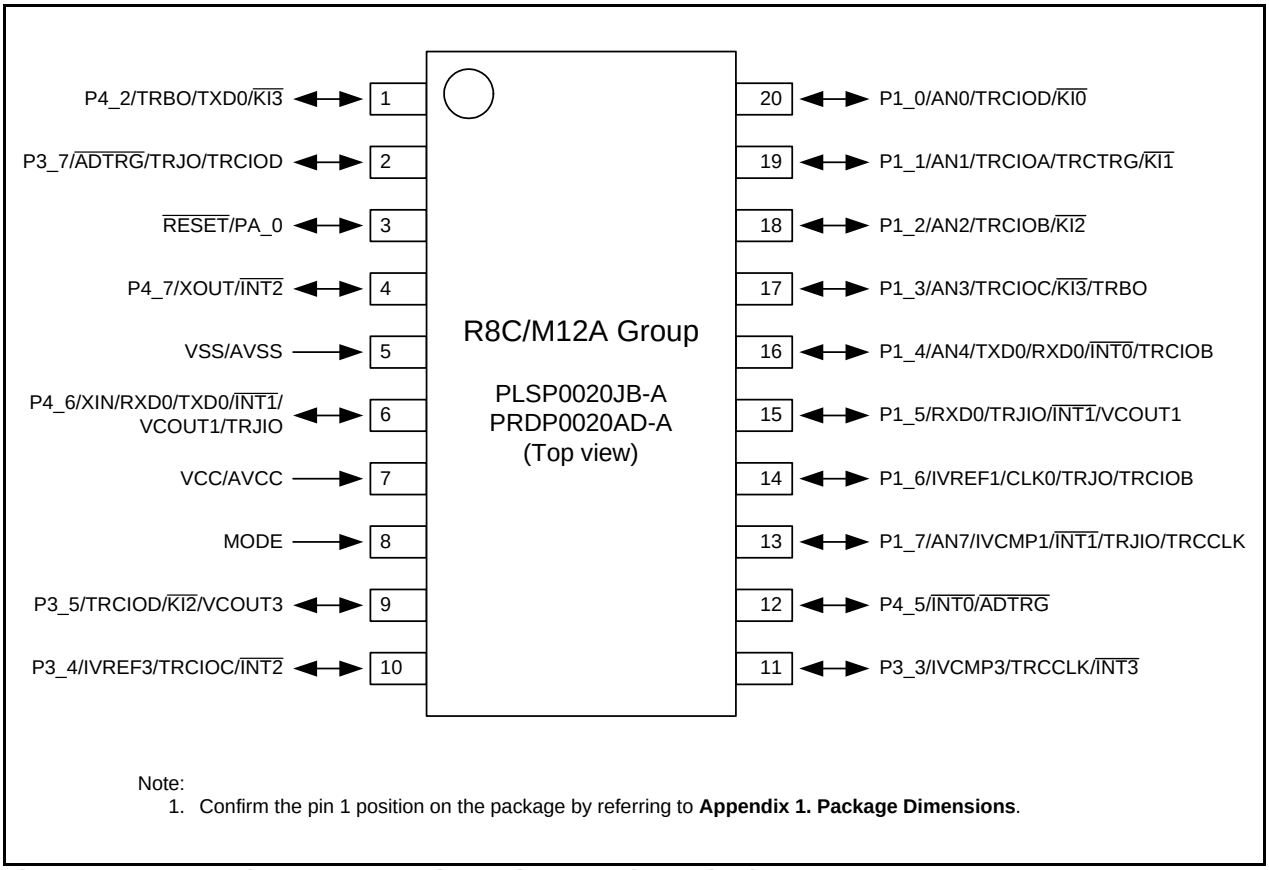
1.4 Pin Assignment

Figures 1.3 and 1.4 show Pin Assignment (Top View). Table 1.6 lists the Pin Name Information by Pin Number.



Note:
1. Confirm the pin 1 position on the package by referring to **Appendix 1. Package Dimensions**.

Figure 1.3 R8C/M11A Group Pin Assignment (Top View)



Note:
1. Confirm the pin 1 position on the package by referring to **Appendix 1. Package Dimensions**.

Figure 1.4 R8C/M12A Group Pin Assignment (Top View)

WDR Bit (Watchdog timer reset detect flag)

This flag indicates that a reset has been generated by the watchdog timer.

[Condition for setting to 0]
• When a software reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a watchdog timer reset occurs.

8. Watchdog Timer

The watchdog timer is a function for detecting program malfunctions. Using this function is recommended, since it can improve system reliability.
The watchdog timer also has a function that can be used as a periodic timer.

8.1 Overview

The watchdog timer has a 14-bit down counter, and count source protection mode can be enabled or disabled.
Table 8.1 lists the Watchdog Timer Specifications.
For details on the watchdog timer reset, see **6.3.5 Watchdog Timer Reset**.
For details on the periodic timer, see **8.3.4 Periodic Timer Function**.
Figure 8.1 shows the Watchdog Timer Block Diagram.

Table 8.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock or low-speed on-chip oscillator clock (1/16)	Low-speed on-chip oscillator clock
Count operation	Decrement	
Count start condition	Either of the following can be selected: • The count is automatically started after a reset. • The count is started by writing to the WDTS register.	
Count stop conditions	When wait mode or stop mode is entered while the count source is the CPU clock	None
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register during the refresh acceptance period (when a refresh acceptance period is set) • Underflow	
Operation at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Selection of the count source Selected by bits WDTC6 to WDTC7 in the WDTC register. • Count source protection mode - Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register. - If count source protection mode is disabled, whether count source protection mode is enabled or disabled is selected by the CSPRO bit in the CSPR register. • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register. • Initial value of the watchdog timer (underflow period) Selected by bits WDTUFS0 to WDTUFS1 in the OFS2 register. • Refresh acceptance period for the watchdog timer Selected by bits WDTRCS0 to WDTRCS1 in the OFS2 register.	

8.3.4 Periodic Timer Function

The count range is determined by the underflow period setting (bits WDTUFS0 to WDTUFS1 in the OFS2 register) and the refresh acceptance period setting (bits WDTRCS0 to WDTRCS1 in the OFS2 register). The periodic timer cannot be used in stop mode.
Table 8.5 lists the Periodic Timer Settings. Figure 8.3 shows the Timing of Periodic Timer Function.
When the periodic timer runs beyond the count range in Table 8.5, the WDTIF bit in the WDTIR register is set to 1 (periodic timer interrupt requested).

Table 8.5 Periodic Timer Settings

Initial Value Set by Bits WDTUFS1 to WDTUFS0 in OFS2 Register	Refresh Range Set by Bits WDTRCS1 to WDTRCS0 in OFS2 Register (1)	Range Counted by Periodic Timer
11b	10b	3FFFh → 2FFFh
	01b	3FFFh → 1FFFh
	00b	3FFFh → 0FFFh
10b	10b	1FFFh → 17FFh
	01b	1FFFh → 0FFFh
	00b	1FFFh → 07FFh
01b	10b	0FFFh → 0BFFh
	01b	0FFFh → 07FFh
	00b	0FFFh → 03FFh
00b	10b	03FFh → 02FFh
	01b	03FFh → 01FFh
	00b	03FFh → 00FFh

Note:
1. When bits WDTRCS1 to WDTRCS0 in the OFS2 register is 11b (100 %), set the WDTIE bit to 0 (periodic timer interrupt disabled).

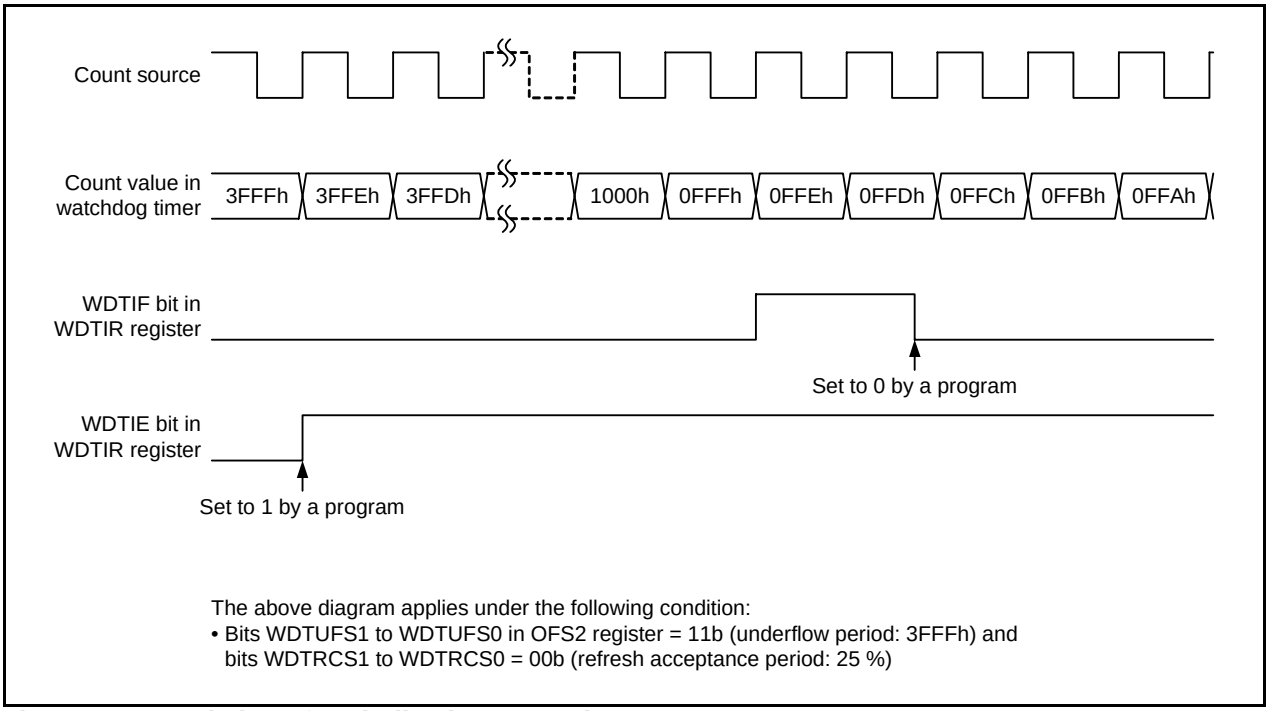
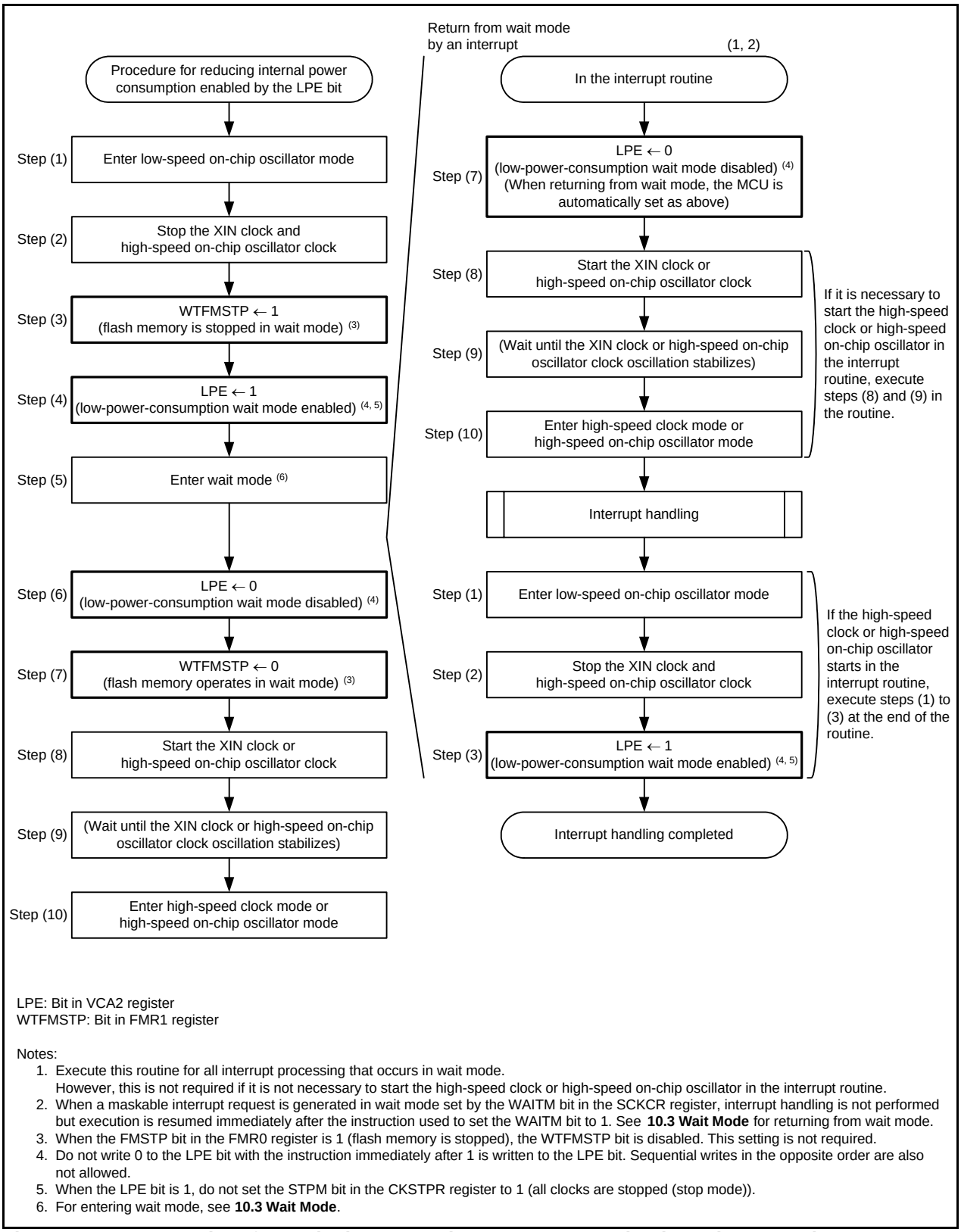


Figure 8.3 Timing of Periodic Timer Function

10.5.9 Reducing Internal Power Consumption

When entering wait mode using low-speed on-chip clock mode or low-speed on-chip oscillator mode, internal power consumption can be reduced using the LPE bit in the VCA2 register. To enable low internal power consumption using the LPE bit, follow **Figure 10.5 Procedure for Reducing Internal Power Consumption by Using LPE Bit**.



LPE: Bit in VCA2 register
WTFMSTP: Bit in FMR1 register

Notes:
1. Execute this routine for all interrupt processing that occurs in wait mode.
   However, this is not required if it is not necessary to start the high-speed clock or high-speed on-chip oscillator in the interrupt routine.
2. When a maskable interrupt request is generated in wait mode set by the WAITM bit in the SCKCR register, interrupt handling is not performed but execution is resumed immediately after the instruction used to set the WAITM bit to 1. See **10.3 Wait Mode** for returning from wait mode.
3. When the FMSTP bit in the FMR0 register is 1 (flash memory is stopped), the WTFMSTP bit is disabled. This setting is not required.
4. Do not write 0 to the LPE bit with the instruction immediately after 1 is written to the LPE bit. Sequential writes in the opposite order are also not allowed.
5. When the LPE bit is 1, do not set the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)).
6. For entering wait mode, see **10.3 Wait Mode**.

Figure 10.5 Procedure for Reducing Internal Power Consumption by Using LPE Bit

Table 11.2 Descriptions of Interrupts

Interrupt	Description
Undefined instruction interrupt	An unidentified instruction interrupt is generated when the UND instruction is executed.
Overflow interrupt	An overflow interrupt is generated when the O flag is 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that change the O flag are as follows: ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.
BRK instruction interrupt	A BRK interrupt is generated when the BRK instruction is executed.
INT instruction interrupt	An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers the INT instruction can specify are 0 to 63. The number is assigned to each peripheral function interrupt. When the INT instruction is executed specifying the number, the peripheral function interrupt with the same number can be executed. For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution, and the U flag is set to 0 (ISP) before the interrupt sequence is executed. The U flag is restored from the stack when the MCU returns from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.
Watchdog timer interrupt	This interrupt is generated by the watchdog timer. For details, see **8. Watchdog Timer**.
Oscillation stop detection interrupt	This interrupt is generated by the oscillation stop detection function. For details on the oscillation stop detection function, see **9. Clock Generation Circuit**.
Voltage monitor 1 interrupt	This interrupt is generated by the voltage detection circuit. For details on the voltage detection circuit, see **7. Voltage Detection Circuit**.
Single-step interrupt	Do not use this interrupt. It is provided exclusively for use in development tools.
Address match interrupt	When one of the AIENi0 bit (i = 0 or 1) in the AIENi register is 1 (enabled), an address match interrupt is generated immediately before executing the instruction that is stored at an address indicated by the corresponding AIADRi register (i = 0 or 1). For details on the address match interrupt, see **11.7 Address Match Interrupt**.
Peripheral function interrupt	A peripheral function interrupt is generated by a peripheral function in the MCU. For the interrupt sources for the corresponding peripheral function interrupt, see the interrupts and the vector table addresses as listed in **Table 11.6 Relocatable Vector Table**. For details on the peripheral functions, see the descriptions of individual peripheral functions.

11.2.4 Key Input Enable Register (KIEN)

Address 0003Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	$\overline{KI0}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	$\overline{KI0}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	$\overline{KI1}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	$\overline{KI1}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	$\overline{KI2}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	$\overline{KI2}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	$\overline{KI3}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	$\overline{KI3}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W

Note:
1. Changing the bits KIiPL or KIiEN (i = 0 to 3) may set the IRKI bit in the IRR3 register to 1 (interrupt requested). See **11.9.4 Rewriting Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN**.

11.2.8 Interrupt Monitor Flag Register 2 (IRR2)

Address 00052h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IRCMP3	IRCMP1	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0.	R
b1	—			
b2	IRCMP1	Comparator B1 interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b3	IRCMP3	Comparator B3 interrupt request monitor flag		R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

The IRR2 register is the monitor flag register for comparator B1 and comparator B3 interrupt requests. See **11.4.2.1 Registers IRR0 to IRR2** for the relation between interrupt monitor flag bits and peripheral function interrupts.

13.3.4 Timer RJ Mode Register (TRJMR)

Address 000DCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RJ operating mode select bits	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode Other than the above: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	TEDGPL	TRJIO edge polarity select bit	0: One-way edge 1: Two-way edge	R/W
b4	TCK0	Timer RJ count source select bits (1, 2)	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fHOCO 0 1 1: f2 Other than the above: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RJ count source cutoff bit (2)	0: Count source is supplied 1: Count source is cut off	R/W

Notes:
1. When event counter mode is selected, the external input (TRJIO) is selected as the count source regardless of the setting of bits TCK0 to TCK2.
2. Do not switch or cut off the count source during count operation. When switching or cutting off the count source, set the TSTART bit in the TRJCR register to 0 (count is stopped) and the TCSTF bit to 0 (count is stopped) to stop the timer count.

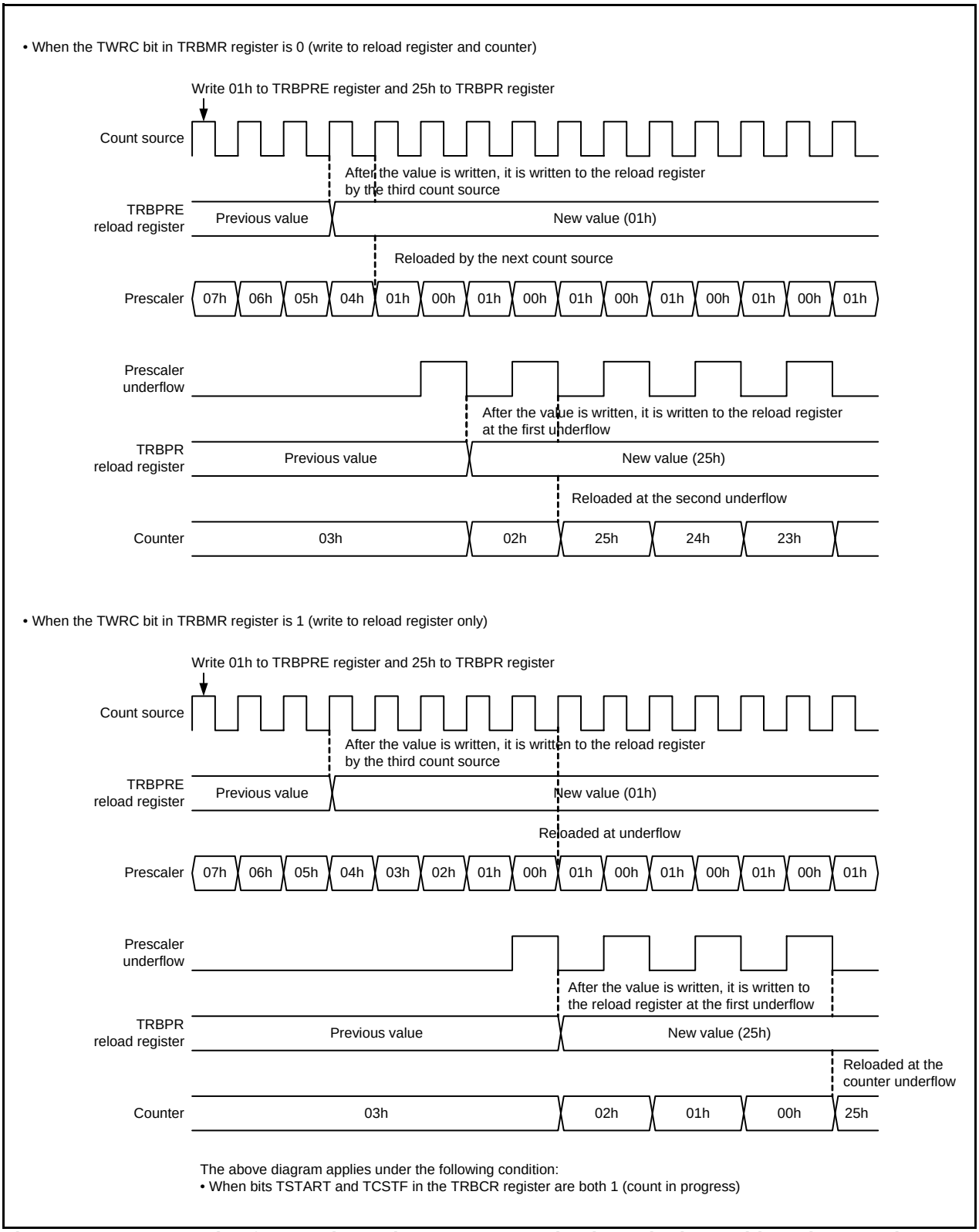
Select the operating mode when the count is stopped (the TSTART bit is 0 and the TCSTF bit is 0).
When a value is written to the TRJMR register, the toggle flip-flop is initialized.

13.3.5 Timer RJ Event Select Register (TRJISR)

Address 000DDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	RCCPSEL2	RCCPSEL1	RCCPSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCCPSEL0	Timer RC output signal select bits	b1 b0 0 0: TRCIOD 0 1: TRCIOC 1 0: TRCIOB 1 1: TRCIOA	R/W
b1	RCCPSEL1			R/W
b2	RCCPSEL2	Timer RC output signal inversion bit	0: Low-level period of timer RC output signal is counted 1: High-level period of timer RC output signal is counted	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			



The above diagram applies under the following condition:
• When bits TSTART and TCSTF in the TRBCR register are both 1 (count in progress)

Figure 14.10 Example of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler (Timer Mode or Programmable One-Shot Generation Mode)

15. Timer RC

Timer RC is a 16-bit timer that provides output compare and input capture functions and can count external events. It can be used as a multifunction timer with various applications such as generation of pulse output with an arbitrary duty cycle using the compare match between the timer RC counter and four general registers.

15.1 Overview

Table 15.1 lists the Timer RC Specifications. Table 15.2 lists the Timer RC Functions. Figure 15.1 shows the Timer RC Block Diagram. Table 15.3 lists Timer RC Pin Configuration.

Table 15.1 Timer RC Specifications

Item			Description
Count sources (counter input clocks)	Operating clock	Internal clock	• f1, f2, f4, f8, or f32: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 000b to 100b. • fHOCO: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 110b.
		External clock (external event count)	TRCCLK input: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 101b.
Pulse I/O pins			4
General registers			4 • Can be set as output compare or input capture registers individually. • Can be used as buffer registers for output compare or input capture.
Operating modes	Timer mode		• Output compare function: Low-level, high-level, or toggle output can be performed. • Input capture function: A rising edge, falling edge, or two-way edge can be detected. • Counter clear function: A count period can be set.
	PWM mode		PWM output with up to three phases.
	PWM2 mode		Pulse output with an arbitrary period and duty.
Interrupt sources			• Compare match/input capture multiplexed interrupt × 4 sources • Overflow interrupt
Others			• The initial value of the timer RC output can be set arbitrarily. • A/D conversions triggered by compare matches in registers TRCGRA, TRCGRB, TRCGRC, and TRCGRD can be set.

Table 15.2 Timer RC Functions

Item		Counter	I/O Pin			
			TRCIOA	TRCIOB	TRCIOC	TRCIOD
General registers (output compare/input capture multiplexed registers)		Period setting with the TRCGRA register	TRCGRA register	TRCGRB register	TRCGRC register In buffer operation Buffer register for the TRCGRA register	TRCGRD register In buffer operation Buffer register for the TRCGRB register
Counter clear function		Input capture/ compare match for the TRCGRA register	Input capture/ compare match for the TRCGRA register	—	—	—
		TRCTRG input	—	—	—	—
Setting function for initial output level		—	Available	Available	Available	Available
Buffer operation		—	Available	Available	—	—
Compare match	Low-level output	—	Available	Available	Available	Available
	High-level output	—	Available	Available	Available	Available
	Toggle output	—	Available	Available	Available	Available
Input capture function		—	Available	Available	Available	Available
PWM mode		—	—	Available	Available	Available
PWM2 mode		—	—	Available	—	—
Interrupt sources		Overflow	Compare match/ input capture	Compare match/ input capture	Compare match/ input capture	Compare match/ input capture

16.3.1.4 Continuous Receive Mode

Continuous receive mode is selected by setting the U0RRM bit in the U0C1 register to 1 (continuous receive mode enabled). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to 0 (data present in the U0TB register). When the U0RRM bit is 1, do not write dummy data to the U0TB register by a program.

16.3.1.5 Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedure below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

17.2.4 A/D Control Register 0 (ADCON0)

Address 0009Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start bit	0: A/D conversion stops 1: A/D conversion starts	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The ADCON0 register is used to control A/D conversion operation.

ADST Bit (A/D conversion start bit)

The ADST bit is used to start or stop A/D conversion.

[Conditions for setting to 0]
- When A/D conversion is completed in one-shot mode or single sweep mode.
- When 0 is written to this bit by software. (A/D conversion stops)

[Conditions for setting to 1]
- When 1 is written to this bit by software. (A/D conversion starts)
- When the A/D conversion start trigger enabled by the TRCADCR register is input.
- When an external trigger ($\overline{\text{ADTRG}}$) is input.

Table 17.6 A/D Conversion Time

Item	Symbol	A/D Conversion Clock				
		f1	f2	f4	f8	fAD
		CKS0 = 1	CKS0 = 0	CKS0 = 1	CKS0 = 0	CKS0 = 0
		CKS1 = 1		CKS1 = 0		CKS1 = 0
		CKS2 = 0 (1)				CKS2 = 1 (2)
A/D conversion start delay time (3)	tD	3	3 to 4	3 to 6	3 to 10	3
Input sampling time	tSPL	16	31	61	121	16
A/D comparison time	tCMP	25	50	100	200	25
A/D conversion time	tCONV	44	84 to 85	164 to 167	324 to 331	44
End processing time	tEND	2 to 3 cycles of fAD				

CKS0, CKS1, CKS2: Bits in ADMOD register

Notes:
1. The numerical values in the table indicate the number of system clock (f) cycles.
2. The numerical values in the table indicate the number of fAD cycles.
3. In repeat mode, single sweep mode, and repeat sweep mode, there is no delay time during the A/D conversion time (tCONV) for the second and subsequent rounds.

17.3.1.2 External Trigger Input Timing

A/D conversion can also be started by an external trigger input. When bits ADCAP1 to ADCAP0 in the ADMOD register are 11b (A/D conversion is started by external trigger ($\overline{\text{ADTRG}}$)), an external trigger can be input to the $\overline{\text{ADTRG}}$ pin. The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) on the rising edge of the $\overline{\text{ADTRG}}$ input pin and A/D conversion is started. Other operations are the same as when the ADST bit in the ADCON0 register set to 1 by software.

Figure 17.3 shows the External Trigger Input Timing.

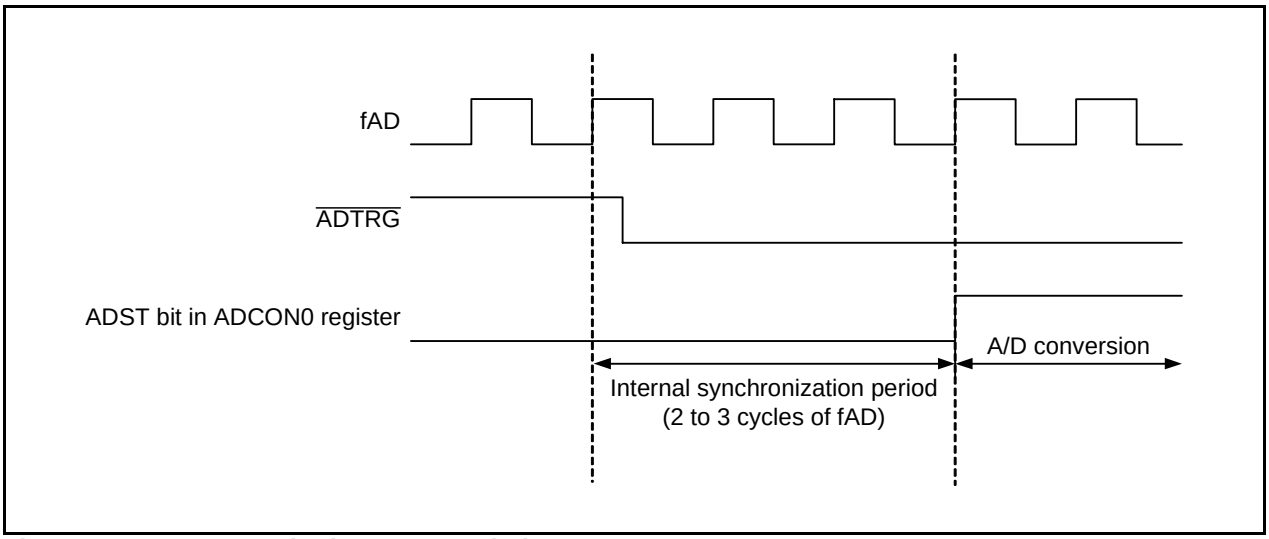


Figure 17.3 External Trigger Input Timing

FST2 Bit (LBDATA monitor flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and then read the FST2 bit after the FST7 bit is set to 1 (ready).
This bit is updated when the program, erase, and read lock bit status commands are generated. When the read lock bit status command is input, the FST7 bit is set to 0 (busy). When the FST7 bit is set to 1 (ready), the lock bit status is stored in the FST2 bit. The data in the FST2 bit is retained until the next command is input.

FST3 Bit (Program-suspend status flag)

This is a read-only bit indicating the suspend status. This bit is set to 1 when a program-suspend request is acknowledged and a program-suspend status is entered; otherwise it is set to 0.

FST4 Bit (Program error status flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise it is set to 0. For details, see the description in **19.6.7 Full Status Check**.

FST5 Bit (Erase error/blank check error status flag)

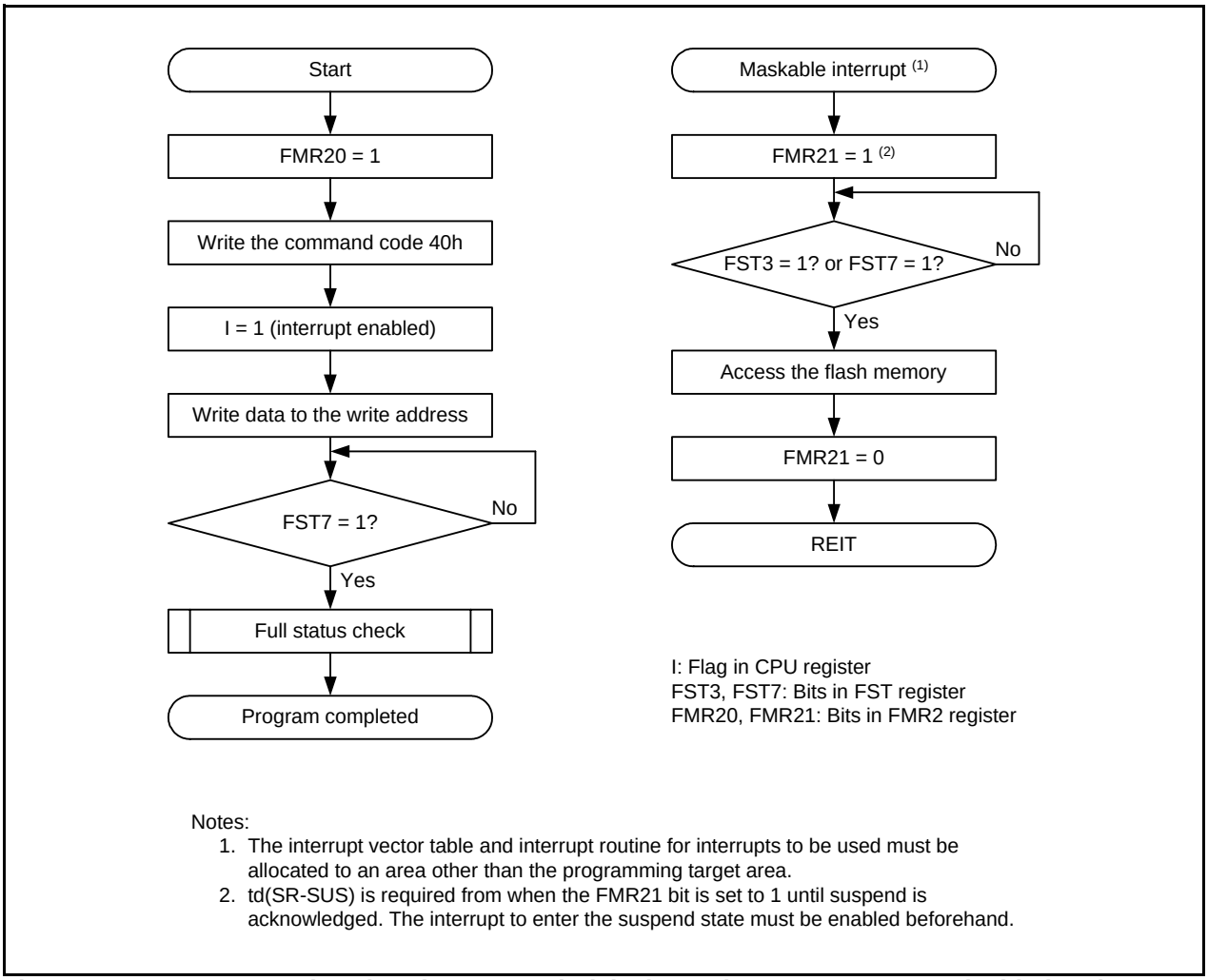
This is a read-only bit indicating the status of auto-erase or block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise it is set to 0. For details, see the description in **19.6.7 Full Status Check**.

FST6 Bit (Erase-suspend status flag)

This is a read-only bit indicating the suspend status. This bit is set to 1 when an erase-suspend request is acknowledged and an erase-suspend status is entered; otherwise it is set to 0.

FST7 Bit (Ready/busy status flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:
• During programming
• During erasure
• During the lock bit program
• During the read lock bit status
• During the block blank check
• During forced stop operation
• The flash memory is being stopped
• The flash memory is being activated
Otherwise, the FST7 bit is set to 1 (ready).

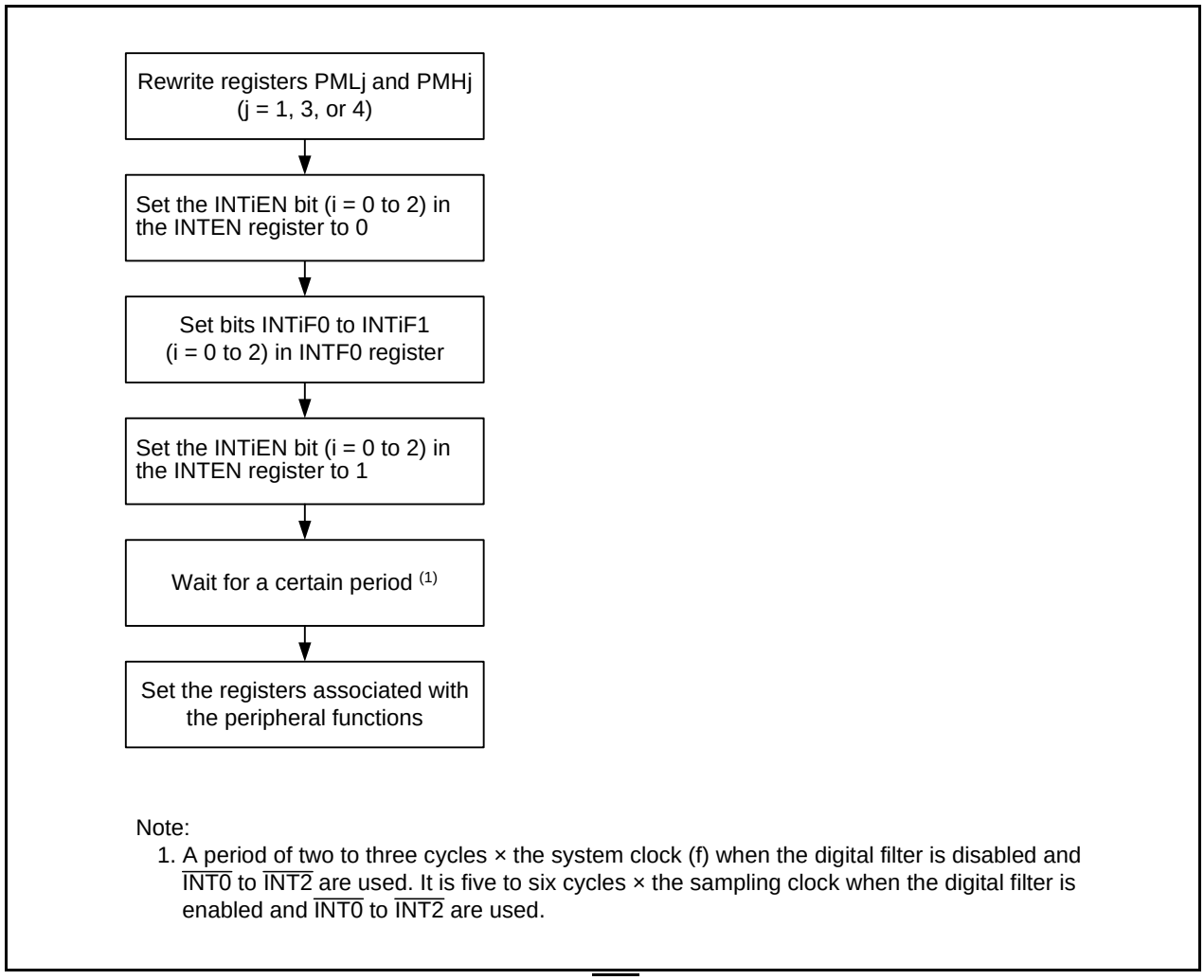


Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter the suspend state must be enabled beforehand.

Figure 19.9 Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

21.5.6 Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions

Figure 21.3 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC).

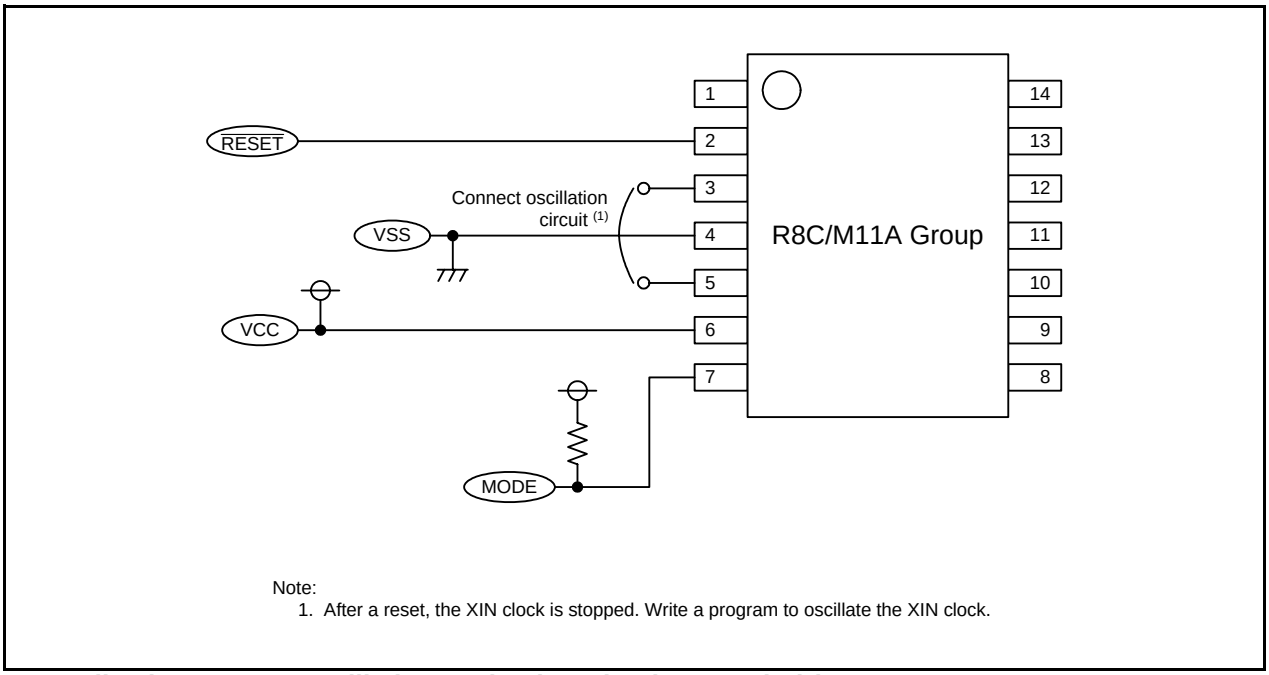


Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used.

Figure 21.3 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC)

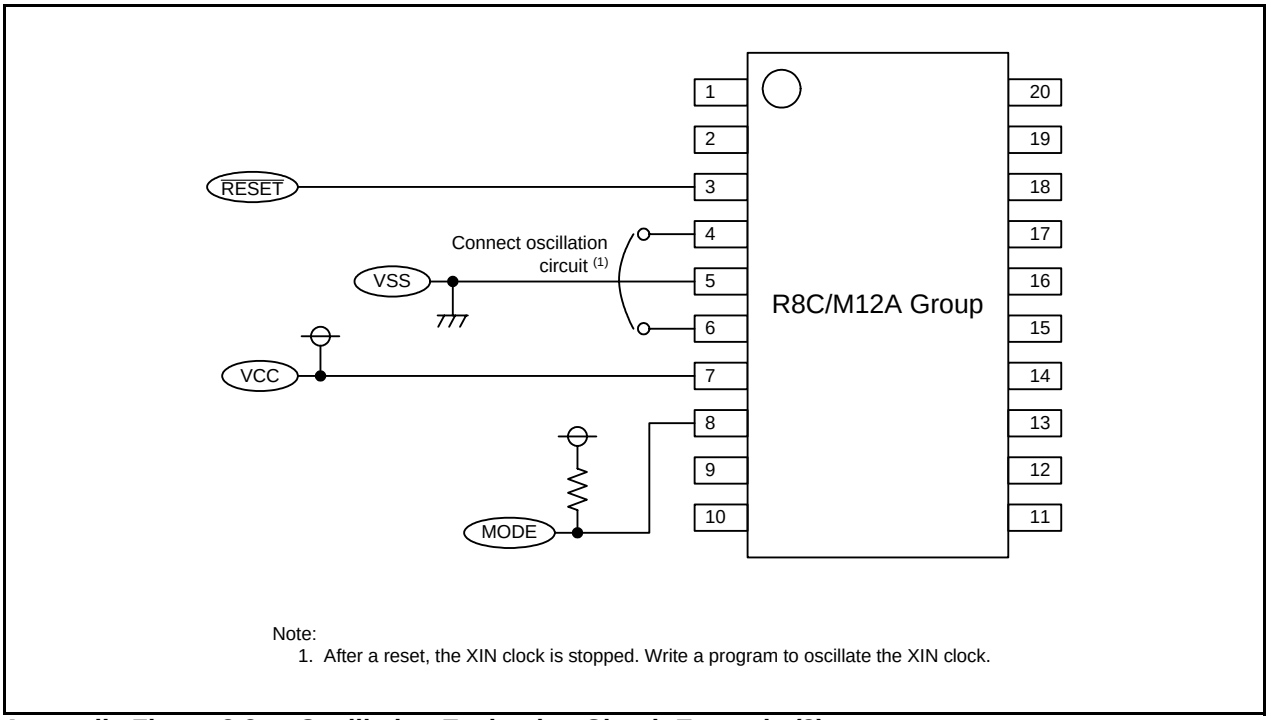
Appendix 3. Oscillation Evaluation Circuit Example

Appendix Figures 3.1 and 3.2 show Oscillation Evaluation Circuit Examples.



Note:
1. After a reset, the XIN clock is stopped. Write a program to oscillate the XIN clock.

Appendix Figure 3.1 Oscillation Evaluation Circuit Example (1)



Note:
1. After a reset, the XIN clock is stopped. Write a program to oscillate the XIN clock.

Appendix Figure 3.2 Oscillation Evaluation Circuit Example (2)

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Colophon 1.1