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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36074lfzv

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. For details, see the text of the manual.

The following documents apply to the R8C/M11A Group and R8C/M12A Group. Make sure to see the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/M11A Group, R8C/M12A Group Datasheet	R01DS0010EJ
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: For details on using peripheral functions, see the application notes.	R8C/M11A Group, R8C/M12A Group User's Manual: Hardware	This User's manual
User's manual: Software	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

SFR Page Reference

Address	Register Name	Symbol	Page
00000h			
00001h			
00002h			
00003h			
00004h			
00005h			
00006h			
00007h			
00008h			
00009h			
0000Ah			
0000Bh			
0000Ch			
0000Dh			
0000Eh			
0000Fh			
00010h	Processor Mode Register 0	PM0	26, 37
00011h			
00012h	Module Standby Control Register	MSTCR	27
00013h	Protect Register	PRCR	28
00014h			
00015h			
00016h	Hardware Reset Protect Register	HRPR	28
00017h			
00018h			
00019h			
0001Ah			
0001Bh			
0001Ch			
0001Dh			
0001Eh			
0001Fh			
00020h	External Clock Control Register	EXCKCR	76
00021h	High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	77
00022h	System Clock f Control Register	SCKCR	78
00023h	System Clock f Select Register	PHISEL	79
00024h	Clock Stop Control Register	CKSTPR	80
00025h	Clock Control Register When Returning from Modes	CKRSCR	81
00026h	Oscillation Stop Detection Register	BAKCR	83
00027h			
00028h			
00029h			
0002Ah			
0002Bh			
0002Ch			
0002Dh			
0002Eh			
0002Fh			
00030h	Watchdog Timer Function Register	RISR	64
00031h	Watchdog Timer Reset Register	WDTR	65
00032h	Watchdog Timer Start Register	WDTS	65
00033h	Watchdog Timer Control Register	WDTC	65
00034h	Count Source Protection Mode Register	CSPR	66
00035h	Periodic Timer Interrupt Control Register	WDTIR	66
00036h			
00037h			
00038h	External Input Enable Register	INTEN	112
00039h			
0003Ah	INT Input Filter Select Register 0	INTF0	112
0003Bh			
0003Ch	INT Input Edge Select Register 0	ISCR0	113
0003Dh			
0003Eh	Key Input Enable Register	KIEN	114
0003Fh			

Address	Register Name	Symbol	Page
00040h	Interrupt Priority Level Register 0	ILVL0	115
00041h			
00042h	Interrupt Priority Level Register 2	ILVL2	115
00043h	Interrupt Priority Level Register 3	ILVL3	115
00044h	Interrupt Priority Level Register 4	ILVL4	115
00045h	Interrupt Priority Level Register 5	ILVL5	115
00046h	Interrupt Priority Level Register 6	ILVL6	115
00047h	Interrupt Priority Level Register 7	ILVL7	115
00048h	Interrupt Priority Level Register 8	ILVL8	115
00049h	Interrupt Priority Level Register 9	ILVL9	115
0004Ah	Interrupt Priority Level Register A	ILVLA	115
0004Bh	Interrupt Priority Level Register B	ILVLB	115
0004Ch	Interrupt Priority Level Register C	ILVLC	115
0004Dh	Interrupt Priority Level Register D	ILVLD	115
0004Eh	Interrupt Priority Level Register E	ILVLE	115
0004Fh			
00050h	Interrupt Monitor Flag Register 0	IRR0	116
00051h	Interrupt Monitor Flag Register 1	IRR1	116
00052h	Interrupt Monitor Flag Register 2	IRR2	117
00053h	External Interrupt Flag Register	IRR3	118
00054h			
00055h			
00056h			
00057h			
00058h	Voltage Monitor Circuit Edge Select Register	VCAC	52
00059h			
0005Ah	Voltage Detect Register 2	VCA2	53
0005Bh	Voltage Detection 1 Level Select Register	VD1LS	54
0005Ch	Voltage Monitor 0 Circuit Control Register	VW0C	55
0005Dh	Voltage Monitor 1 Circuit Control Register	VW1C	56
0005Eh			
0005Fh	Reset Source Determination Register	RSTFR	29, 38
00060h			
00061h			
00062h			
00063h			
00064h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 0	FR18S0	83
00065h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 1	FR18S1	84
00066h			
00067h	High-Speed On-Chip Oscillator Control Register 1	FRV1	84
00068h	High-Speed On-Chip Oscillator Control Register 2	FRV2	84
00069h			
0006Ah			
0006Bh			
0006Ch			
0006Dh			
0006Eh			
0006Fh			
00070h			
00071h			
00072h			
00073h			
00074h			
00075h			
00076h			
00077h			
00078h			
00079h			
0007Ah			
0007Bh			
0007Ch			
0007Dh			
0007Eh			
0007Fh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 1.4 Specifications (2)

Item	Function	Description
Flash memory		• Program/erase voltage for program ROM: VCC = 1.8 V to 5.5 V • Program/erase voltage for data flash: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ID code check, protection enabled by lock bit • Debug functions: On-chip debug, on-board flash rewrite function
Operating frequency/ Power supply voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)
Temperature range		-20 °C to 85 °C (N version) -40 °C to 85 °C (D version) (1)
Package		14-pin TSSOP: [Package code] PTSP0014JA-B 14-pin DIP: [Package code] PRDP0014AC-A 20-pin LSSOP: [Package code] PLSP0020JB-A 20-pin DIP: [Package code] PRDP0020AD-A

Note:
1. Specify the D version if it is to be used.

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.8 list the SFR Information. Table 3.9 lists the ID Code Area and Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Register Name	Symbol	After Reset
00000h			
00001h			
00002h			
00003h			
00004h			
00005h			
00006h			
00007h			
00008h			
00009h			
0000Ah			
0000Bh			
0000Ch			
0000Dh			
0000Eh			
0000Fh			
00010h	Processor Mode Register 0	PM0	00h
00011h			
00012h	Module Standby Control Register	MSTCR	00h (2) 01110111b (3)
00013h	Protect Register	PRCR	00h
00014h			
00015h			
00016h	Hardware Reset Protect Register	HRPR	00h
00017h			
00018h			
00019h			
0001Ah			
0001Bh			
0001Ch			
0001Dh			
0001Eh			
0001Fh			
00020h	External Clock Control Register	EXCKCR	00h
00021h	High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h
00022h	System Clock f Control Register	SCKCR	00h
00023h	System Clock f Select Register	PHISEL	00h
00024h	Clock Stop Control Register	CKSTPR	00h
00025h	Clock Control Register When Returning from Modes	CKRSCR	00h
00026h	Oscillation Stop Detection Register	BAKCR	00h
00027h			
00028h			
00029h			
0002Ah			
0002Bh			
0002Ch			
0002Dh			
0002Eh			
0002Fh			
00030h	Watchdog Timer Function Register	RISR	10000000b (4) 00h (5)
00031h	Watchdog Timer Reset Register	WDTR	XXh
00032h	Watchdog Timer Start Register	WDTS	XXh
00033h	Watchdog Timer Control Register	WDTC	01XXXXXXb
00034h	Count Source Protection Mode Register	CSPR	10000000b (4) 00h (5)
00035h	Periodic Timer Interrupt Control Register	WDTIR	00h
00036h			
00037h			
00038h	External Input Enable Register	INTEN	00h
00039h			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The MSTINI bit in the OFS2 register is 0.
3. The MSTINI bit in the OFS2 register is 1.
4. The CSPROINI bit in the OFS register is 0.
5. The CSPROINI bit in the OFS register is 1.

8.3 Operation

8.3.1 Items Common to Multiple Modes

8.3.1.1 Refresh Acceptance Period

The period for accepting a refresh operation to the watchdog timer (a write to the WDTR register) can be selected by bits WDTRCS0 to WDTRCS1 in the OFS2 register. Figure 8.2 shows the Watchdog Timer Refresh Acceptance Period.

When the period from the start of counting to underflow is 100 %, a refresh operation executed during the acceptance period is accepted as shown below. A refresh operation executed during a period other than the acceptance period is processed as an illegal refresh, generating a watchdog timer interrupt or watchdog timer reset (selected by the RIS bit in the RISR register). In addition, the UFIF bit in the RISR register is set to 1.

Do not perform a refresh operation when the watchdog timer is stopped.

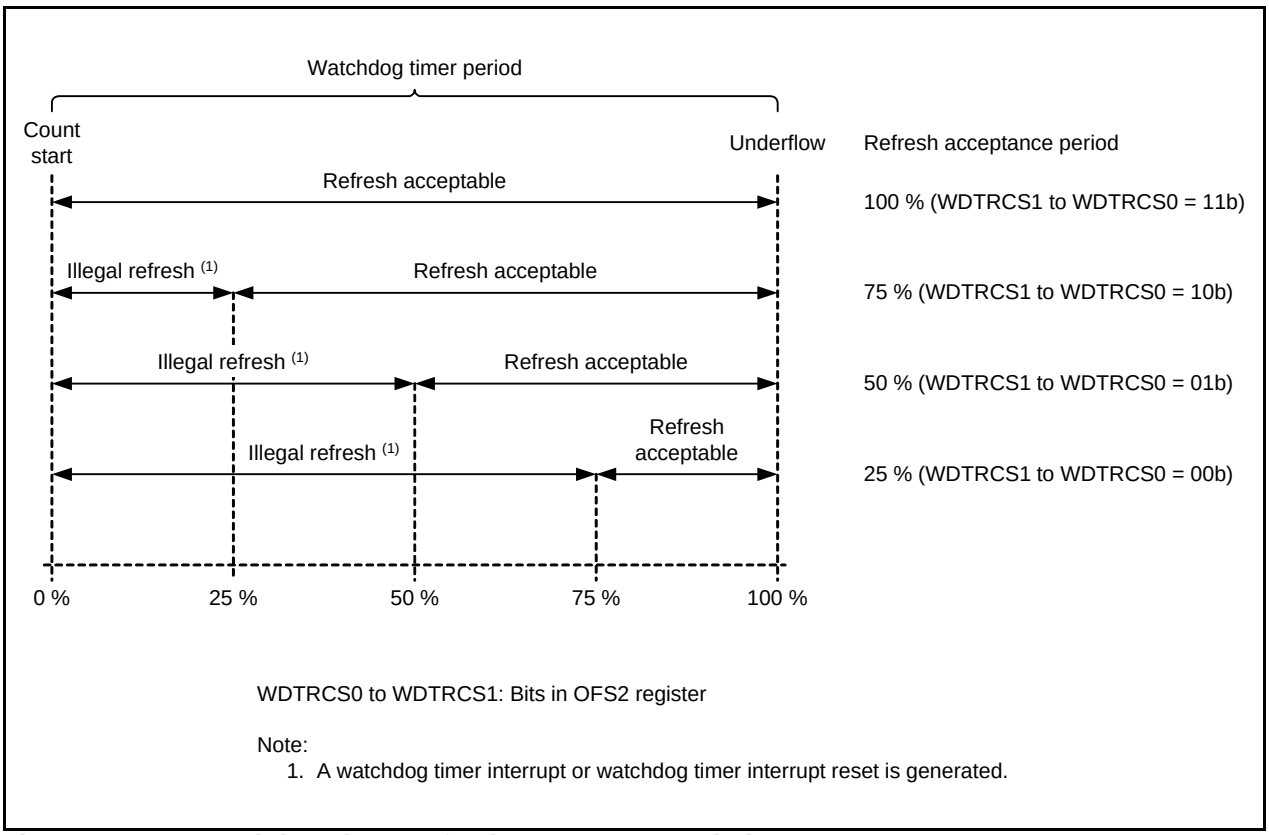


Figure 8.2 Watchdog Timer Refresh Acceptance Period

9.2.2 High-Speed/Low-Speed On-Chip Oscillator Control Register (OCOCR)

Address 00021h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	LOCODIS	HOCOE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	HOCOE	High-speed on-chip oscillator oscillation enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	LOCODIS	Low-speed on-chip oscillator oscillation stop bit	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCOCR register.

HOCOE Bit (High-speed on-chip oscillator oscillation enable bit)

The high-speed on-chip oscillator clock generated by the high-speed on-chip oscillator is stopped after a reset. Table 9.4 lists the Register Settings and High-Speed On-Chip Oscillator States. When selecting the high-speed on-chip oscillator clock as the system base clock, switch the clock according to **9.4.6 Procedure for Switching System Base Clock**.

Table 9.4 Register Settings and High-Speed On-Chip Oscillator States

Register	CKSTPR	SCKCR	CKSTPR	OCOCR	High-Speed On-Chip Oscillator State
Bit	STPM	HSCKSEL	SCKSEL	HOCOE	
Setting value	0	Other than 11b		0	Oscillation off
	0	Other than 11b		1	Oscillation on
	0	11b		X	Oscillation on
	1	X		X	Oscillation off

X: 0 or 1

LOCODIS Bit (Low-speed on-chip oscillator oscillation stop bit)

Table 9.5 lists the Register Settings and Low-Speed On-Chip Oscillator States. If the XINBAKE bit in the BAKCR register is 1 (oscillation stop detection function enabled), when the XIN clock is stopped, the low-speed on-chip oscillator starts operation and supplies the system base clock.

Table 9.5 Register Settings and Low-Speed On-Chip Oscillator States

Register	CSPR	WDTC		CKSTPR		OCOCR	Low-Speed On-Chip Oscillator State
Bit	CSPRO	WDTC7	WDTC6	STPM	SCKSEL	LOCODIS	
Setting value	0	Other than 11b		0	1	0	Oscillation on
	0	Other than 11b		0	1	1	Oscillation off
	0	Other than 11b		0	0	X	Oscillation on
	0	Other than 11b		1	X	X	Oscillation off
	0	11b		X	X	X	Oscillation on
	1	X		X	X	X	Oscillation on

X: 0 or 1

11.2.10 Address Match Interrupt Register i (AIADRi) (i = 0 or 1)

Address 001C0h (AIADR0L), 001C4h (AIADR1L)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Address 001C1h (AIADR0M), 001C5h (AIADR1M)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Address 001C2h (AIADR0H), 001C6h (AIADR1H)

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Setting for the addresses to be matched	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b21	—			
b22	—			
b23	—			

The AIADRi register (i = 0 or 1) is initialized after a voltage monitor 0 reset, power-on reset, or hardware reset. This register remains unchanged after a watchdog timer reset or software reset.

11.2.11 Address Match Interrupt Enable Register i (AIENi) (i = 0 or 1)

Address 001C3h (AIEN0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	AIEN00
After Reset	0	0	0	0	0	0	0	0

Address 001C7h (AIEN1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	AIEN10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	AIENi0	Address match interrupt enable i bit (i = 0 or 1)	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The AIENi register (i = 0 or 1) is initialized after a voltage monitor 0 reset, power-on reset, or hardware reset. This register remains unchanged after a watchdog timer reset or software reset.

12.3.5 Open-Drain Control Register 1 (POD1)

Address 000C1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POD1_7	POD1_6	POD1_5	POD1_4	POD1_3	POD1_2	POD1_1	POD1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POD1_0	Port P1_0 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b1	POD1_1	Port P1_1 open-drain control bit		R/W
b2	POD1_2	Port P1_2 open-drain control bit		R/W
b3	POD1_3	Port P1_3 open-drain control bit		R/W
b4	POD1_4	Port P1_4 open-drain control bit		R/W
b5	POD1_5	Port P1_5 open-drain control bit		R/W
b6	POD1_6	Port P1_6 open-drain control bit		R/W
b7	POD1_7	Port P1_7 open-drain control bit		R/W

The POD1 register is used to select whether the output type is CMOS output or N-channel open-drain output. These settings are enabled when the peripheral function output or output port function is selected.
The corresponding pins are set to N-channel open-drain output when the POD1_j bit (j = 0 to 7) is set to 1 (open-drain), and CMOS output when the bit is set to 0 (not open-drain).

12.3.6 Port 1 Function Mapping Register 0 (PML1)

Address 000C8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P13SEL1	P13SEL0	P12SEL1	P12SEL0	P11SEL1	P11SEL0	P10SEL1	P10SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P10SEL0	Port P1_0 function select bits	b1 b0 0 0: I/O port or AN0 input 0 1: TRCIOD 1 0: $\overline{KI0}$ 1 1: Do not set.	R/W
b1	P10SEL1			R/W
b2	P11SEL0	Port P1_1 function select bits	b3 b2 0 0: I/O port or AN1 input 0 1: TRCIOA/TRCTRG 1 0: $\overline{KI1}$ 1 1: Do not set.	R/W
b3	P11SEL1			R/W
b4	P12SEL0	Port P1_2 function select bits	b5 b4 0 0: I/O port or AN2 input 0 1: TRCIOB 1 0: $\overline{KI2}$ 1 1: Do not set.	R/W
b5	P12SEL1			R/W
b6	P13SEL0	Port P1_3 function select bits	b7 b6 0 0: I/O port or AN3 input 0 1: TRCIOC 1 0: $\overline{KI3}$ 1 1: TRBO	R/W
b7	P13SEL1			R/W

The PML1 register is used to select the functions of pins P1_0 to P1_3.

12.9 Handling of Unused Pins

Table 12.25 lists the Handling of Unused Pins. Figure 12.5 shows the Handling of Unused Pins.

Table 12.25 Handling of Unused Pins

Pin Name	Connection
Ports P1, P3_3 to P3_5, P3_7, P4_2, P4_5 to 4_7	• Set each of these pins to input mode, and either connect the pin to VSS through a resistor (pull-down) or connect it to VCC through a resistor (pull-up). (2) • Set each of these pins to output mode and leave it open. (2, 3)
$\overline{\text{RESET}}$/PA_0 (1)	Connect to VCC through a pull-up resistor. (2)

Notes:
1. When the power-on reset is used.
2. Use lines that are as short as possible (2 cm or shorter) to handle unused pins in the vicinity of the MCU.
3. When these ports are set to output mode and left open, keep the following in mind. They remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be unstable and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. The program should periodically reconfigure the content for enhanced reliability.

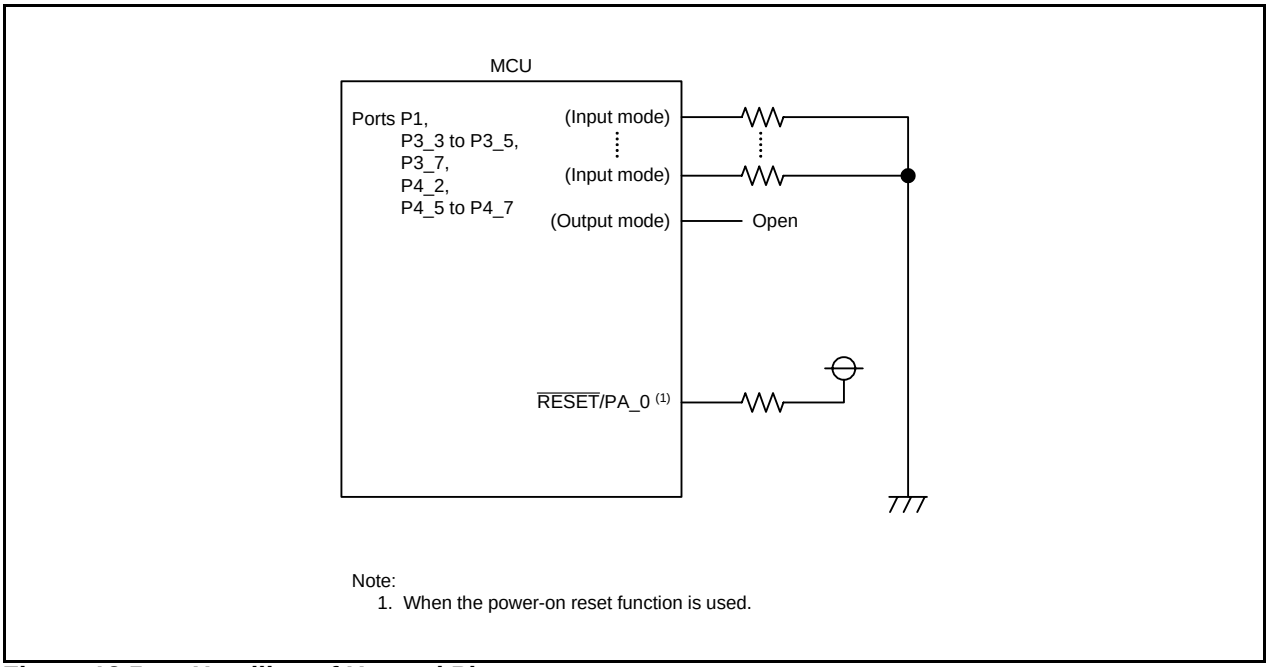


Figure 12.5 Handling of Unused Pins

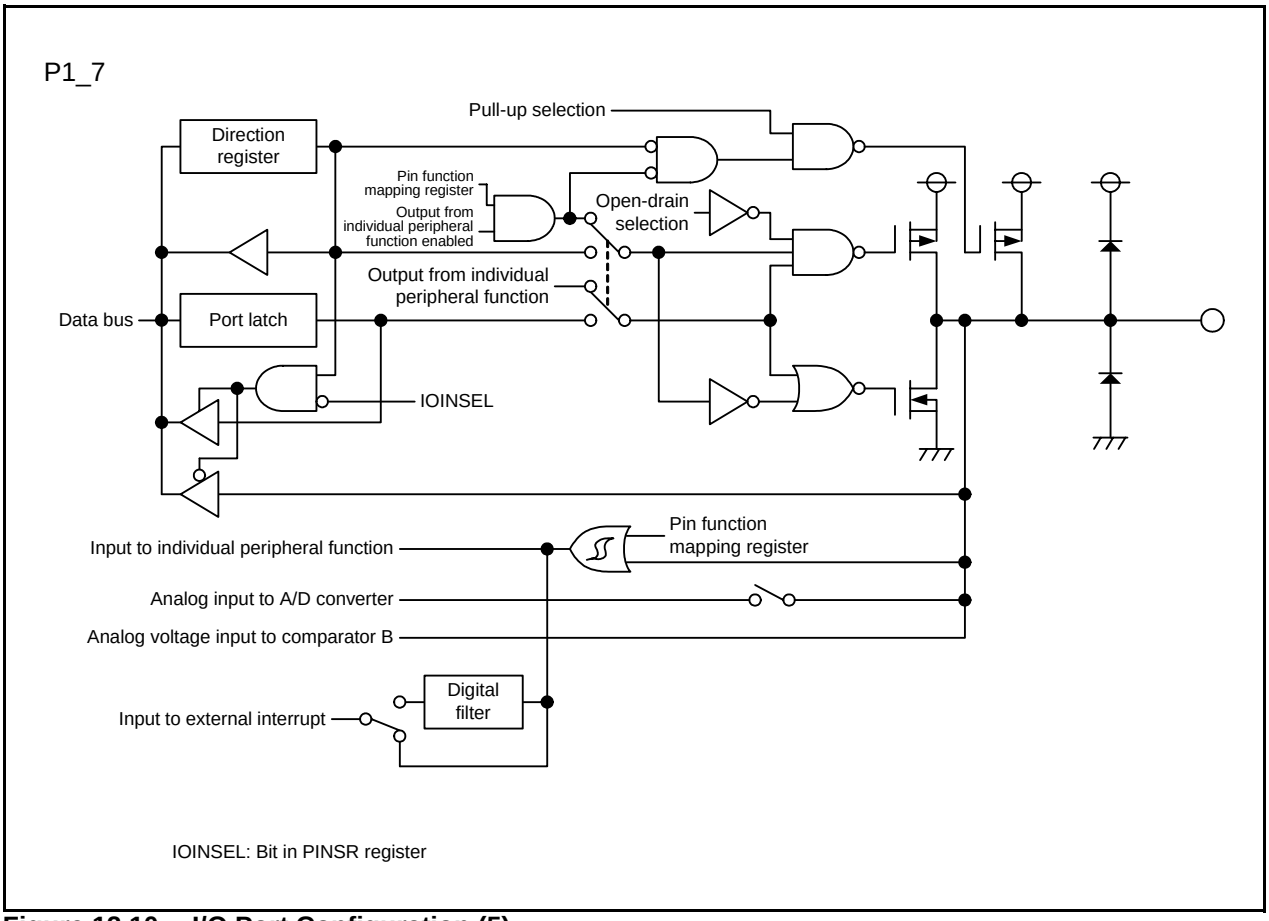


Figure 12.10 I/O Port Configuration (5)

13.3.2 Timer RJ Control Register (TRJCR)

Address 000DAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RJ count start bit (1)	0: Count is stopped 1: Count is started	R/W
b1	TCSTF	Timer RJ count status flag (1)	0: Count is stopped 1: Count is in progress	R
b2	TSTOP	Timer RJ count forced stop bit (2)	When 1 is written to this bit, the count is forcibly stopped. The read value is 0.	W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	TEDGF	Active edge judgement flag	0: No active edge received 1: Active edge received	R/W
b5	TUNDF	Timer RJ underflow flag	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Notes:
1. For notes on using bits TSTART and TCSTF, see **13.5 Notes on Timer RJ2 (2)**.
2. When 1 (count is forcibly stopped) is written to the TSTOP bit, bits TSTART and TCSTF are initialized at the same time. The pulse output level is also initialized.

Use the MOV instruction to set the TRJCR register in pulse width measurement mode and pulse period measurement mode. To avoid changing TEDGF and TUNDF at this time, write 1 to these bits.

TSTART Bit (Timer RJ count start bit)

Count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count is started), the TCSTF bit is set to 1 (count is in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count is stopped) in synchronization with the count source. For details, see **13.5 Notes on Timer RJ2 (2)**.

TCSTF Bit (Timer RJ count status flag)

[Conditions for setting to 0]
- When 0 is written to the TSTART bit (the TCSTF bit is set to 0 in synchronization with the count source).
- When 1 is written to the TSTOP bit.

[Condition for setting to 1]
- When 1 is written to the TSTART bit (the TCSTF bit is set to 1 in synchronization with the count source).

TEDGF Bit (Active edge judgement flag)

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Conditions for setting to 1]
- When the measurement of the active width of the external input (TRJIO) is completed in pulse width measurement mode.
- The set edge of the external input (TRJIO) is input in pulse period measurement mode.

TUNDF Bit (Timer RJ underflow flag)

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Condition for setting to 1]
- When the counter underflows.

14. Timer RB2

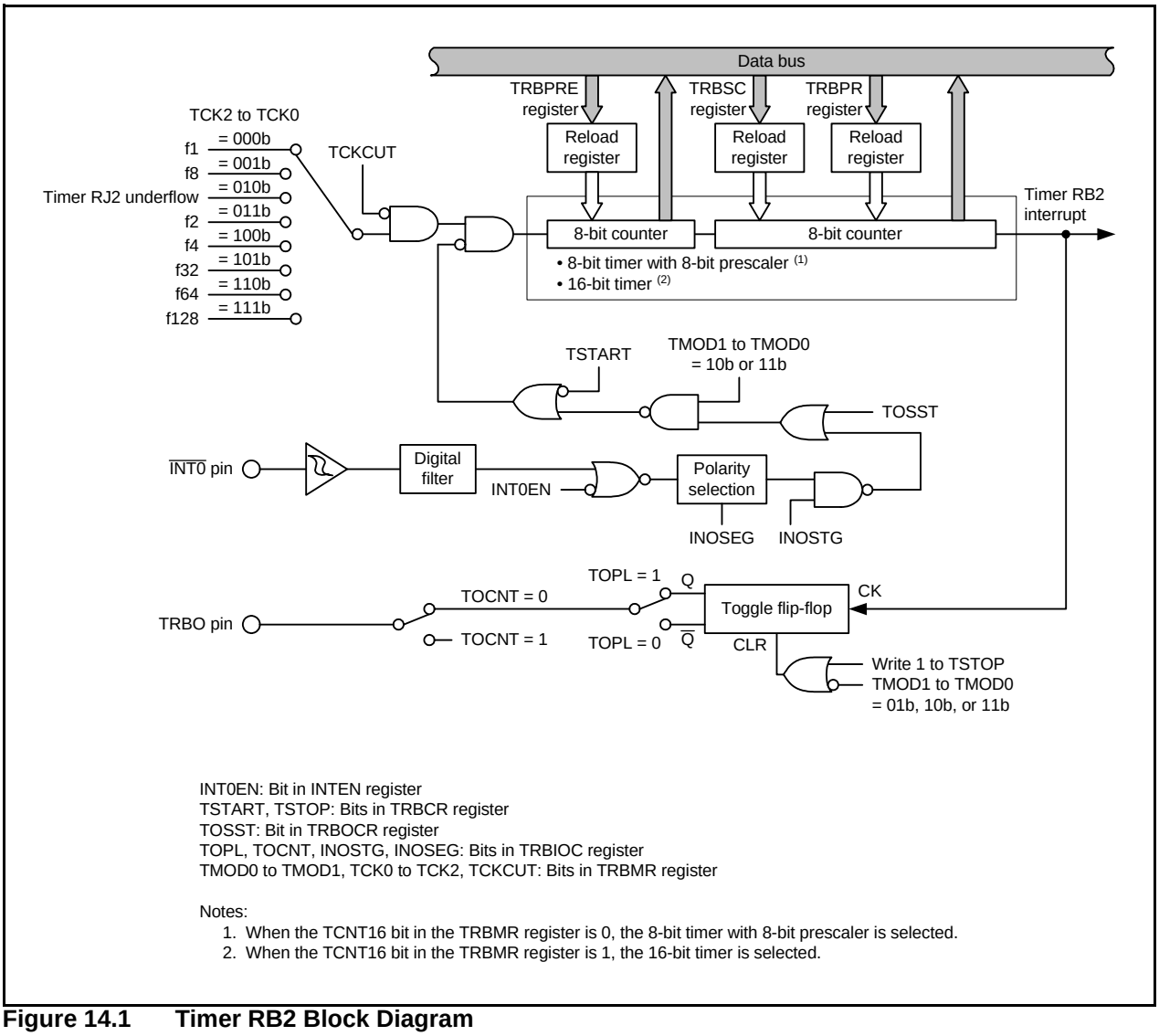
Timer RB2 can be used as an 8-bit timer with an 8-bit prescaler or as a 16-bit timer. The prescaler and timer each consist of a reload register and counter which are allocated to the same address. Timer RB2 has timer RB primary and timer RB secondary reload registers.

14.1 Overview

Table 14.1 lists the Timer RB2 Specifications. Figure 14.1 shows the Timer RB2 Block Diagram.

Table 14.1 Timer RB2 Specifications

Item		Description
Operating modes	Timer mode	An internal count source or timer RJ2 underflow is counted.
	Programmable waveform generation mode	An arbitrary pulse width is output successively.
	Programmable one-shot generation mode	A one-shot pulse is output.
	Programmable wait one-shot generation mode	A delayed one-shot pulse is output.
Count source		Selectable from f1, f2, f4, f8, f32, f64, f128, and timer RJ2 underflow.
Interrupt		Timer RB2 underflow



INT0EN: Bit in INTEN register
TSTART, TSTOP: Bits in TRBCR register
TOSST: Bit in TRBOCR register
TOPL, TOCNT, INOSTG, INOSEG: Bits in TRBIOC register
TMOD0 to TMOD1, TCK0 to TCK2, TCKCUT: Bits in TRBMR register

Notes:
1. When the TCNT16 bit in the TRBMR register is 0, the 8-bit timer with 8-bit prescaler is selected.
2. When the TCNT16 bit in the TRBMR register is 1, the 16-bit timer is selected.

Figure 14.1 Timer RB2 Block Diagram

14.3.8 Timer RB Interrupt Control Register (TRBIR)

Address 000E7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRBIE	TRBIF	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	TRBIF	Timer RB interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b7	TRBIE	Timer RB interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W

TRBIF Bit (Timer RB interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• See **Table 14.5 Conditions for Setting TRBIF Bit to 1**.

Table 14.5 Conditions for Setting TRBIF Bit to 1

Operating Mode	Condition
Timer mode	When timer RB2 underflows.
Programmable waveform generation mode	When timer RB2 underflows during the secondary period.
Programmable one-shot generation mode	When timer RB2 underflows.
Programmable wait one-shot generation mode	When timer RB2 underflows during the secondary period.

17.2.2 A/D Mode Register (ADMOD)

Address 0009Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	—	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	A/D conversion clock select bits	b2 b1 b0 0 0 0: f8 0 0 1: f4 0 1 0: f2 0 1 1: f1 1 0 0: fAD Other than the above: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	MD0	A/D operating mode select bits	b4 b3 0 0: One-shot mode 0 1: Repeat mode 1 0: Single sweep mode 1 1: Repeat sweep mode	R/W
b4	MD1			R/W
b5	—	Reserved	Set to 0.	R/W
b6	ADCAP0	A/D conversion trigger select bits	b7 b6 0 0: A/D conversion start by timer RC or external trigger is disabled 0 1: Do not set. 1 0: A/D conversion is started by conversion trigger from timer RC 1 1: A/D conversion is started by external trigger ($\overline{\text{ADTRG}}$)	R/W
b7	ADCAP1			R/W

The ADMOD register must be written only when A/D conversion is stopped.

Bits CKS0 to CKS2 (A/D conversion clock select bits)

These bits are used to select the clock for A/D conversion.

Bits ADCAP0 to ADCAP1 (A/D conversion trigger select bits)

These bits are used to select or disable the trigger for starting A/D conversion.
When using a software trigger, set bits ADCAP1 to ADCAP0 to a value other than 01b.

17.3.2 One-Shot Mode

Figure 17.4 shows an Operation Example in One-Shot Mode When Channel 1 is Selected.
In one-shot mode, A/D conversion of an analog input is performed for the specified single channel a single time as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started on the selected channel.
(2) When A/D conversion completes, the result is transferred to the ADi register (i = 0 or 1) corresponding to the channel.
(3) When A/D conversion completes, the ADF bit in the ADICSR register is set to 1 (interrupt requested). Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).
(4) The ADST bit remains at 1 (A/D conversion starts) during A/D conversion. When conversion completes, the ADST bit is automatically set to 0 (A/D conversion stops) and the A/D converter enters the standby state. When the ADST bit is set to 0 during A/D conversion, A/D conversion is stopped and the A/D converter enters the standby state.

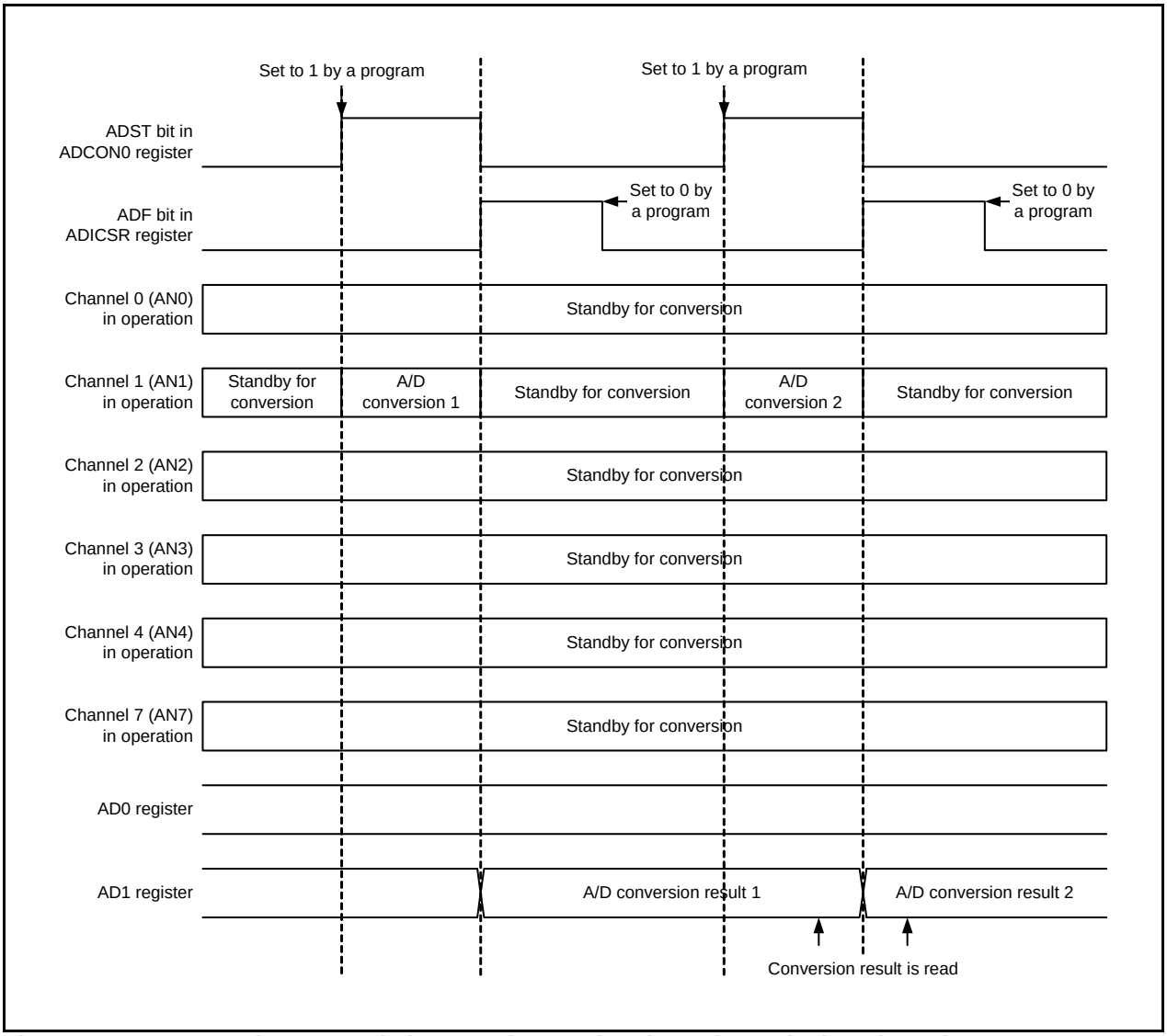


Figure 17.4 Operation Example in One-Shot Mode When Channel 1 is Selected

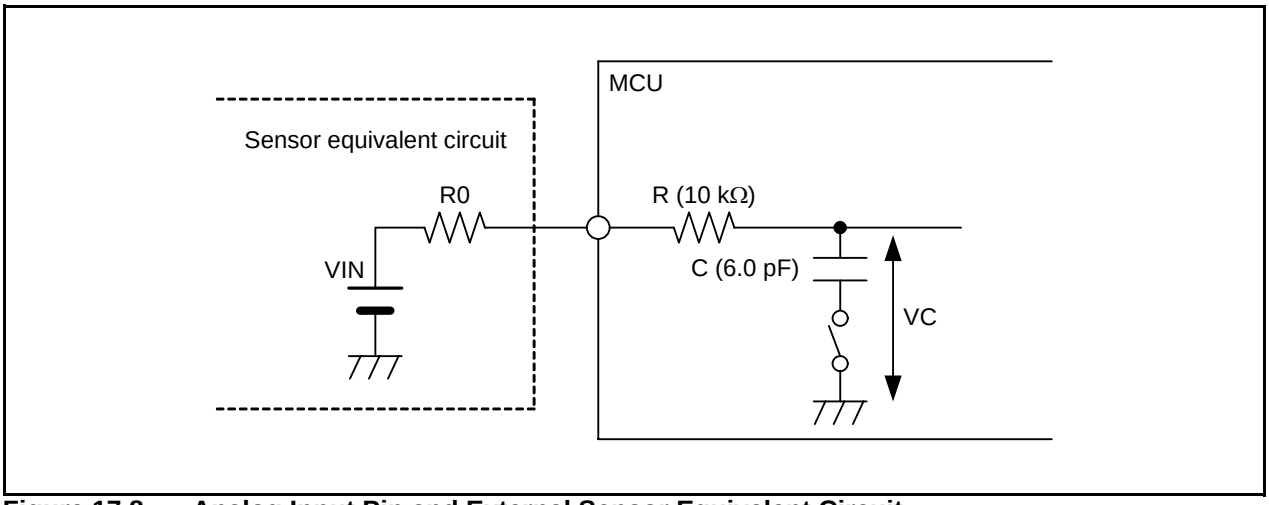


Figure 17.8 Analog Input Pin and External Sensor Equivalent Circuit

17.5.3 Register Setting

- Registers ADMOD and ADINSEL must be written only when A/D conversion is stopped.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion while the WCKSTP bit in the CKSTPR register is 1 (system clock is stopped in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory is stopped) or the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled) during A/D conversion.
- During A/D conversion, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate the conversion, the conversion result from the A/D converter will be undefined and no interrupt will be generated. The value of the ADi register (i = 0 or 1) which is not engaged in A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use any of the values of the ADi register.
- When using the A/D converter, it is recommended that the average of the conversion results be taken.

19.6.7 Full Status Check

If an error occurs, bits FST4 to FST5 in the FST register are set to 1, indicating the occurrence of the error. The execution result can be confirmed by checking these status bits (full status check).
Table 19.9 lists the Errors and FST Register States. Figure 19.19 shows the Full Status Check and Handling Procedures for Individual Errors.

Table 19.9 Errors and FST Register States

FST Register States		Error	Error Occurrence Condition
FST5 Bit	FST4 Bit		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written as the second command of the block erase, lock bit program, read lock bit status, or block blank check command (1). • The erase command is executed during erase-suspend or the block blank check command is executed. • The program, lock bit program, erase, or block blank check command is executed during program-suspend. • The program, lock bit program, erase, or block blank check command is executed to the block during suspend. • The lock bit program or read lock bit status commands are executed to the data flash.
1	0	Erase error	When the block erase command is executed and auto-erase does not complete normally.
		Blank check error	When the block blank check command is executed and data other than the blank data, FFh, is read.
0	1	Program error	When the program command is executed and auto-programming does not complete normally.
		Lock bit program error	When the lock bit command is executed, but the lock bit is not set to 0 (locked).

Note:
1. When FFh is written as the second command of these commands, the MCU enters read array mode. At the same time, the command code written as the first command becomes invalid.

Table 19.13 Interrupt Handling during CPU Rewrite Operation (EW1 Mode)

Interrupt Type	Data Flash/Program ROM	
	Suspend Enabled (FMR20 = 1)	Suspend Disabled (FMR20 = 0)
Maskable interrupt	When an interrupt request is acknowledged, the FMR21 bit is automatically set to 1 (suspend request) if the FMR22 bit is 1 (suspend request enabled by interrupt request). The flash memory suspends auto-erase or auto-programming after td(SR-SUS) and interrupt handling is executed. When auto-erase is being suspended, auto-programming and reading can be executed for any block other than the blocks being auto-erased. When auto-programming is being suspended, any block other than the blocks being auto-programmed can be read. After interrupt handling completes, auto-erase or auto-programming can be restarted by setting the FMR21 bit is set to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.	Auto-erase or auto-programming has priority. Interrupt handling is executed after auto-erase or auto-programming.
Address match	Do not use during auto-erasing or auto-programming.	
UND, INTO, and BRK instructions		
Single-step		
Watchdog timer	When an interrupt request is acknowledged, auto-erase or auto-programming is forcibly stopped immediately and the flash memory is reset. After the specified period, the flash memory is restarted before interrupt handling is started. Since auto-erase or auto-programming is forcibly stopped, the correct values may not be read from the block being auto-erased or the address being auto-programmed. After the flash memory is restarted, execute auto-erase again and verify it complete normally. The watchdog timer does not stop while the command is executing, so interrupt requests may be generated. Initialize the watchdog timer periodically using the erase-suspend function. Since the flash memory control registers are initialized in this case, these registers must be set again. (1)	
Oscillation stop detection		
Voltage monitor 1		

FMR20, FMR21, FMR22: Bits in FMR2 register

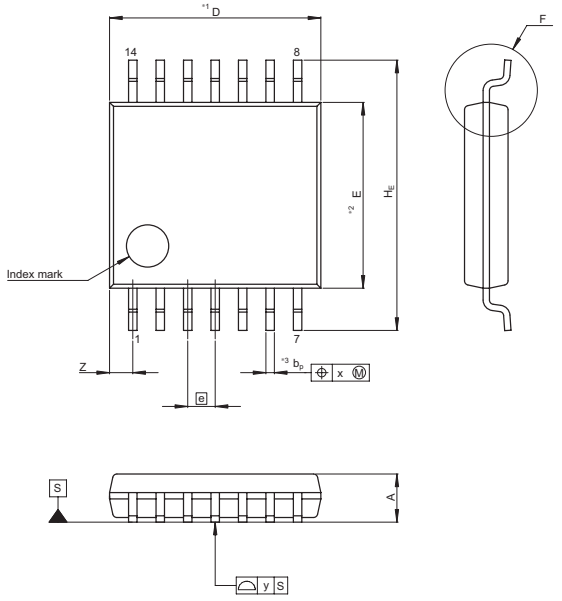
Note:

1. Registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated while the flash memory is busy.
   When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMSTP bit is 1 (flash memory is stopped), registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated.

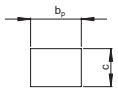
Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

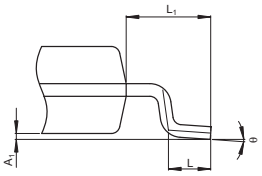
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP14-4.4x5-0.65	PTSP0014JA-B	TTP-14DV	0.05g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



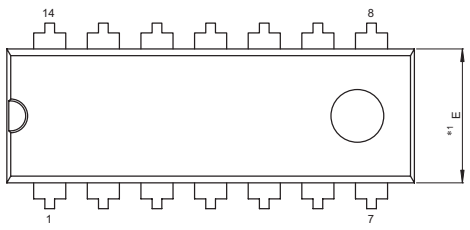
Terminal cross section
(Ni/Pd/Au plating)

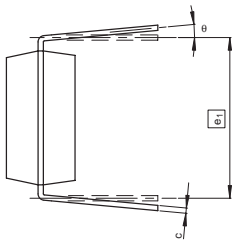


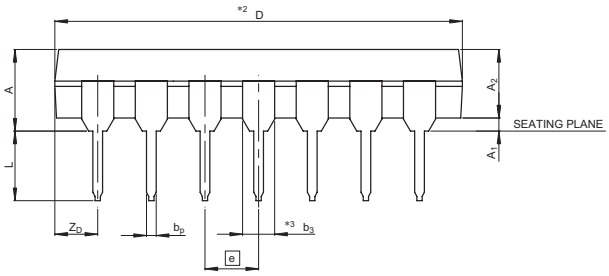
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.00	5.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.83
L	0.4	0.5	0.6
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.35x19.3-2.54	PRDP0014AC-A	14P4X-A	0.94g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	—	7.69	—
D	19.2	19.3	19.4
E	6.25	6.35	6.45
A	—	—	4.8
A_1	0.5	—	—
A_2	3.05	3.25	3.45
b_p	0.38	—	0.55
b_3	1.47	1.52	1.57
c	0.21	—	0.35
θ	0°	—	15°
e	—	2.54	—
Z_D	—	2.03	—
L	2.92	—	—

R8C/M11A Group, R8C/M12A Group

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