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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36074lfzwv

5.2.7 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer is automatically started after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) 1 0: 2.35 V (typ.) selected (Vdet0_1) 1 1: 1.90 V (typ.) selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Note:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.

   For an example of the OFS register settings, see **5.6.1 Option Function Select Area Setting Example**.

WDTON Bit (Watchdog timer start select bit)

This bit is used to select whether the watchdog timer is automatically started after a reset is cleared.

Bits VDSEL0 to VDSEL1 (Voltage detection 0 level select bits)

These bits are used to select the detection level (Vdet0) for voltage monitor 0 reset. The same level of the voltage detection 0 level selected by bits VDSEL0 to VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.

LVDAS Bit (Voltage detection 0 circuit start bit)

This bit is used to select whether voltage monitor 0 reset is enabled. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset.

CSPROINI Bit (Count source protection mode after reset select bit)

This bit is used to select whether to protect the count source for the watchdog timer from being changed.

6.2.4 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer is automatically started after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) 1 0: 2.35 V (typ.) selected (Vdet0_1) 1 1: 1.90 V (typ.) selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Note:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.

   For an example of the OFS register settings, see **5.6.1 Option Function Select Area Setting Example**.

WDTON Bit (Watchdog timer start select bit)

This bit is used to select whether the watchdog timer is automatically started after a reset is cleared.

Bits VDSEL0 to VDSEL1 (Voltage detection 0 level select bits)

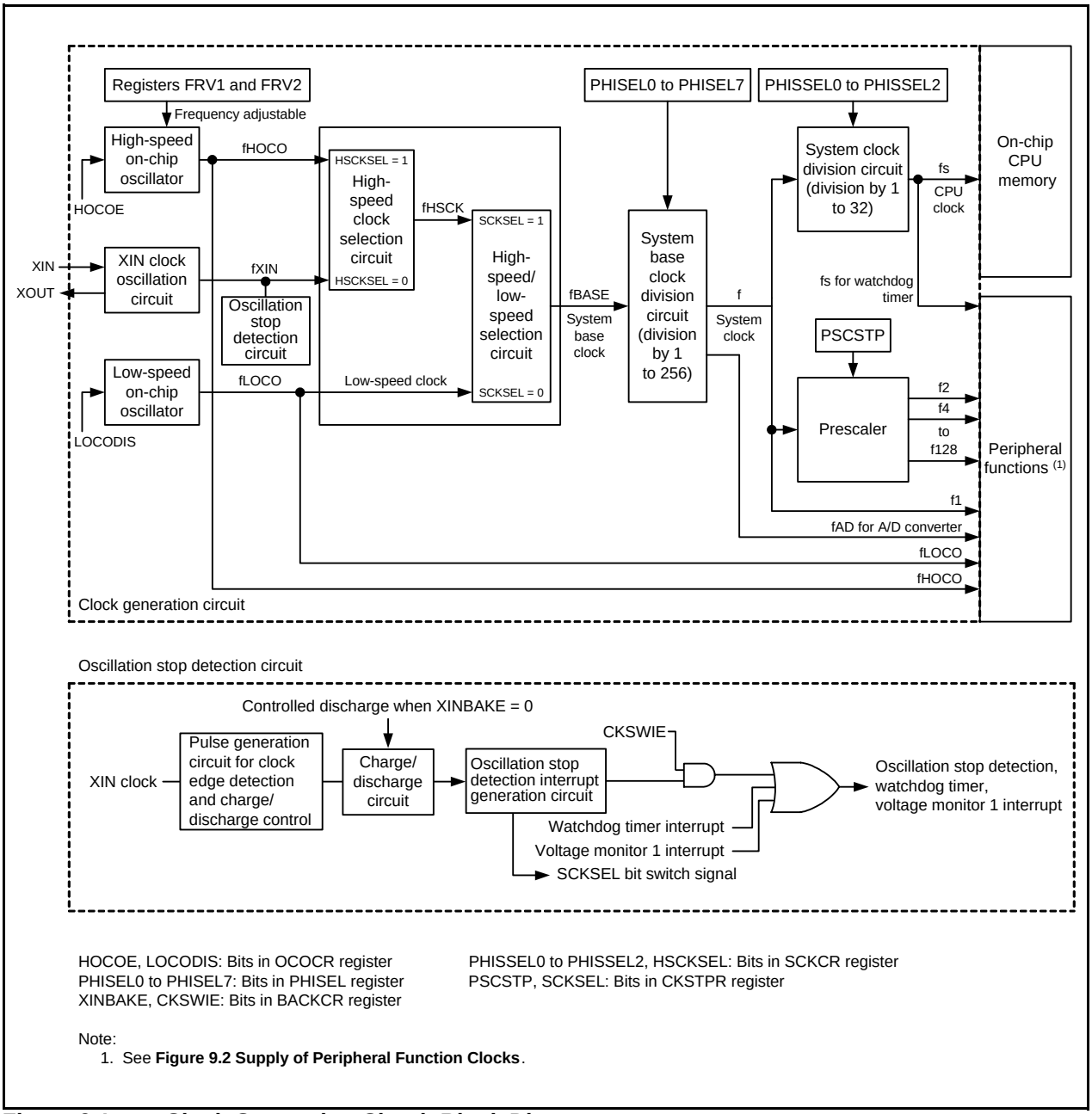
These bits are used to select the detection level (Vdet0) for voltage monitor 0 reset. The same level of the voltage detection 0 level selected by bits VDSEL0 to VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.

LVDAS Bit (Voltage detection 0 circuit start bit)

This bit is used to select whether voltage monitor 0 reset is enabled. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset.

CSPROINI Bit (Count source protection mode after reset select bit)

This bit is used to select whether to protect the count source for the watchdog timer from being changed.



HOCOE, LOCODIS: Bits in OCOCR register
PHISEL0 to PHISEL7: Bits in PHISEL register
XINBAKE, CKSWIE: Bits in BACKCR register

PHISSEL0 to PHISSEL2, HSCKSEL: Bits in SCKCR register
PSCSTP, SCKSEL: Bits in CKSTPR register

Note:
1. See **Figure 9.2 Supply of Peripheral Function Clocks**.

Figure 9.1 Clock Generation Circuit Block Diagram

11.5 $\overline{\text{INT}}$ Interrupt

11.5.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 3)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity can be selected by bits INTiSA to INTiSB in the ISCR0 register. The input pins used as the $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ input can be selected.
Inputs can be passed through a digital filter with three different sampling clocks.
The interrupt by the $\overline{\text{INTi}}$ input can be used as a wakeup function to cancel wait mode or stop mode.
Table 11.11 lists the Pin Configuration for $\overline{\text{INTi}}$ Interrupt.

Table 11.11 Pin Configuration for $\overline{\text{INTi}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P1_4, P4_5	I	$\overline{\text{INT0}}$ interrupt input
$\overline{\text{INT1}}$	P1_5, P1_7, P4_6	I	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P3_4, P4_7	I	$\overline{\text{INT2}}$ interrupt input
$\overline{\text{INT3}}$	P3_3	I	$\overline{\text{INT3}}$ interrupt input

11.8 How to Determine Interrupt Sources

Table 11.15 lists How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt. Figure 11.12 shows Example of How to Determine Interrupt Sources for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt.

Table 11.15 How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection	CKSWIF bit in BAKCR register = 1
Watchdog timer	UFIF bit in RISR register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1

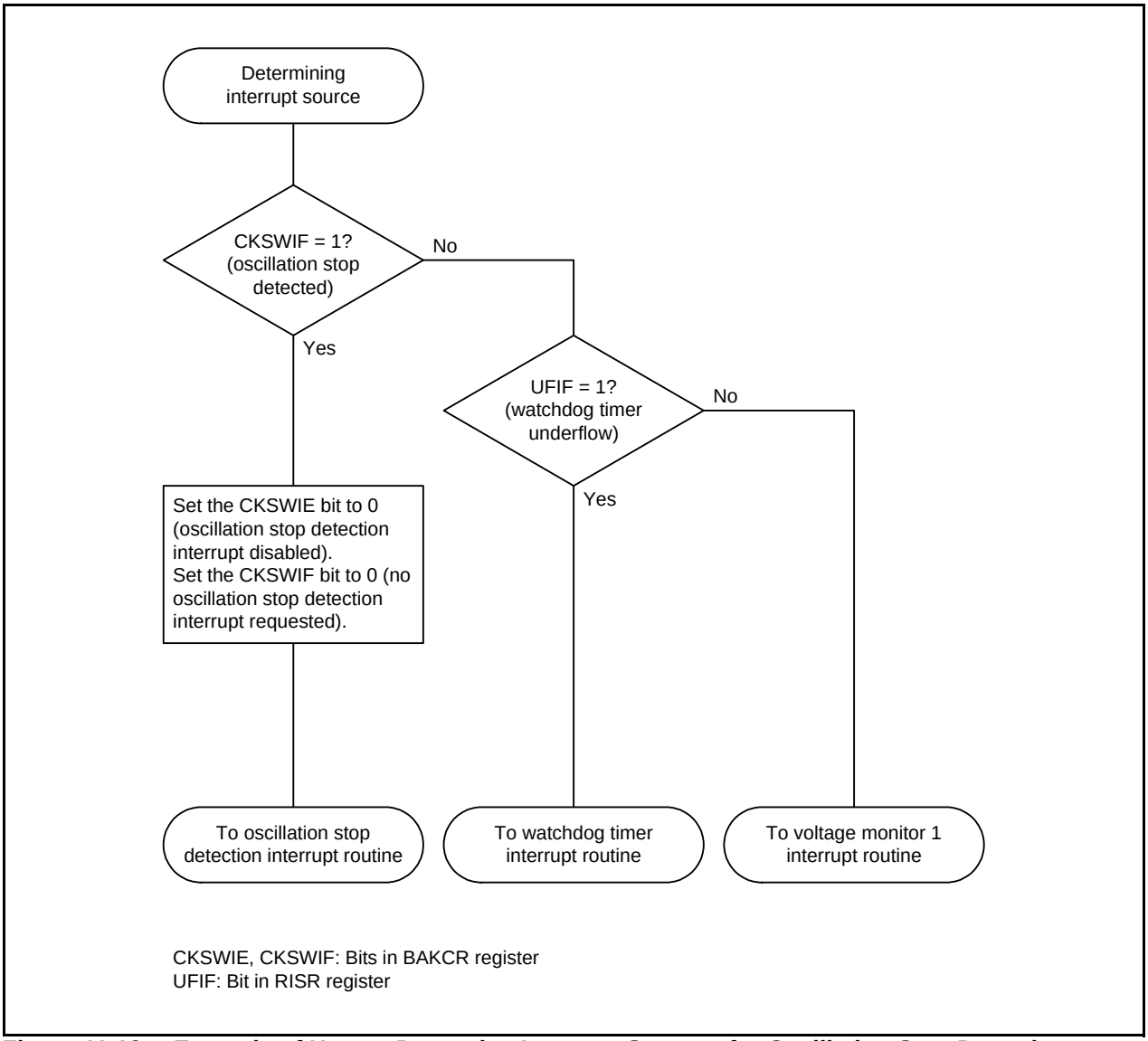


Figure 11.12 Example of How to Determine Interrupt Sources for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt

12. I/O Ports

There are 17 I/O ports. P4_6 and P4_7 can be used as I/O ports when the XIN clock oscillation circuit is not used. PA_0 can be used as an I/O port when a hardware reset is not used. In addition, all the ports are multiplexed with multiple peripheral functions.

12.1 Overview

The functions of the ports are selected by the peripheral function mapping registers (PMLi/PMHi, i = 1, 3, or 4) and the peripheral function mapping expansion registers (PMH1E and PMH4E). The functions of the I/O ports are selected by the port direction registers (PDi, i = 1, 3, 4, or A). In addition, the drive capacity of some ports can be switched. Table 12.1 shows the I/O Port Overview. Table 12.2 lists the Port Functions by Pin (R8C/M12A Group). Table 12.3 lists the I/O Port Register Configuration.

Table 12.1 I/O Port Overview

Ports	I/O	Output Type	I/O Setting	Internal Pull-Up Resistor	Drive Capacity Switching
P1_0 to P1_7	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (3)	Set in 1-bit units. (4)
P3_3, P3_4, P3_5, P3_7	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (3)	Set in 1-bit units. (4)
PA_0 (1)	I/O	3-state CMOS	Set in 1-bit units.	None	None
P4_2, P4_5, P4_6, P4_7 (2)	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (3)	None

Notes:
1. When the hardware reset is not used, this port can be used as an I/O port.
2. When the XIN clock oscillation circuit or direct input of the XIN clock is not used, these can be used as I/O ports.
3. In input mode, whether an internal pull-up resistor is connected or not can be selected by the PURi register (i = 1, 3, or 4).
4. The drive capacity of the output transistors (low or high) can be selected by the DRRi register (i = 1 or 3).

Table 12.2 Port Functions by Pin (R8C/M12A Group)

Pin Number	R8C/M12A Group	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function Select Bit		
		PM2 to PM0 = 000b	PM2 to PM0 = 001b	PM2 to PM0 = 010b	PM2 to PM0 = 011b	PM2 to PM0 = 100b	PM2 to PM0 = 101b	PM2	PM1	PM0
1	P4_2	P4_2	TRBO	TXD0	$\overline{KI3}$	—	—	—	P42SEL1	P42SEL0
2	P3_7	P3_7	$\overline{ADTRG}$	TRJO	TRCIOD	—	—	—	P37SEL1	P37SEL0
3	$\overline{RESET}$	PA_0	—	—	—	—	—	—	—	—
4	P4_7/XOUT	P4_7/XOUT	$\overline{INT2}$	—	—	—	—	—	P47SEL1	P47SEL0
5	VSS/AVSS	—	—	—	—	—	—	—	—	—
6	P4_6/XIN	P4_6/XIN	RXD0	TXD0	$\overline{INT1}$	VCOUT1	TRJIO	P46SEL2	P46SEL1	P46SEL0
7	VCC/AVCC	—	—	—	—	—	—	—	—	—
8	MODE	—	—	—	—	—	—	—	—	—
9	P3_5	P3_5	TRCIOD	$\overline{KI2}$	VCOUT3	—	—	—	P35SEL1	P35SEL0
10	P3_4	P3_4/IVREF3	TRCIOC	$\overline{INT2}$	—	—	—	—	P34SEL1	P34SEL0
11	P3_3	P3_3/IVCMP3	TRCCLK	$\overline{INT3}$	—	—	—	—	P33SEL1	P33SEL0
12	P4_5	P4_5	$\overline{INT0}$	$\overline{ADTRG}$	—	—	—	—	P45SEL1	P45SEL0
13	P1_7	P1_7/AN7/ IVCMP1	$\overline{INT1}$	TRJIO	TRCCLK	—	—	—	P17SEL1	P17SEL0
14	P1_6	P1_6/IVREF1	CLK0	TRJO	TRCIOB	—	—	—	P16SEL1	P16SEL0
15	P1_5	P1_5	RXD0	TRJIO	$\overline{INT1}$	VCOUT1	—	P15SEL2	P15SEL1	P15SEL0
16	P1_4	P1_4/AN4	TXD0	RXD0	$\overline{INT0}$	TRCIOB	—	P14SEL2	P14SEL1	P14SEL0
17	P1_3	P1_3/AN3	TRCIOC	$\overline{KI3}$	TRBO	—	—	—	P13SEL1	P13SEL0
18	P1_2	P1_2/AN2	TRCIOB	$\overline{KI2}$	—	—	—	—	P12SEL1	P12SEL0
19	P1_1	P1_1/AN1	TRCIOA/ TRCTRG	$\overline{KI1}$	—	—	—	—	P11SEL1	P11SEL0
20	P1_0	P1_0/AN0	TRCIOD	$\overline{KI0}$	—	—	—	—	P10SEL1	P10SEL0

TOPCR Bit (TRJIO output control bit)

The TOPCR bit is enabled only in pulse output mode. When this bit is set to 0, a pulse can be output from the TRJIO pin. When it is set to 1, output is disabled and the port selected as the TRJIO function becomes high impedance.
In other operating modes, the functions listed in Table 13.6 are supported regardless of the setting of the TOPCR bit.

Table 13.6 TRJIO Pin Function

Operating Mode	Function
Timer mode	Not used
Event counter mode	Event input (count source input)
Pulse width measurement mode	Input for pulse width measurement
Pulse period measurement mode	Input for pulse period measurement

Bits TIPF0 to TIPF1 (TRJIO input filter select bits)

These bits are used to specify the sampling frequency of the filter for the TRJIO input. If the input to the TRJIO pin is sampled and the value matches three successive times, that value is taken as the input value.

Bits TIOGT0 to TIOGT1 (TRJIO count control bits)

These bits are enabled only in event counter mode.
They are used to select the period to count an event input from the TRJIO pin.
When bits TIOGT1 to TIOGT0 are set to 00b, an event is always counted.
When bits TIOGT1 to TIOGT0 are set to 01b, an event is counted while the $\overline{\text{INT2}}$ pin is held high.
When bits TIOGT1 to TIOGT0 are set to 10b, an event is counted for the period corresponding to the timer RC output set by the TRJISR register. Bits RCCPSEL0 to RCCPSEL1 in the TRJISR register are used to select the timer RC output signal and the RCCPSEL2 bit is used to select the level of the timer RC output signal.

14.4.2 Programmable Waveform Generation Mode

In the 8-bit timer with 8-bit prescaler, the values in registers TRBPR and TRBSC are counted alternately.
In the 16-bit timer, the lower 8 bits are counted by the TRBPRE register and the higher 8 bits are counted by registers TRBPR and TRBSC alternately.
The TRBO pin outputs a signal which is inverted each time the counter underflows. The count is started from the value set in the TRBPR register. In programmable waveform generation mode, the TRBOCR register is not used.
When 1 (count is started) is written to the TSTART bit in the TRBCR register, the count is started after the count source is sampled three times. When 0 (count is stopped) is written to the TSTART bit, the count is stopped after the count source is sampled three times. When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped. The actual count state should be monitored with the TCSTF bit in the TRBCR register.
An interrupt request is generated when timer RB2 underflows during the secondary period.
When registers TRBPRE and TRBPR are read, each count value can be read. Read the TRBPR register even while the secondary period is counted. When registers TRBPRE, TRBPR, and TRBSC are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to the reload register and then transferred to the counter at the next reload operation.
Figure 14.3 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Waveform Generation Mode. Figure 14.4 shows an Example of 16-Bit Timer Operation in Programmable Waveform Generation Mode.

15. Timer RC

Timer RC is a 16-bit timer that provides output compare and input capture functions and can count external events. It can be used as a multifunction timer with various applications such as generation of pulse output with an arbitrary duty cycle using the compare match between the timer RC counter and four general registers.

15.1 Overview

Table 15.1 lists the Timer RC Specifications. Table 15.2 lists the Timer RC Functions. Figure 15.1 shows the Timer RC Block Diagram. Table 15.3 lists Timer RC Pin Configuration.

Table 15.1 Timer RC Specifications

Item			Description
Count sources (counter input clocks)	Operating clock	Internal clock	• f1, f2, f4, f8, or f32: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 000b to 100b. • fHOCO: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 110b.
		External clock (external event count)	TRCCLK input: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 101b.
Pulse I/O pins			4
General registers			4 • Can be set as output compare or input capture registers individually. • Can be used as buffer registers for output compare or input capture.
Operating modes	Timer mode		• Output compare function: Low-level, high-level, or toggle output can be performed. • Input capture function: A rising edge, falling edge, or two-way edge can be detected. • Counter clear function: A count period can be set.
	PWM mode		PWM output with up to three phases.
	PWM2 mode		Pulse output with an arbitrary period and duty.
Interrupt sources			• Compare match/input capture multiplexed interrupt × 4 sources • Overflow interrupt
Others			• The initial value of the timer RC output can be set arbitrarily. • A/D conversions triggered by compare matches in registers TRCGRA, TRCGRB, TRCGRC, and TRCGRD can be set.

15.3.2 PWM Mode

In PWM mode, when the TRCGRA register is set as the period register and registers TRCGRB, TRCGRC, and TRCGRD are set as duty registers, a PWM waveform is output from pins TRCIOB, TRCIOC, and TRCIOD individually. A PWM waveform with up to three phases can be output. In this mode, the general register automatically functions as an output compare register. The settings of bits IOB2, IOC2, and IOD2 are invalid. The initial output level of the corresponding pin is set according to the values in bits TOA to TOD in the TRCCR1 register and bits POLB to POLD in the TRCCR2 register.
Table 15.15 lists the Initial Output Levels of TRCIOB Pin.

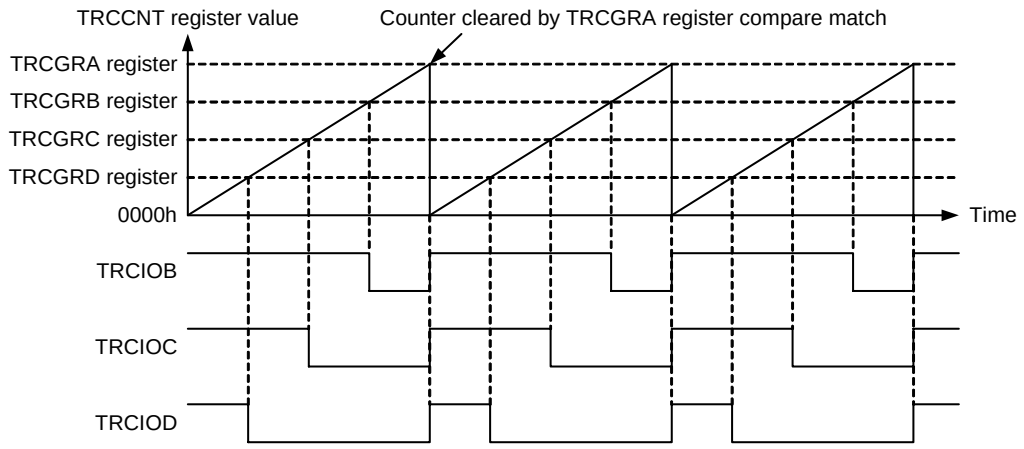
Table 15.15 Initial Output Levels of TRCIOB Pin

TOB Bit in TRCCR1 Register	POLB Bit in TRCCR2 Register	Initial Output Level
0	0	1
	1	0
1	0	0
	1	1

The output level is determined by bits POLB to POLD in the TRCCR2 register. When the POLB bit is 0 (output level is active low), the TRCIOB output pin is set to low at compare match B and high at compare match A. When the POLB bit is 1 (output level is active high), the TRCIOB output pin is set to high at compare match B and low at compare match A.
The setting values of bits PWMD to PWMB in TRCMR take precedence over those in registers TRCIOR0 and TRCIOR1. When the values set in the period and duty registers are the same, the output value remains unchanged even if a compare match occurs.

Figure 15.9 shows an Operation Example in PWM Mode.

• High-level output when TRCCNT register is cleared at compare match A. Low-level output at compare matches B, C, and D. (POLB bit = 0, POLC bit = 0, and POLD bit = 0 in TRCCR2 register)



• Low-level output when TRCCNT register is cleared at compare match A. High-level output at compare matches B, C, and D. (POLB bit = 1, POLC bit = 1, and POLD bit = 1 in TRCCR2 register)

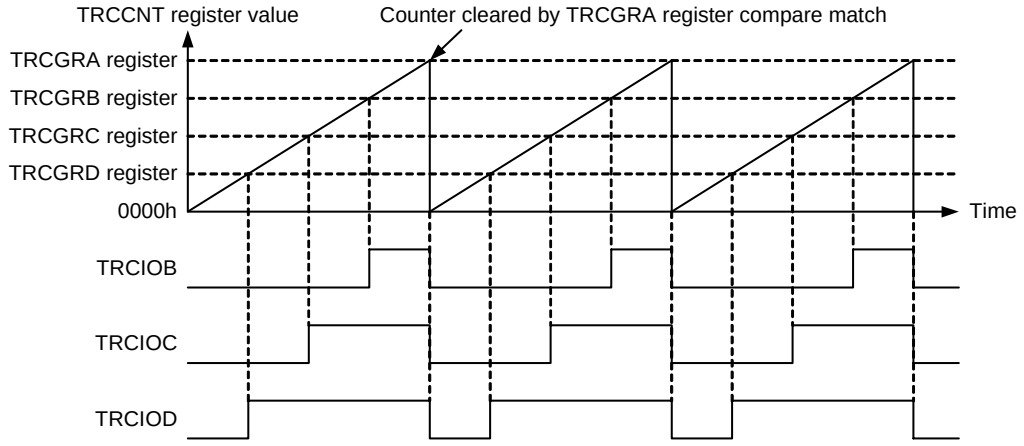


Figure 15.9 Operation Example in PWM Mode

16.3 Operation

UART0 supports two modes: Clock synchronous serial I/O mode and clock asynchronous serial I/O (UART) mode.

16.3.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, transmission or reception is performed using a transfer clock.
Table 16.4 lists the Clock Synchronous Serial I/O Mode Specifications. Table 16.5 lists the Registers and Settings Used in Clock Synchronous Serial I/O Mode.

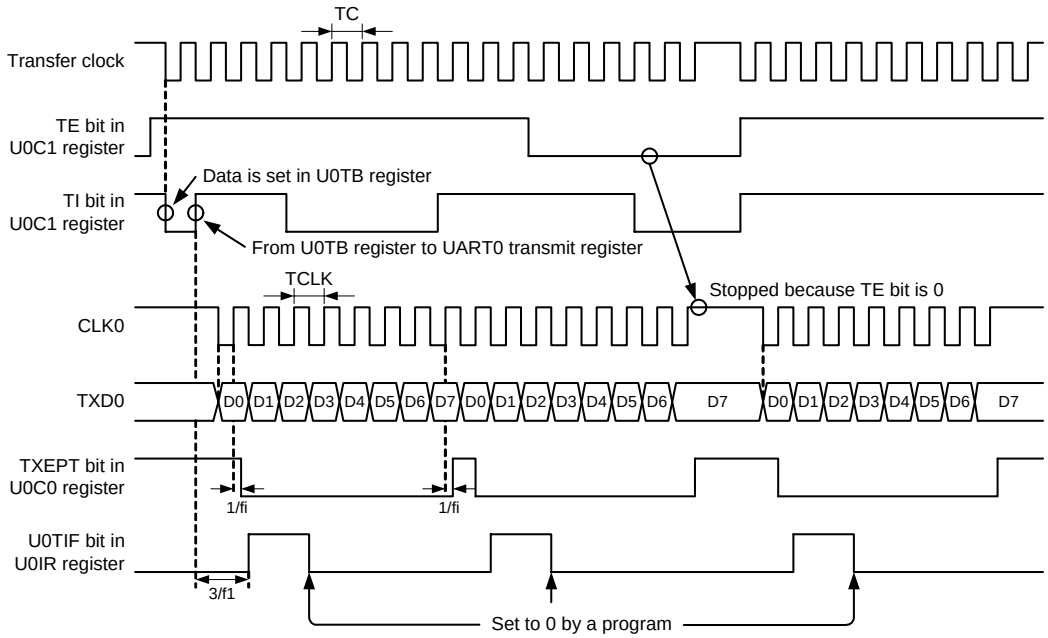
Table 16.4 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fi/(2 (n + 1)) fi = f1, f8, or f32 n = Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT (input from the CLK0 pin)
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U0C1 register must be 1 (transmission enabled). • The TI bit in the U0C1 register must be 0 (data present in the U0TB register).
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U0C1 register must be 1 (reception enabled). • The TE bit in the U0C1 register must be 1 (transmission enabled). • The TI bit in the U0C1 register must be 0 (data present in the U0TB register).
Interrupt request generation timing	• For transmission: One of the following can be selected. - The U0IRS bit in the U0C1 register is 0 (transmit buffer is empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit in the U0C1 register is 1 (transmission is completed): When data transmission from the UART0 transmit register is completed. • For reception: When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (2) This error occurs if the next data reception is started and the 7th bit is received before the U0RB register is read.
Selectable functions	• CLK polarity selection The output and input timing of transfer data can be selected to be either the rising or the falling edge of the transfer clock. • LSB first or MSB first selection The start bit can be selected to be bit 0 or bit 7 when transmission and reception are started. • Continuous receive mode selection Reading the U0RB register enables reception at the same time.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   • The external clock is set to high when the CKPOL bit in the U0C0 register is 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock).
   • The external clock is set to low when the CKPOL bit is 1 (transmit data is output on the rising edge and receive data is input on the falling edge of the transfer clock).
2. If an overrun error occurs, the receive data (b0 to b7) in the U0RB register is undefined. The U0RIF bit in the U0IR register remains unchanged.

16.3.1.1 Operation Examples

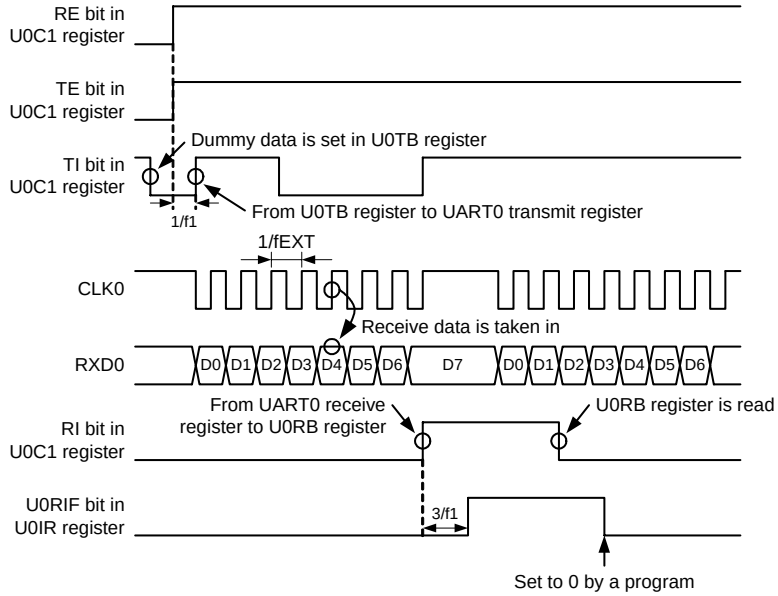
• Transmit timing example (internal clock selected)



The above diagram applies for the following settings:
- CKDIR bit in U0MR register = 0 (internal clock)
- CKPOL bit in U0C0 register = 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock)
- U0IRS bit in U0C1 register = 0 (transmit buffer is empty)

TC = TCLK = 2 (n + 1)/fi
fi: Frequency of U0BRG count source (f1, f8, or f32)
n: Value set in U0BRG register

• Receive timing example (external clock selected)



fEXT: Frequency of external clock

The above diagram applies for the following settings:
- CKDIR bit in U0MR register = 1 (external clock)
- CKPOL bit in U0C0 register = 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock)

The following requirements must be met when an input to the CLK0 pin is high before data reception:
- TE bit in U0C1 register → 1 (transmission enabled)
- RE bit in U0C1 register → 1 (reception enabled)
- Dummy data is written to U0TB register

Figure 16.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

17. A/D Converter

This MCU features a 10-bit successive approximation A/D converter that can process analog inputs for up to six channels.

17.1 Overview

Table 17.1 lists the A/D Converter Specifications. Figure 17.1 shows the A/D Converter Block Diagram.

Table 17.1 A/D Converter Specifications

Item	Specification
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage	0 V to AVCC
Input channels	6 channels (AN0 to AN4, AN7)
Resolution	10 bits
A/D conversion clock	f1, f2, f4, f8, or fAD
Conversion time	2.2 μs (A/D conversion clock = 20 MHz)
A/D operating modes	• One-shot mode: A/D conversion is performed on the specified single channel for a single round. • Repeat mode: A/D conversion is performed on the specified single channel repeatedly. • Single sweep mode: A/D conversion is performed on the specified two channels for a single round. • Repeat sweep mode: A/D conversion is performed on the specified two channels repeatedly.
A/D conversion data register (× 2)	16-bit data register corresponding to each channel group where the A/D conversion result is stored (valid data length: 10 bits).
A/D conversion start conditions	• Software trigger • Conversion start trigger from timer RC • External trigger
Interrupt source	An A/D conversion interrupt is generated when A/D conversion completes.
Others	The A/D converter is set to standby by the MSTAD bit in the MSTCR register.

17.2.2 A/D Mode Register (ADMOD)

Address 0009Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	—	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	A/D conversion clock select bits	b2 b1 b0 0 0 0: f8 0 0 1: f4 0 1 0: f2 0 1 1: f1 1 0 0: fAD Other than the above: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	MD0	A/D operating mode select bits	b4 b3 0 0: One-shot mode 0 1: Repeat mode 1 0: Single sweep mode 1 1: Repeat sweep mode	R/W
b4	MD1			R/W
b5	—	Reserved	Set to 0.	R/W
b6	ADCAP0	A/D conversion trigger select bits	b7 b6 0 0: A/D conversion start by timer RC or external trigger is disabled 0 1: Do not set. 1 0: A/D conversion is started by conversion trigger from timer RC 1 1: A/D conversion is started by external trigger ($\overline{\text{ADTRG}}$)	R/W
b7	ADCAP1			R/W

The ADMOD register must be written only when A/D conversion is stopped.

Bits CKS0 to CKS2 (A/D conversion clock select bits)

These bits are used to select the clock for A/D conversion.

Bits ADCAP0 to ADCAP1 (A/D conversion trigger select bits)

These bits are used to select or disable the trigger for starting A/D conversion.
When using a software trigger, set bits ADCAP1 to ADCAP0 to a value other than 01b.

19. Flash Memory

The flash memory supports two rewrite modes: CPU rewrite mode and standard serial I/O mode.

19.1 Overview

Table 19.1 lists the Flash Memory Specifications (see **Tables 1.3** and **1.4 Specifications** for items not listed in Table 19.1). Table 19.2 outlines Flash Memory Rewrite Mode.

Table 19.1 Flash Memory Specifications

Item		Specification
Flash memory operating modes		2 modes (CPU rewrite and standard serial I/O modes)
Erase block division		See **Figure 19.1 Flash Memory Block Diagram**.
Programming method		Byte units
Erase method		Block erase
Program/erase control method (1)		Program/erase control by software commands
Rewrite control method	Blocks 1 and 2 (program ROM) (2)	Rewrite protect control in block units by lock bits
	Blocks A and B (data flash)	Individual rewrite control on blocks A and B by bits FMR16 to FMR17 in the FMR1 register
Number of commands		6 commands
Program/erase endurance (3)	Blocks 1 and 2 (program ROM) (2)	10,000 times
	Blocks A and B (data flash)	
ID code check function (4)		Standard serial I/O mode supported

Notes:
1. When programming/erasing the program ROM and the data flash, use a VCC supply voltage in the range of 1.8 V to 5.5 V.
2. The number of blocks and their division differ depending on products. For details, see **Figure 19.1 Flash Memory Block Diagram**.
3. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. When rewrites are performed 100 or more times, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used up before performing an erase operation. Avoid rewriting only particular blocks and average out the number of programming/erasure of the blocks. It is also advisable to retain data on the number of erasure of each block and limit the number to a certain extent.
4. For details on the ID code check function, see **19.3 ID Code Check Function**.

Table 19.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode
Function	The user ROM area is rewritten by executing software commands from the CPU.	The user ROM area is rewritten using a dedicated serial programmer.
Rewritable area	User ROM	User ROM
Rewrite programs	User program	Standard boot program

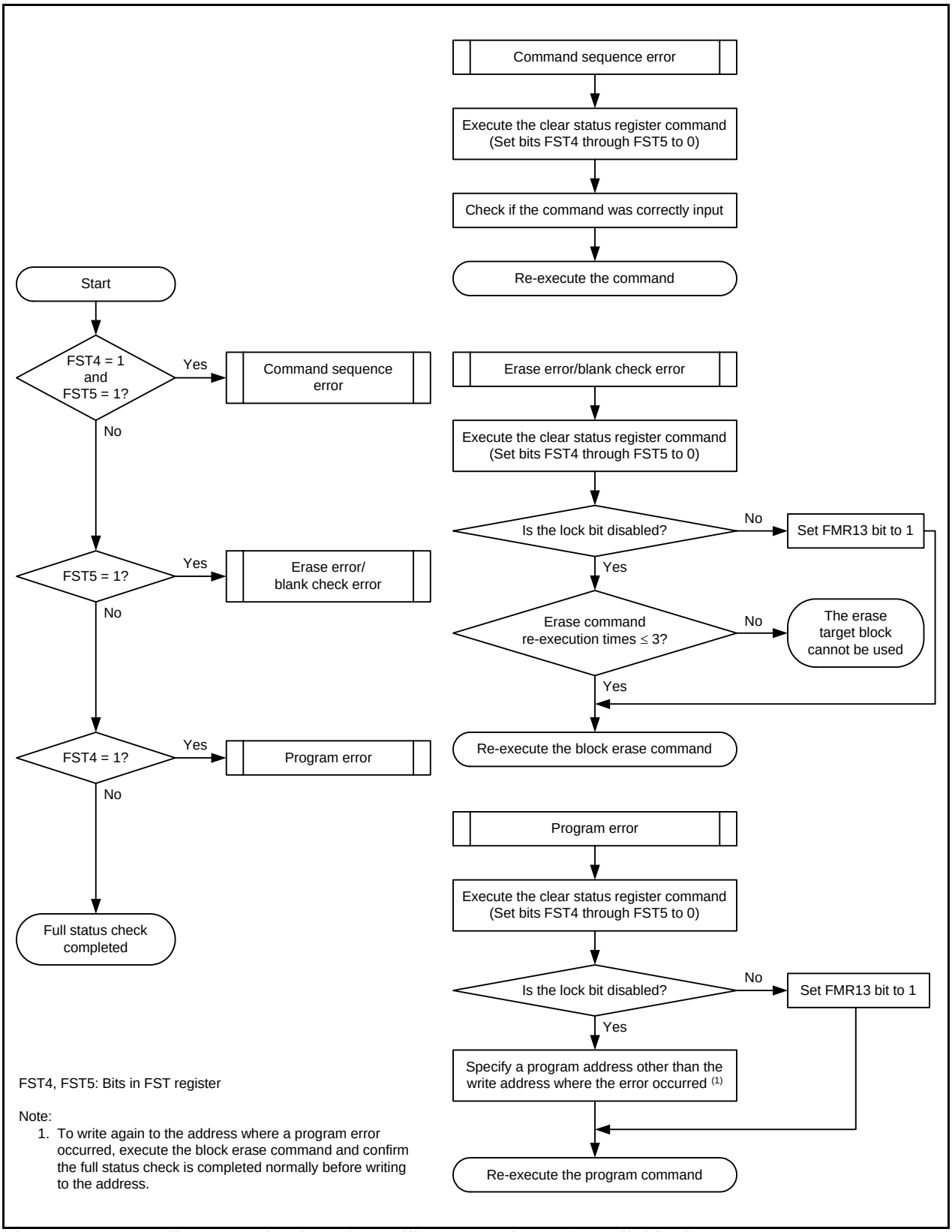


Figure 19.19 Full Status Check and Handling Procedures for Individual Errors

21.7 Notes on Timer RJ2

(1) Timer RJ2 stops counting after a reset. Start the count only after setting the value in the timer.

(2) After 1 (count is started) is written to the TSTART bit in the TRJCR register while the count is stopped, the TCSTF bit in the TRJCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started from the first active edge of the count source after the TCSTF bit is set to 1. After 0 (count is stopped) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 0.
Note:
1. Registers associated with timer RJ2: TRJ, TRJCR, TRJIOC, and TRJMR

(3) In event counter mode, set the TSTART bit in the TRJCR register to 1 (count is started) and then input an external pulse.

(4) In pulse width/pulse period measurement modes, bits TEDGF and TUNDF in the TRJCR register used are set to 0 by writing 0 by a program but remain unchanged even if 1 is written to these bits. If a read-modify-write instruction is used to set the TRJCR register, bits TEDGF and TUNDF may be erroneously set to 0 depending on the timing, even when the TEDGF bit is set to 1 (active edge received) and the TUNDF bit is set to 1 (underflow) during execution of the instruction.
In this case, write 1 using the MOV instruction to the TEDGF or TUNDF bit which is not supposed to be set to 0.

(5) Insert NOP instructions between writing to and reading from registers associated with the TRJ counter while the counter is stopped.

(6) When the TSTART bit in the TRJCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), allow at least three cycles of the count source clock for each write interval when writing to the TRJ register successively.

(7) Note the following when writing 0 to the TEDGF bit in the TRJCR register in pulse width measurement mode or pulse period measurement mode.
Set the TRJIF bit in the TRJIR register to 0 before setting the TEDGF bit to 0.
When reading the TEDGF bit immediately after setting it to 0, it is read as 0. However the internal signal of the TEDGF bit remains 1 for one to two cycles of the count source. If an active edge is input during this period, the internal signal of the TEDGF bit does not become 0 and the TEDGF bit is read as 1.
Since the TRJIF bit becomes 1 when the internal signal of the TEDGF bit changes from 0 to 1, the TRJIF bit does not become 1 and no interrupt is generated.
After setting the TEDGF bit to 0, confirm that 0 can be read after waiting for three or more count source cycles in order to accept the next interrupt request.

21.12 Notes on Flash Memory

21.12.1 ID Code Area Setting Example

The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

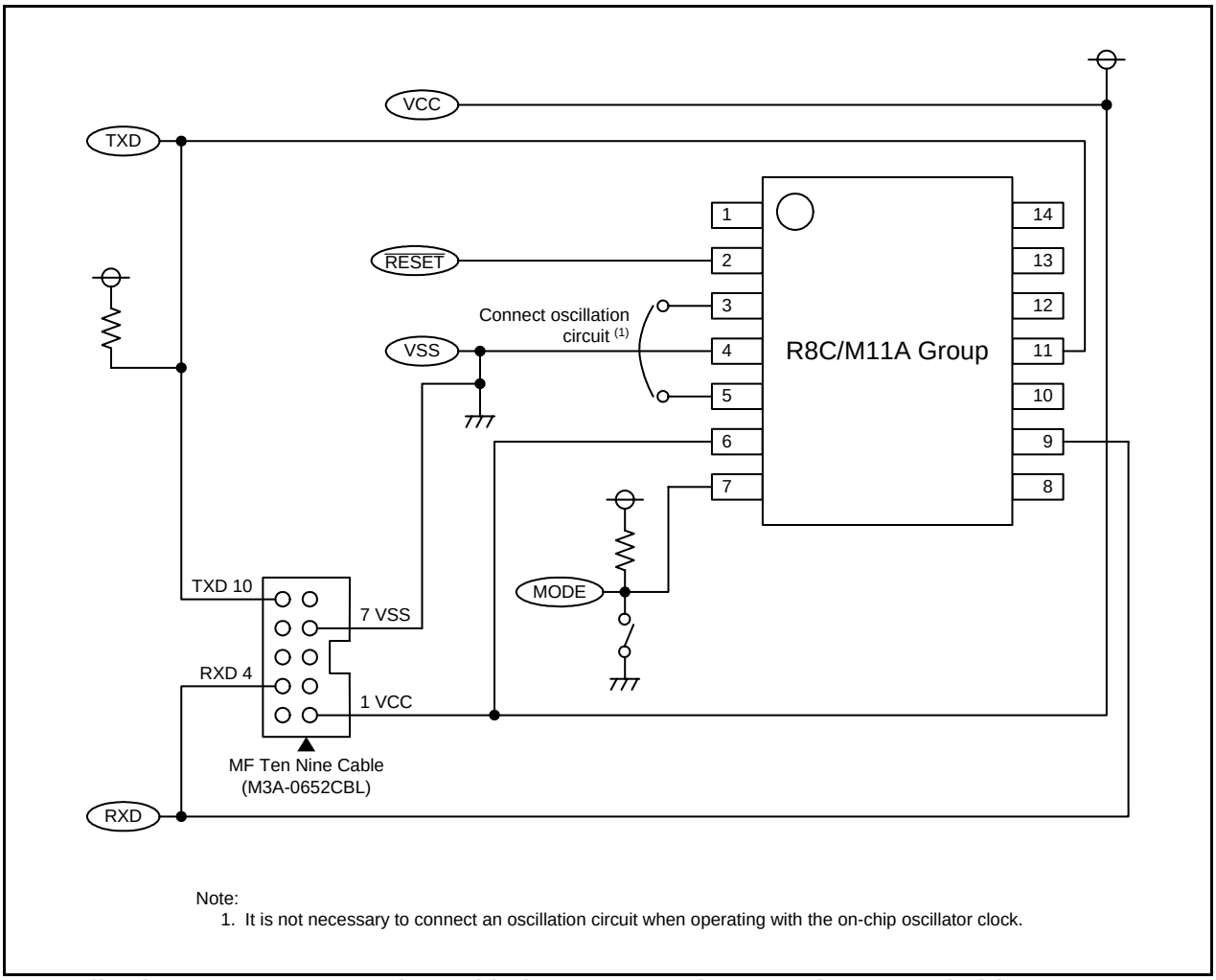
• To set 55h in all of the ID code area

```
  .org 00FFDCH
  .lword dummy | (55000000h)      ; UND
  .lword dummy | (55000000h)      ; INTO
  .lword dummy                    ; BREAK
  .lword dummy | (55000000h)      ; ADDRESS MATCH
  .lword dummy | (55000000h)      ; SET SINGLE STEP
  .lword dummy | (55000000h)      ; WDT
  .lword dummy | (55000000h)      ; RESERVE
  .lword dummy | (55000000h)      ; RESERVE
```

Programming formats vary depending on the compiler. Check the compiler manual.

Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator

Appendix Figures 2.1 and 2.2 show MF Ten Nine Cable (M3A-0652CBL) Connection Examples. Appendix Figures 2.3 and 2.4 show E8a Emulator (R0E00008AKCE00) Connection Examples.



Note:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.

Appendix Figure 2.1 MF Ten Nine Cable (M3A-0652CBL) Connection Example (1)