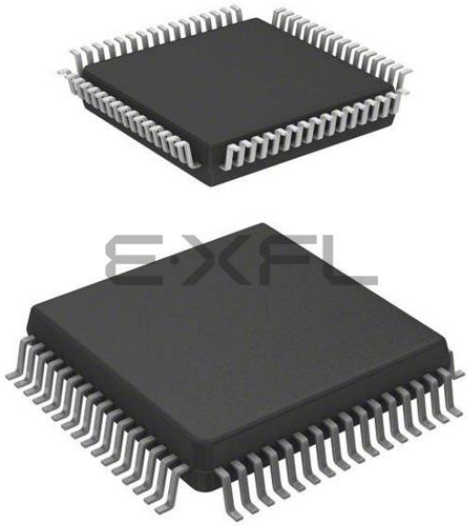


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36074lhv

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	—	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b3	—	Reserved	Set to 0.	W
b4	—			
b5	XXX5	XXX bits	Function varies depending on the operating mode.	R/W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2 *3

*1
R/W: Read and write.
R: Read only.
W: Write only.
—: Nothing is assigned.

*2
• Reserved
Reserved bits. Set to the specified value.

*3
• Nothing is assigned.
Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
• Do not set.
Operation is not guaranteed when a value is set.
• Function varies depending on the operating mode.
The function of the bit varies with the peripheral function mode. For information on the individual modes, see the register diagram.

9.2.6 Clock Control Register When Returning from Modes (CKRSCR)

Address 00025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	STOPRS	WAITRS	PHISRS	—	CKST3	CKST2	CKST1	CKST0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKST0	Clock oscillator circuit oscillation stabilization state select bits	Number of wait states b3 b2 b1 b0 0 0 0 0: 4 0 0 0 1: 16 0 0 1 0: 32 0 0 1 1: 64 0 1 0 0: 128 0 1 0 1: 256 0 1 1 0: 512 0 1 1 1: 1024 1 0 0 0: 2048 1 0 0 1: 4096 1 0 1 0: 8192 1 0 1 1: 16384 1 1 0 0: 32768 1 1 0 1: 65536 1 1 1 0: 131072 1 1 1 1: 262144	R/W
b1	CKST1			R/W
b2	CKST2			R/W
b3	CKST3			R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	PHISRS	CPU clock division select bit when returning from wait mode or stop mode	0: The value set in bits PHISSEL0 to PHISSEL2 in the SCKCR register is valid 1: No division	R/W
b6	WAITRS	System base clock select bit when returning from wait mode	0: Return using the system base clock used immediately before entering wait mode 1: fHSCK (1, 2)	R/W
b7	STOPRS	System base clock select bit when returning from stop mode	0: Return using the system base clock used immediately before entering stop mode 1: fHSCK (1, 2)	R/W

Notes:
1. When the HSCKSEL bit in the SCKCR register is 0 (XIN clock), set pins P4_6 and P4_7 to XIN oscillation by a program before entering wait mode or stop mode.
2. Set this bit to 0 before entering wait mode or stop mode if the FMR27 bit in the FMR2 register is set to 1 (low-current-consumption read mode enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CKRSCR register.

9.2.9 High-Speed On-Chip Oscillator 18.432 MHz Control Register 1 (FR18S1)

Address 00065h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

Bit	Function	R/W
b7 to b0	Frequency adjustment data for 18.432 MHz is stored. The frequency of the high-speed on-chip oscillator can be adjusted to 18.432 MHz by transferring this value to the FRV2 register and the adjustment value in the FR18S0 register to the FRV1 register.	R/W

9.2.10 High-Speed On-Chip Oscillator Control Register 1 (FRV1)

Address 00067h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

Bit	Function	R/W
b7 to b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 20 MHz: FRV1 = Value after reset, FRV2 = Value after reset 18.432 MHz: Transfer the value in the FR18S0 register to the FRV1 register and the value in the FR18S1 register to the FRV2 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRV1 register.

9.2.11 High-Speed On-Chip Oscillator Control Register 2 (FRV2)

Address 00068h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

Bit	Function	R/W
b7 to b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 20 MHz: FRV1 = Value after reset, FRV2 = Value after reset 18.432 MHz: Transfer the value in the FR18S0 register to the FRV1 register and the value in the FR18S1 register to the FRV2 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRV2 register.

Figure 10.1 shows the Power Control State Transition Diagram.

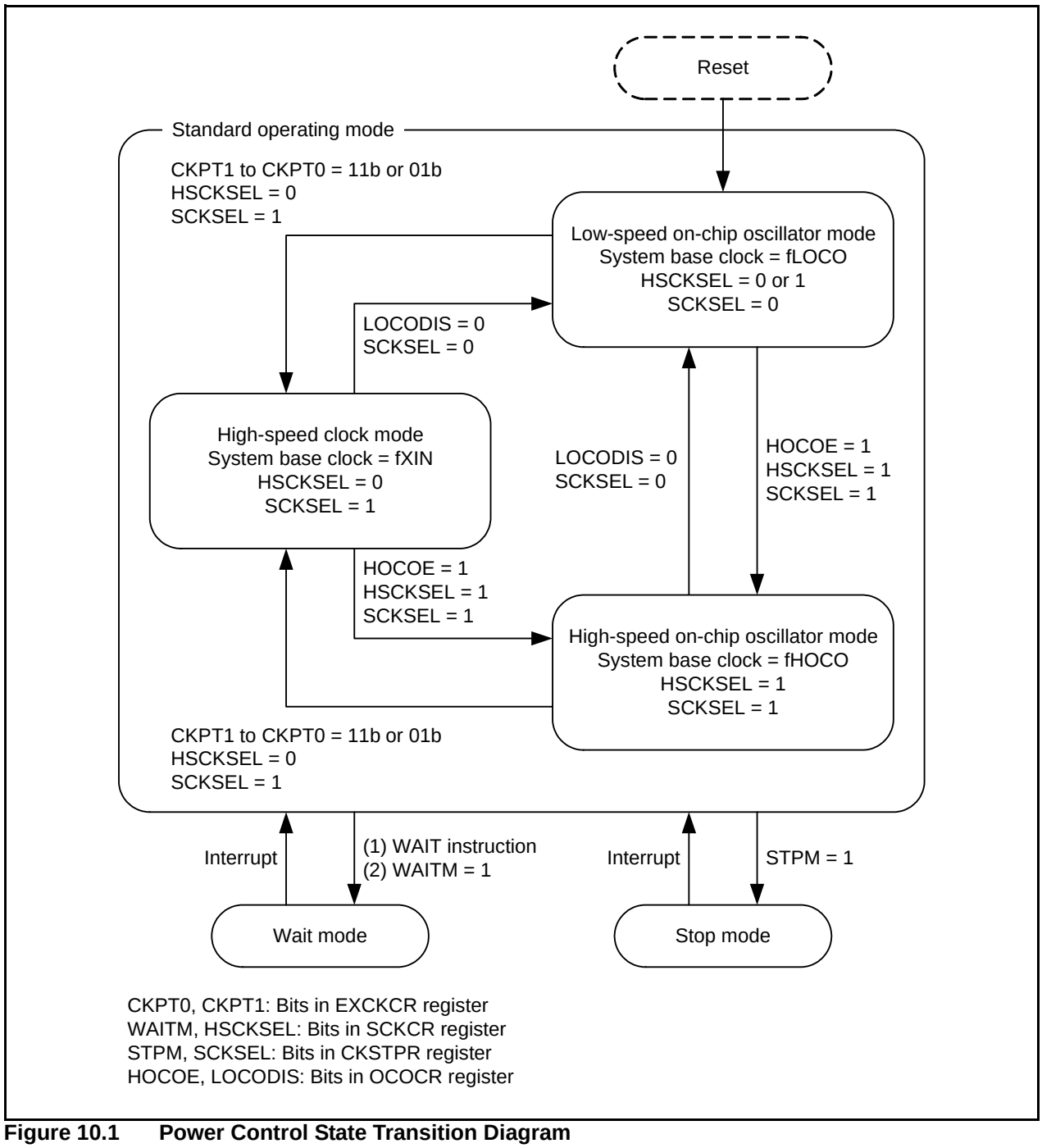


Figure 10.1 Power Control State Transition Diagram

10.2 Standard Operating Mode

In standard operating mode, the system clock is supplied to operate the CPU and the peripheral functions. Power consumption control is implemented by controlling the frequency of the system clock or CPU clock.
The higher the CPU clock frequency, the higher processing power. The lower the CPU clock frequency, the lower the power consumption. Stopping unnecessary oscillation circuits will further reduce power consumption.
When the clock sources for the CPU clock are switched, the new clock needs to be oscillating and stable. Assure the wait time for the new clock oscillation to stabilize by a program before switching the clocks.
Table 10.2 lists the Register Settings in Standard Operating Mode.

Table 10.2 Register Settings in Standard Operating Mode

Mode	Register	OCOCR		SCKCR	CKSTPR	EXCKCR	
	Bit	HOCOE	LOCODIS	HSCKSEL	SCKSEL	CKPT1	CKPT0
	Content to be Switched	fHOCO Oscillate/Stop	fLOCO Oscillate/Stop	XIN/fHOCO	fLOCO/ fHSCK	P4_6 and P4_7 Pin Function	
High-speed clock mode		—	—	0 (XIN)	1 (fHSCK)	1	1
High-speed on-chip oscillator mode		1 (oscillate)	—	1 (fHOCO)	1 (fHSCK)	—	—
Low-speed on-chip oscillator mode		—	0 (oscillate)	—	0 (fLOCO)	—	—

—: Indicates that either 0 or 1 can be set.
The setting in ( ) is selected.

10.2.1 High-Speed Clock Mode

When the HSCKSEL bit in the SCKCR register is 0 (XIN clock) and the SCKSEL bit in the CKSTPR register is 1 (fHSCK), the XIN clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the XIN clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fHOCO can be used as the peripheral function clock when the HOCOE bit in the OCOCR register is 1 (high-speed on-chip oscillator on), and fLOCO when the LOCODIS bit is 0 (low-speed on-chip oscillator on).

10.2.2 High-Speed On-Chip Oscillator Mode

When the HOCOE bit in the OCOCR register is 1 (high-speed on-chip oscillator on), the HSCKSEL bit in the SCKCR register is 1 (high-speed on-chip oscillator clock), and the SCKSEL bit in the CKSTPR register is 1 (fHSCK), the high-speed on-chip oscillator clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the high-speed on-chip oscillator clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fLOCO can be used as the peripheral function clock when the LOCODIS bit is 0 (low-speed on-chip oscillator on).

10.2.3 Low-Speed On-Chip Oscillator Mode

When the LOCODIS bit in the OCOCR register is 0 (low-speed on-chip oscillator on) and the SCKSEL bit in the CKSTPR register is 0 (fLOCO), the low-speed on-chip oscillator clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the low-speed on-chip oscillator clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fHOCO can be used as the peripheral function clock when the HOCOE bit in the OCOCR register is 1 (high-speed on-chip oscillator on).

In this mode, low-power operation can be enabled by stopping the XIN clock and the high-speed on-chip oscillator and setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). Furthermore, if wait mode is entered from this mode, power consumption in wait mode can be reduced even further by setting the VCA2 register LPE bit to 1 (low-power-consumption wait mode enabled).

For details on how to reduce power consumption, see **10.5 Reducing Power Consumption**.

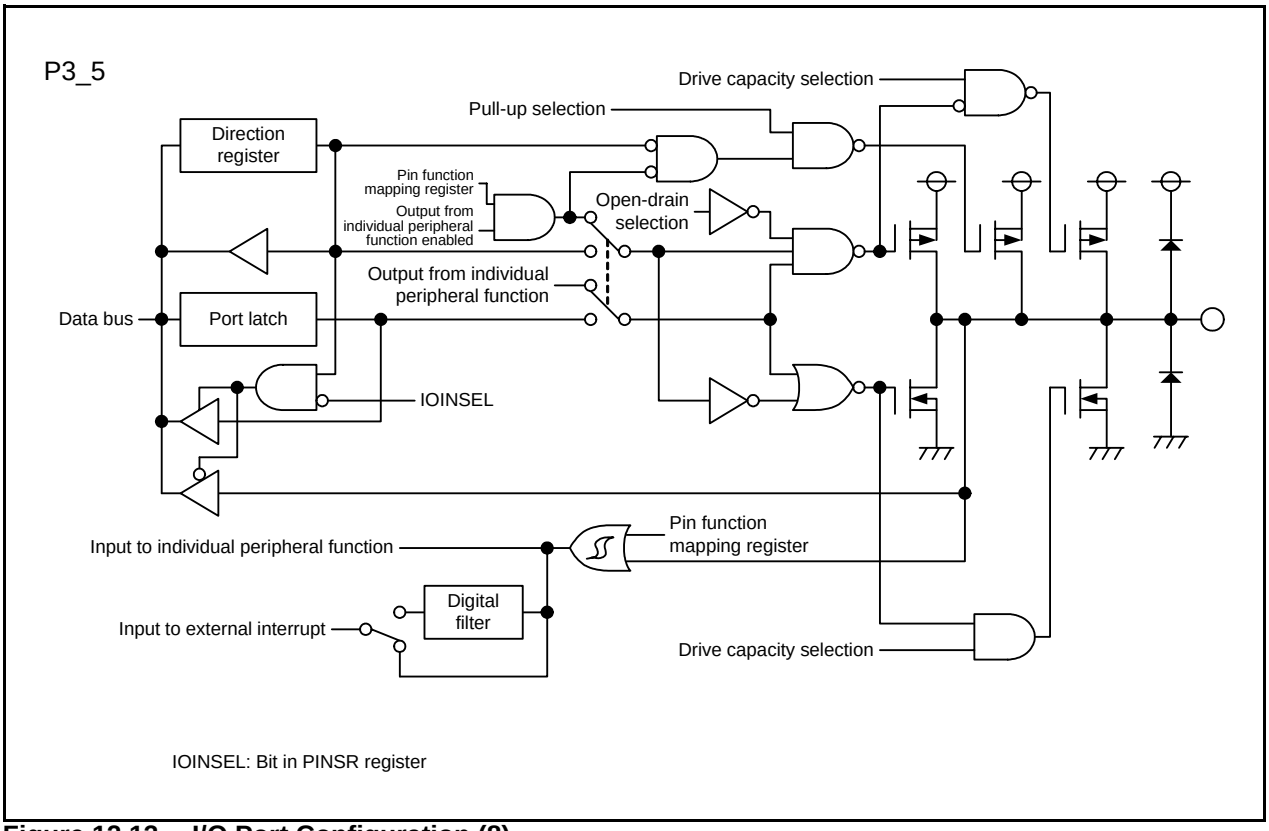


Figure 12.13 I/O Port Configuration (8)

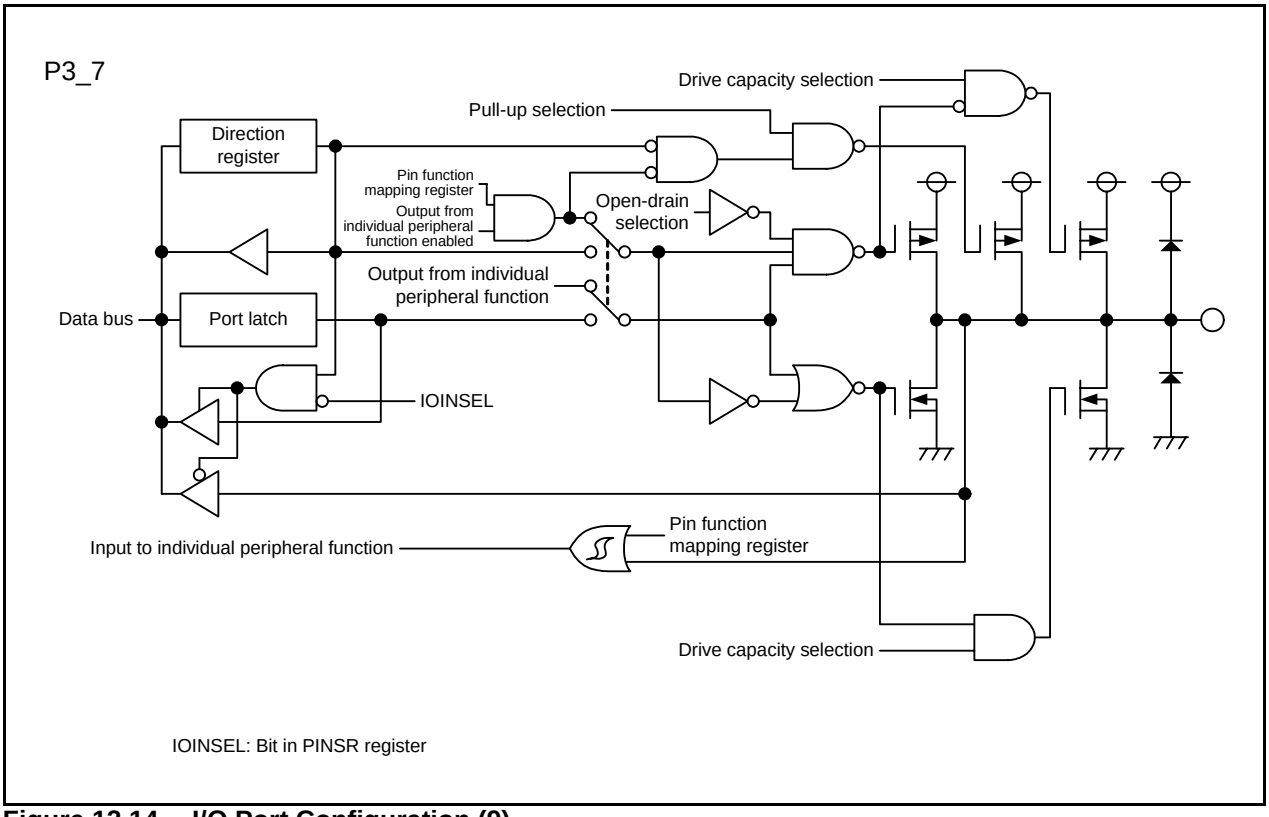


Figure 12.14 I/O Port Configuration (9)

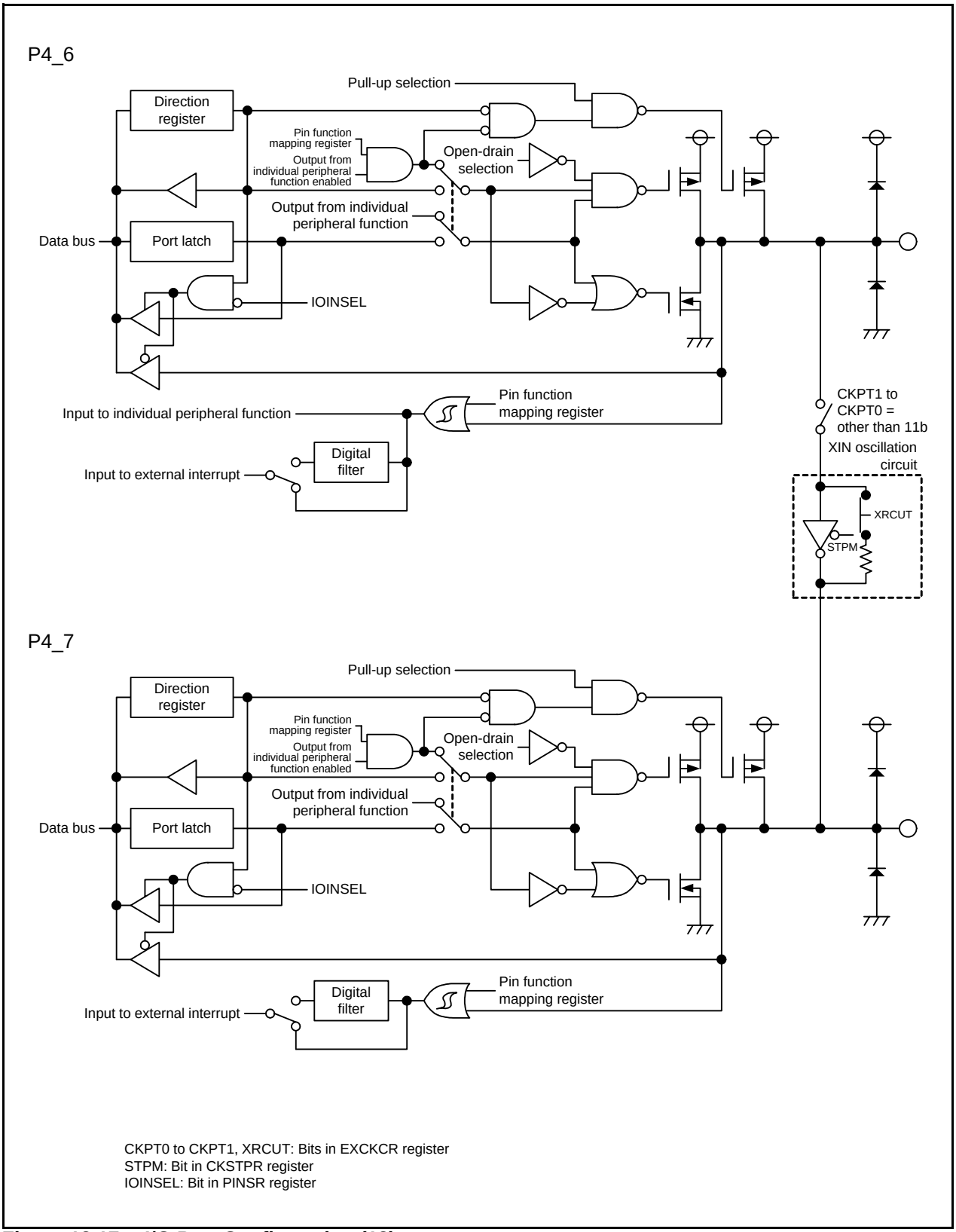


Figure 12.17 I/O Port Configuration (12)

15.2.10 Timer RC Digital Filter Function Select Register (TRCDF)

Address 000F9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA digital filter function bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB digital filter function bit (1)		R/W
b2	DFC	TRCIOC digital filter function bit (1)		R/W
b3	DFD	TRCIOD digital filter function bit (1)		R/W
b4	DFTRG	TRCTRG digital filter function bit (2)		R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	DFCK0	Digital filter clock select bits (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits CKS2 to CKS0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. Enabled in the input capture function.
2. Enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

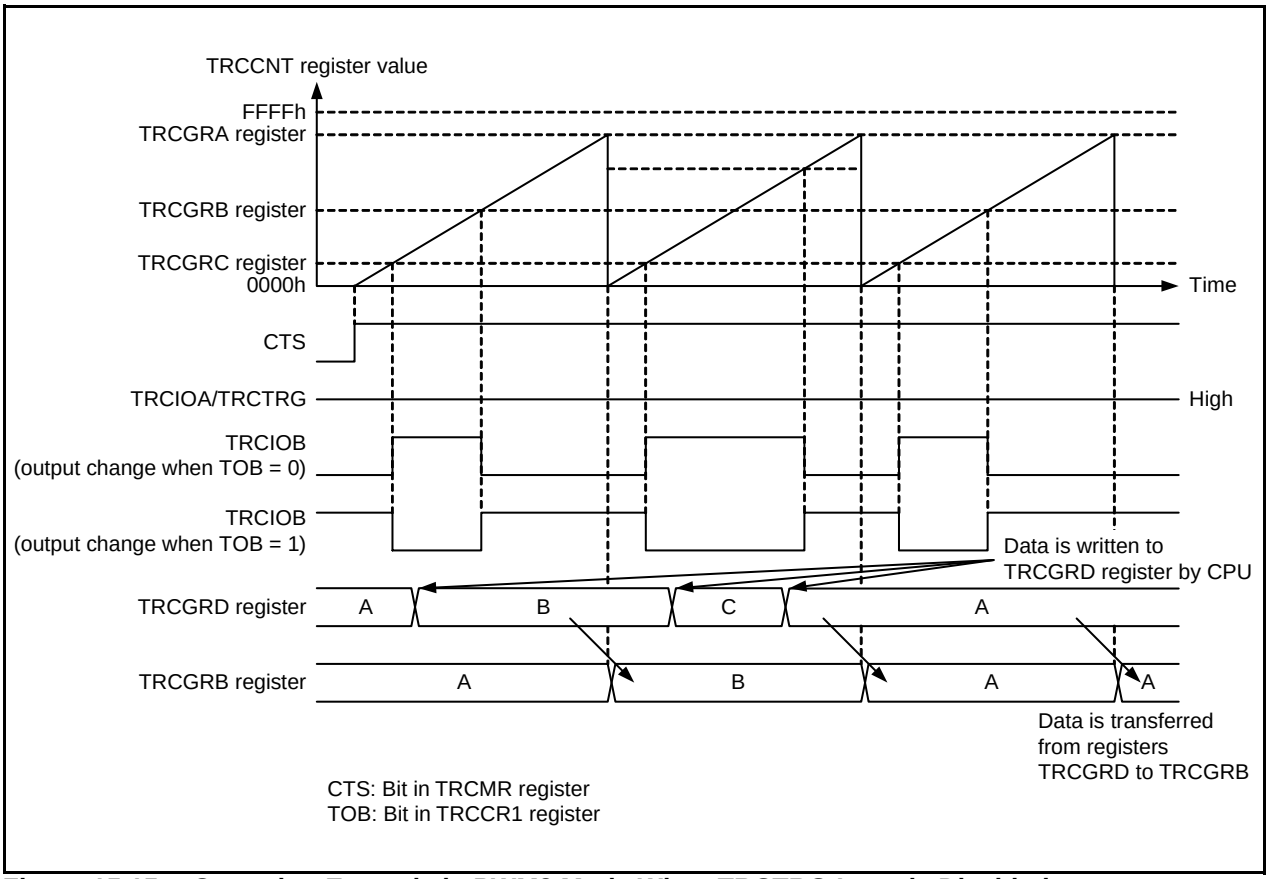


Figure 15.15 Operation Example in PWM2 Mode When TRCTRG Input is Disabled

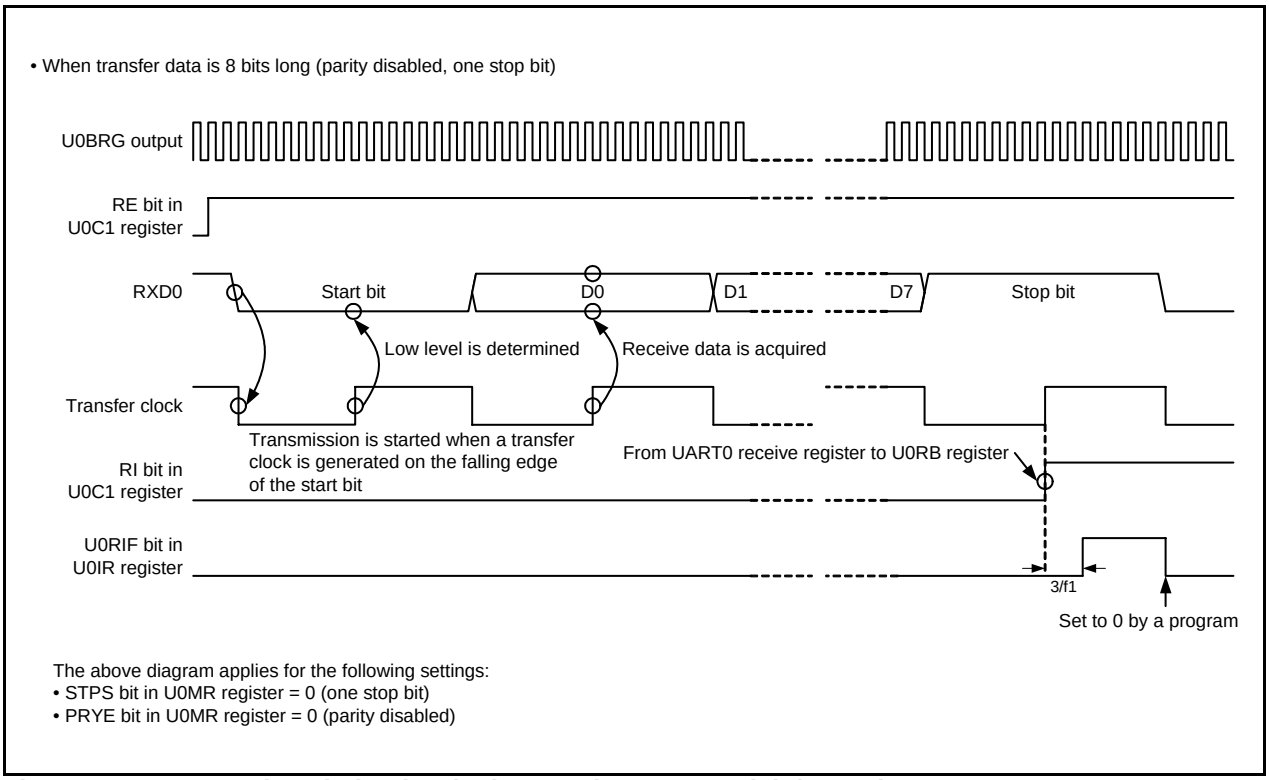


Figure 16.7 Receive Timing in Clock Asynchronous Serial I/O Mode

16.4 UART0 Interrupt

The UART0 interrupt requests are the transmit buffer empty or transmit complete interrupt, and the receive complete interrupt.
Table 16.9 lists the Interrupt Requests.

Table 16.9 Interrupt Requests

Interrupt Request	Interrupt Generation Condition
Transmit buffer empty	U0TIF = 1 (transmit interrupt requested) and U0TIE = 1 (transmit interrupt enabled)
Transmit complete	
Receive complete	U0RIF = 1 (receive interrupt requested) and U0RIE = 1 (receive interrupt enabled)

U0TIF, U0TIE, U0RIF, U0RIE: Bits in U0IR register
Note:
1. The CPU executes interrupt exception handling when the interrupt generation conditions are met and the I flag in the FLG register is 1.

17.3 Operation

This A/D converter provides operating four modes: One-shot, repeat, single sweep, and repeat sweep modes. This converter is a successive approximation type with 10-bit resolution.
The operating mode, analog input channel, and A/D conversion clock should be switched while the ADST bit in the ADCON0 register is 0 (A/D conversion stops).

17.3.1 Items Common to Multiple Modes

17.3.1.1 Input Sampling and A/D Conversion Time

The A/D converter includes a sample and hold circuit. When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts), the A/D converter samples the input and starts conversion after the A/D conversion start delay time (tD) has elapsed.
Figure 17.2 shows the A/D Conversion Timing. Table 17.6 lists the A/D Conversion Time.
As shown in Figure 17.2, the A/D conversion time (tCONV) includes tD and the input sampling time (tSPL). Here, tD is determined by the timing for writing to the ADCON0 register and is not a fixed value. The conversion time, therefore, varies within the range shown in Table 17.6.
In one-shot mode and single sweep mode, the ADF bit in the ADICSR register is set to 1 during end processing time, and the last A/D conversion result is stored in the ADi register.

- In one-shot mode
  A/D conversion time (tCONV) + end processing time (tEND)
- When two channels are selected in single sweep mode
  A/D conversion time (tCONV) + A/D conversion time (tCONV with no start delay time (tD) included) + end processing time (tEND)

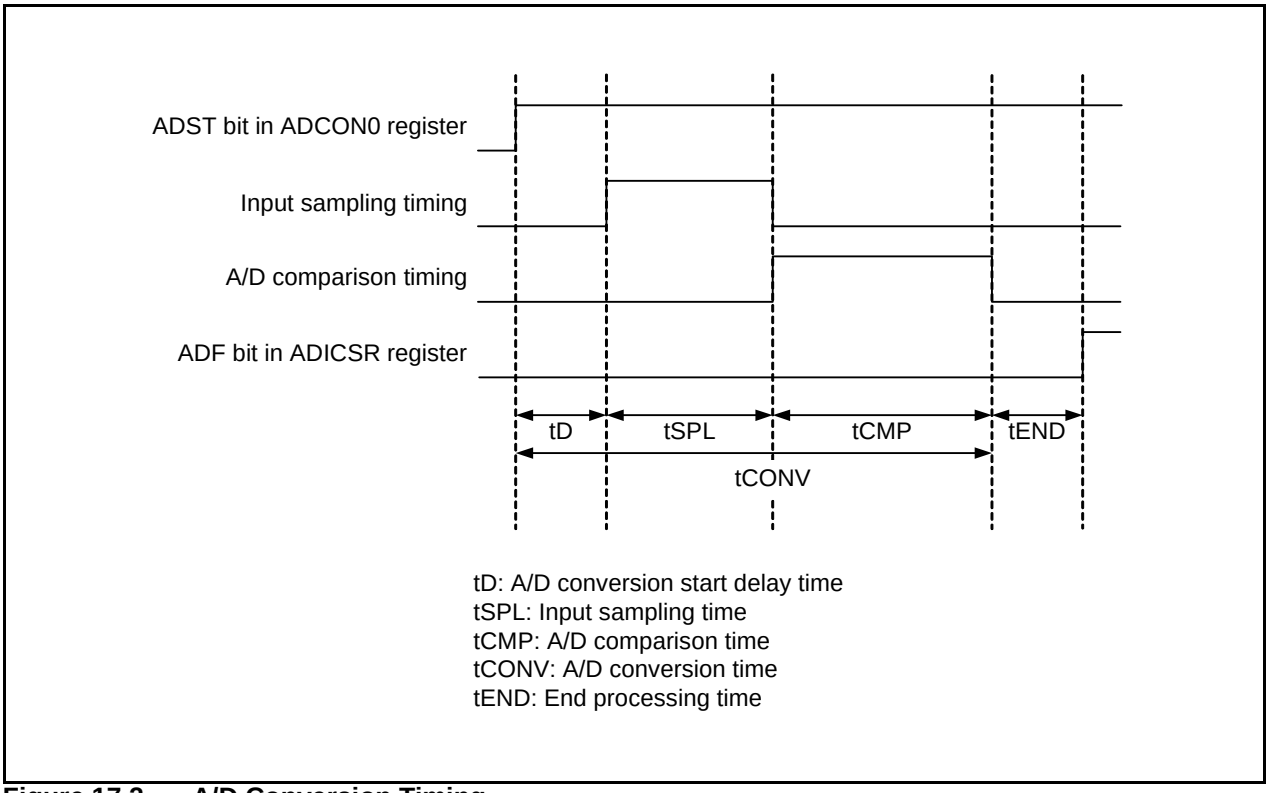


Figure 17.2 A/D Conversion Timing

19.6.7 Full Status Check

If an error occurs, bits FST4 to FST5 in the FST register are set to 1, indicating the occurrence of the error. The execution result can be confirmed by checking these status bits (full status check).
Table 19.9 lists the Errors and FST Register States. Figure 19.19 shows the Full Status Check and Handling Procedures for Individual Errors.

Table 19.9 Errors and FST Register States

FST Register States		Error	Error Occurrence Condition
FST5 Bit	FST4 Bit		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written as the second command of the block erase, lock bit program, read lock bit status, or block blank check command (1). • The erase command is executed during erase-suspend or the block blank check command is executed. • The program, lock bit program, erase, or block blank check command is executed during program-suspend. • The program, lock bit program, erase, or block blank check command is executed to the block during suspend. • The lock bit program or read lock bit status commands are executed to the data flash.
1	0	Erase error	When the block erase command is executed and auto-erase does not complete normally.
		Blank check error	When the block blank check command is executed and data other than the blank data, FFh, is read.
0	1	Program error	When the program command is executed and auto-programming does not complete normally.
		Lock bit program error	When the lock bit command is executed, but the lock bit is not set to 0 (locked).

Note:
1. When FFh is written as the second command of these commands, the MCU enters read array mode. At the same time, the command code written as the first command becomes invalid.

19.8.2.3 Access Methods

To set one of the following bits to 1, first write 0 and then 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
• The FMR01 or FMR02 bit in the FMR0 register
• The FMR13 bit in the FMR1 register
• The FMR20, FMR22, or FMR27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Interrupts must be disabled between writing 1 and then writing 0.
The FMR16 or FMR17 bit in the FMR1 register

19.8.2.4 Rewriting User ROM Area

When EW0 mode is used and the supply voltage falls while rewriting a block where a rewrite control program is stored, the rewrite control program is not be rewritten correctly. As a result, it may not be possible to rewrite the flash memory afterwards. Use standard serial I/O mode to rewrite this block.

19.8.2.5 Programming

Do not perform even a single additional write to an already programmed address.

19.8.2.6 Entering Wait Mode or Stop Mode

Do not enter wait mode or stop mode during suspend.
When the FST7 bit in the FST register is 0 (busy) while programming or erasing the flash memory, do not enter wait mode or stop mode.
Do not set the FMR27 bit to 1 while the FMSTP bit (flash memory stop bit) in the FMR0 register is 1 (flash memory is stopped).

19.8.2.7 Flash Memory Programming and Erase Voltages

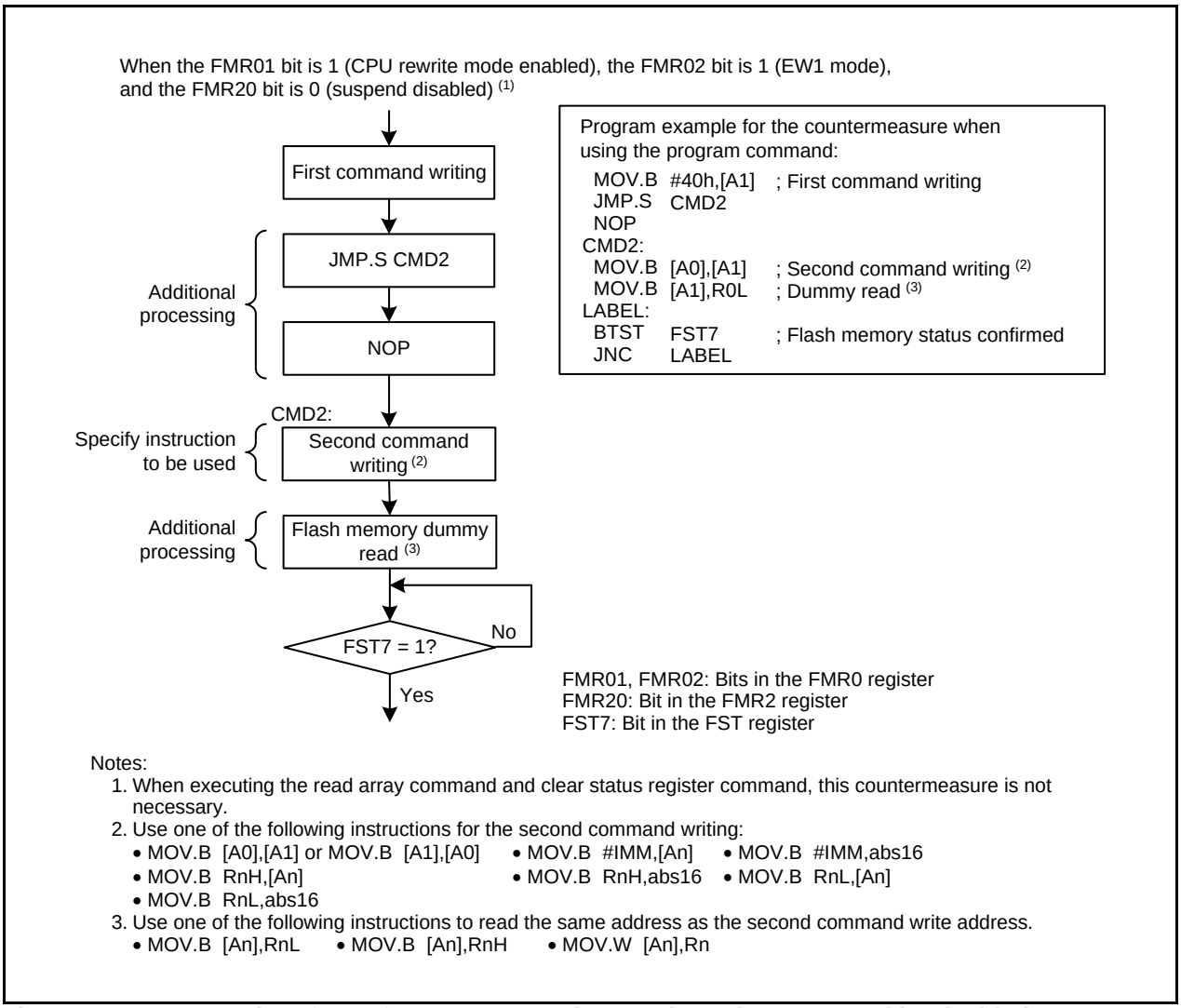
When performing a program/erase operation, use a VCC supply voltage in the range of 1.8 V to 5.5 V. Do not perform a program/erase operation at less than 1.8 V.

19.8.2.8 Block Blank Check

Do not execute a block blank check command during erase-suspend.

19.8.2.9 EW1 Mode

When setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled) and the FMR02 bit to 1 (EW1 mode) to execute CPU rewrite mode, follow the procedure below in EW1 mode. Figure 19.22 shows the Procedure for Software Command Execution When Suspend is Disabled. Figure 19.23 shows the Procedure for Software Command Execution When Suspend is Enabled.



Notes:
1. When executing the read array command and clear status register command, this countermeasure is not necessary.
2. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
3. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn

Figure 19.22 Procedure for Software Command Execution When Suspend is Disabled

Table 20.14 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition							Standard			Unit
			Oscillation Circuit	On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other				
			XIN (2)	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	125 kHz	No division	—		—	3	7.0	mA
			16 MHz	Off	125 kHz	No division	—		—	2.5	6.0	mA
			10 MHz	Off	125 kHz	No division	—		—	1.7	—	mA
			20 MHz	Off	125 kHz	Division by 8	—		—	1.5	—	mA
			16 MHz	Off	125 kHz	Division by 8	—		—	1.2	—	mA
			10 MHz	Off	125 kHz	Division by 8	—		—	1.0	—	mA
		High-speed on-chip oscillator mode	Off	20 MHz	125 kHz	No division			—	3.5	7.5	mA
			Off	20 MHz	125 kHz	Division by 8			—	2.0	—	mA
			Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	270	µA
		Wait mode	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	100	µA
			Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.0	90	µA
		Stop mode	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	µA
			Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.5	—	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 5.0 V
4. Set the system clock to 4 MHz with the PHISEL register.

Timing Requirements (Vcc = 5 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 20.15 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

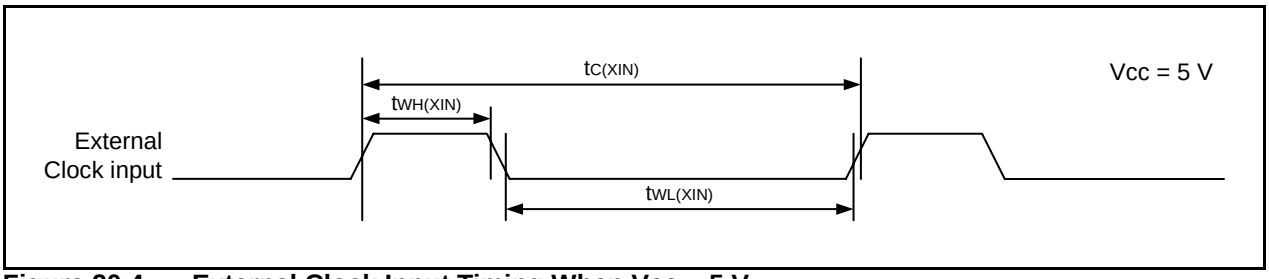


Figure 20.4 External Clock Input Timing When Vcc = 5 V

Table 20.16 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	100	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	40	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	40	—	ns

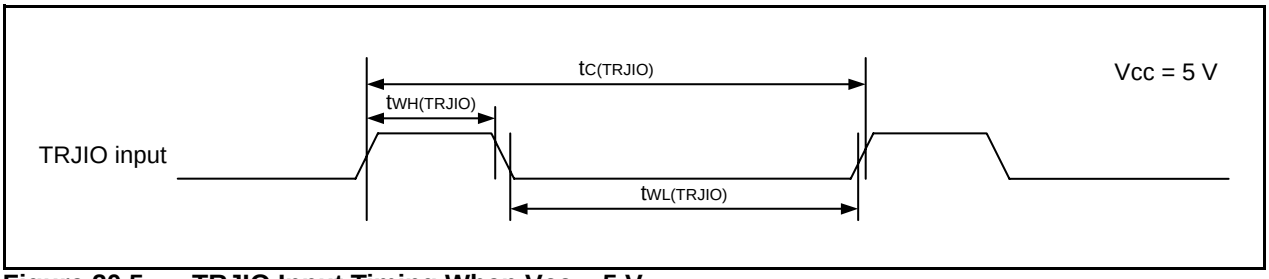


Figure 20.5 TRJIO Input Timing When Vcc = 5 V

21.13 Notes on Noise

21.13.1 Inserting a Bypass Capacitor between Pins VCC and VSS as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (approximately 0.1 μF) across pins VCC and VSS using the shortest and thickest possible wiring.

21.13.2 Countermeasures against Noise Error in Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.
As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may occur between the reset routine and interrupt routines.

21.14 Note on Power Supply Voltage Fluctuation

After a reset is cleared, the supply voltage applied to the VCC pin must meet either or both of the allowable ripple voltage Vr(vcc) and the ripple voltage falling gradient dVr(vcc)/dt shown in Figure 21.11.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
Vr(vcc)	Allowable ripple voltage			0.1 VCC	V
dVr(vcc)/dt	Ripple voltage falling gradient			10	V/ms

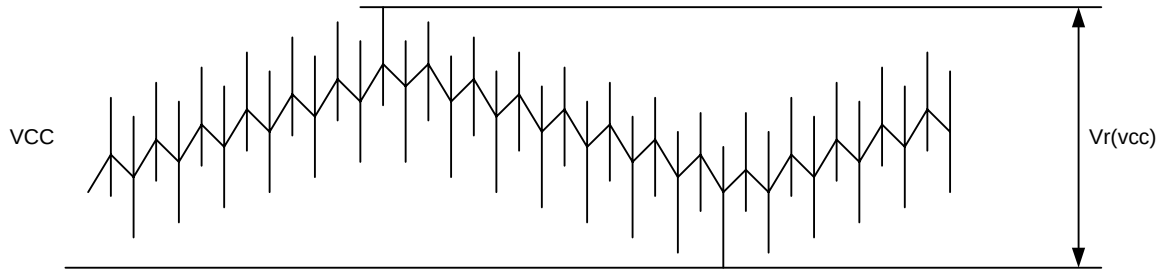


Figure 21.11 Ripple Voltage Definition