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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36077gfzv

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Address	Register Name	Symbol	Page
00180h	Comparator B Control Register	WCMPR	318
00181h	Comparator B1 Interrupt Control Register	WCB1INTR	319
00182h	Comparator B3 Interrupt Control Register	WCB3INTR	320
00183h			
00184h			
00185h			
00186h			
00187h			
00188h			
00189h			
0018Ah			
0018Bh			
0018Ch			
0018Dh			
0018Eh			
0018Fh			
00190h			
00191h			
00192h			
00193h			
00194h			
00195h			
00196h			
00197h			
00198h			
00199h			
0019Ah			
0019Bh			
0019Ch			
0019Dh			
0019Eh			
0019Fh			
001A0h			
001A1h			
001A2h			
001A3h			
001A4h			
001A5h			
001A6h			
001A7h			
001A8h			
001A9h	Flash Memory Status Register	FST	330
001AAh	Flash Memory Control Register 0	FMR0	333
001ABh	Flash Memory Control Register 1	FMR1	335
001ACh	Flash Memory Control Register 2	FMR2	336
001ADh	Flash Memory Refresh Control Register	FREFR	338
001AEh			
001AFh			
001B0h			
001B1h			
001B2h			
001B3h			
001B4h			
001B5h			
001B6h			
001B7h			
001B8h			
001B9h			
001BAh			
001BBh			
001BCh			
001BDh			
001BEh			
001BFh			

Note:
1. The blank areas are reserved. No access is allowed.

Address	Register Name	Symbol	Page
001C0h	Address Match Interrupt Register 0	AIADR0L	119
001C1h		AIADR0M	
001C2h		AIADR0H	
001C3h	Address Match Interrupt Enable Register 0	AIEN0	119
001C4h	Address Match Interrupt Register 1	AIADR1L	119
001C5h		AIADR1M	
001C6h		AIADR1H	
001C7h	Address Match Interrupt Enable Register 1	AIEN1	119
001C8h			
001C9h			
001CAh			
001CBh			
001CCh			
001CDh			
001CEh			
001CFh			
001D0h			
001D1h			
001D2h			
001D3h			
001D4h			
001D5h			
001D6h			
001D7h			
001D8h			
001D9h			
001DAh			
001DBh			
001DCh			
001DDh			
001DEh			
001DFh			
001E0h			
001E1h			
001E2h			
001E3h			
001E4h			
001E5h			
001E6h			
001E7h			
001E8h			
001E9h			
001EAh			
001EBh			
001ECh			
001EDh			
001EEh			
001EFh			
001F0h			
001F1h			
001F2h			
001F3h			
001F4h			
001F5h			
001F6h			
001F7h			
001F8h			
001F9h			
001FAh			
001FBh			
001FCh			
001FDh			
001FEh			
001FFh			
:			
0FFDBh	Option Function Select Register 2	OFS2	31, 40
:			
0FFFFh	Option Function Select Register	OFS	32, 41

Table 3.8 SFR Information (8) (1)

Address	Register Name	Symbol	After Reset
001C0h	Address Match Interrupt Register 0	AIADR0L	00h
001C1h		AIADR0M	00h
001C2h		AIADR0H	00h
001C3h	Address Match Interrupt Enable Register 0	AIEN0	00h
001C4h	Address Match Interrupt Register 1	AIADR1L	00h
001C5h		AIADR1M	00h
001C6h		AIADR1H	00h
001C7h	Address Match Interrupt Enable Register 1	AIEN1	00h
001C8h			
001C9h			
001CAh			
001CBh			
001CCh			
001CDh			
001CEh			
001CFh			
001D0h			
001D1h			
001D2h			
001D3h			
001D4h			
001D5h			
001D6h			
001D7h			
001D8h			
001D9h			
001DAh			
001DBh			
001DCh			
001DDh			
001DEh			
001DFh			
001E0h			
001E1h			
001E2h			
001E3h			
001E4h			
001E5h			
001E6h			
001E7h			
001E8h			
001E9h			
001EAh			
001EBh			
001ECh			
001EDh			
001EEh			
001EFh			
001F0h			
001F1h			
001F2h			
001F3h			
001F4h			
001F5h			
001F6h			
001F7h			
001F8h			
001F9h			
001FAh			
001FBh			
001FCh			
001FDh			
001FEh			
001FFh			

Note:
1. The blank areas are reserved. No access is allowed.

6.3.4 Voltage Monitor 0 Reset

The voltage monitor 0 reset is due to the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the voltage applied to the VCC pin. Vdet0 is the detection level. The Vdet0 level is set with bits VDSEL0 to VDSEL1 in the OFS register.

When the input voltage to the VCC pin falls to the Vdet0 level or lower, the CPU, SFRs and I/O ports are initialized. The internal RAM is not initialized. If the supply voltage falls to Vdet0 or lower while writing to the internal RAM, the RAM values will be undefined.

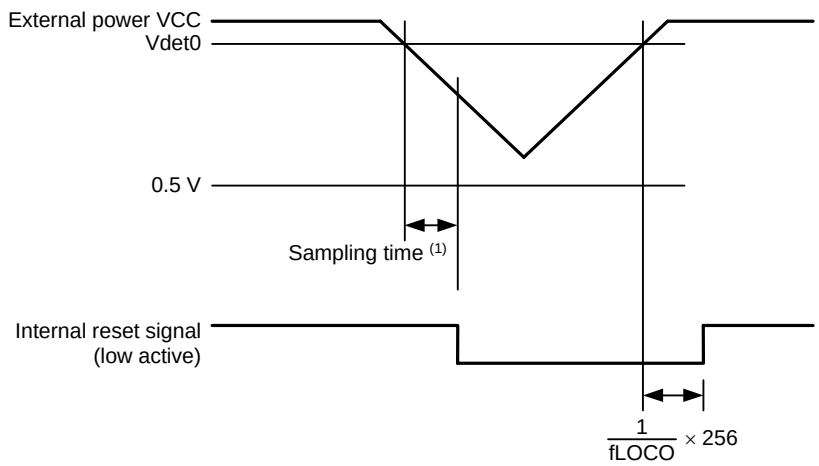
When the voltage applied to the VCC pin next rises to the Vdet0 level or higher, counting of the low-speed on-chip oscillator clock starts. When the low-speed on-chip oscillator clock count reaches 256, the internal reset signal goes high and the MCU proceeds to the reset sequence (see Figure 6.2). The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset.

The LVDAS bit in the OFS register can be used to enable or disable the voltage monitor 0 reset after a reset. The setting of the LVDAS bit is valid at all resets.

Bits VDSEL0 to VDSEL1, and LVDAS cannot be changed by a program. To change these bits, write values to b4 to b6 at address 0FFFFh using a flash programmer. For details on the OFS register, see **6.2.4 Option Function Select Register (OFS)**.

For details on the voltage monitor 0 reset, see **7. Voltage Detection Circuit**.

Figure 6.5 shows an Example of Voltage Monitor 0 Reset Operation.



Note:
1. The voltage monitor 0 digital filter samples VCC to monitor the voltage. If VCC falls below the operating voltage range (1.8 V or more), the voltage cannot be correctly measured. This factor should be considered when selecting the sampling clock for the digital filter. For details, see **7. Voltage Detection Circuit**.

Figure 6.5 Example of Voltage Monitor 0 Reset Operation

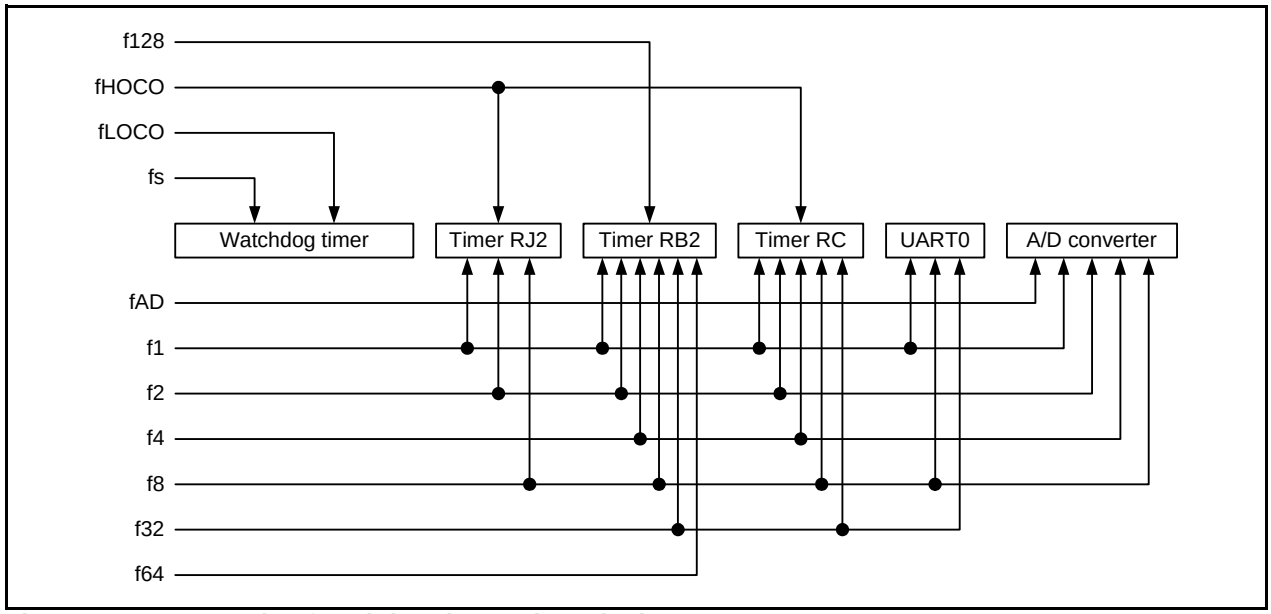


Figure 9.2 Supply of Peripheral Function Clocks

Table 9.2 Clock Generation Circuit Pin Configuration

Pin Name	I/O	Function
XIN	I	XIN clock input/external clock input
XOUT	O	XIN clock output

9.4 Clocks

9.4.1 System Base Clock (fBASE)

The system base clock is selected from the XIN clock oscillation circuit, high-speed on-chip oscillator, or low-speed on-chip oscillator to operate the MCU.
After a reset, the MCU operates using the on-chip oscillator clock in standard mode.

9.4.2 System Clock (f)

The system clock is obtained by dividing the system base clock by any value from 1 to 256, set by bits PHISEL0 to PHISEL7 in the PHISEL register. After a reset is cleared, the low-speed on-chip oscillator clock (no division) is used as the system clock.

9.4.3 CPU Clock (fs)

The CPU clock can be obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32 for CPU operation. The frequency division ratio for the system clock is set by bits PHISSEL0 to PHISSEL2 in the SCKCR register. After a reset is cleared, the low-speed on-chip oscillator clock (no division) will be the CPU clock.

9.4.4 Various Clocks

Table 9.8 lists the Names and Descriptions of Various Clocks that can be generated in the clock generation circuit.

Table 9.8 Names and Descriptions of Various Clocks

Clock Name	Description
Peripheral function clocks f1 to f128	Clocks for the peripheral functions. These clocks are generated by dividing the system clock. They are used in timer RJ2, timer RB2, timer RC, UART0, or the A/D converter. The peripheral function clocks are stopped when wait mode is entered after the WCKSTP bit in the CKSTPR register is set to 1 (system clock stopped in wait mode).
fHOCO	fHOCO is generated by the high-speed on-chip oscillator, and oscillates when the HOCOE bit in the OCOCR register is set to 1. fHOCO is not stopped in wait mode.
fLOCO	fLOCO is generated by the low-speed on-chip oscillator, and oscillates when the LOCODIS bit in the OCOCR register is set to 0. fLOCO is not stopped in wait mode.
fHSCK	fHSCK is selected from the XIN clock or high-speed on-chip oscillator clock using the HSCKSEL bit in the SCKCR register.
fAD	A clock for the A/D converter. This clock is obtained by dividing the system clock. fAD is not stopped in wait mode.

Figure 10.1 shows the Power Control State Transition Diagram.

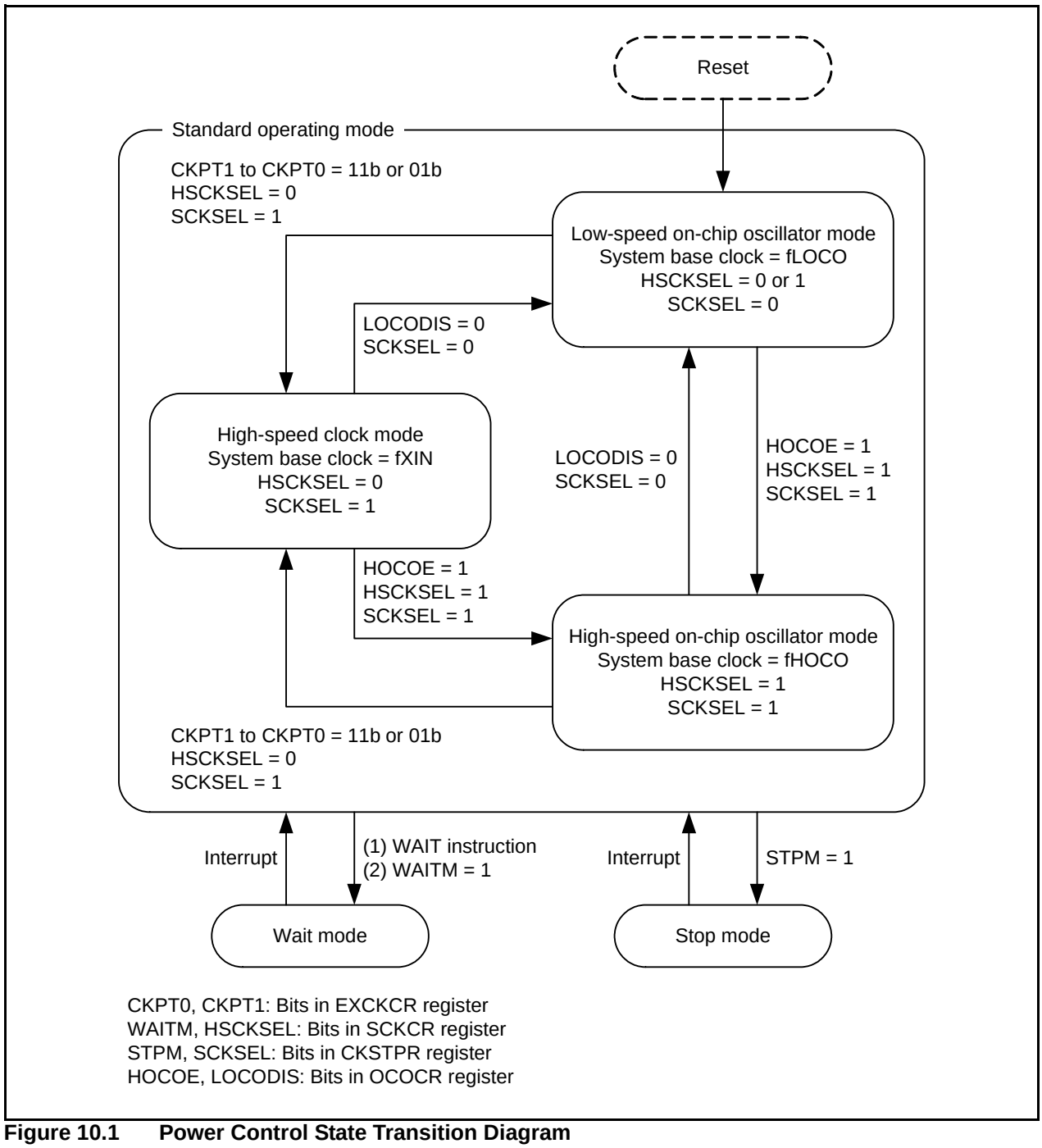


Figure 10.1 Power Control State Transition Diagram

The system base clock when returning from wait mode by a peripheral interrupt is the clock set by the WAITRS bit in the CKRSCR register. At this time, bits PHISSEL0 to PHISSEL2 in the SCKCR register and the SCKSEL bit in the CKSTPR register are automatically changed according to bits PHISRS and WAITRS.
If the system base clock when returning is different from the clock used immediately before entering wait mode, a period until the clock supply (oscillation stabilization time) is generated automatically. If the system base clock when returning is the high-speed on-chip oscillator clock, oscillation is started when an interrupt request is generated. If the system base clock is the XIN clock, set pins P4_6 and P4_7 to XIN oscillation by a program to start oscillation before entering wait mode.
Depending on the clock to be used, set appropriate values for oscillation stabilization time using bits CKST0 to CKST3 in the CKRSCR register. It is unnecessary to generate a wait time by a program. When returning from wait mode using the same clock as the one used immediately before entering the mode, no oscillation stabilization time is generated.

FMR0 Register FMSTP Bit	FMR1 Register WTFMSTP Bit	VCA2 Register LPE Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Clock Stabilization Time (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	1 (flash memory is stopped in wait mode)	0 (low-power-consumption wait mode disabled)	0 µs	60 µs (max.)	Set by bits CKST0 to CKST3 in the CKRSCR register if the clocks are switched when returning from wait mode 0 if the clocks are not switched when returning from wait mode	CPU clock period × 2 cycles	CPU clock period × 20 cycles	The total on the left amounts to the time from wait mode until execution of an interrupt routine.
		1 (low-power-consumption wait mode enabled)	100 µs (max.)					
1 (flash memory is stopped)	—	0 (low-power-consumption wait mode disabled)	0 µs	— (Flash memory is not activated)				
		1 (low-power-consumption wait mode enabled)	100 µs (max.)					
0 (flash memory operates)	0 (flash memory operates in wait mode)	0 (low-power-consumption wait mode disabled)	0 µs					
		1 (low-power-consumption wait mode enabled)	—					Setting prohibited

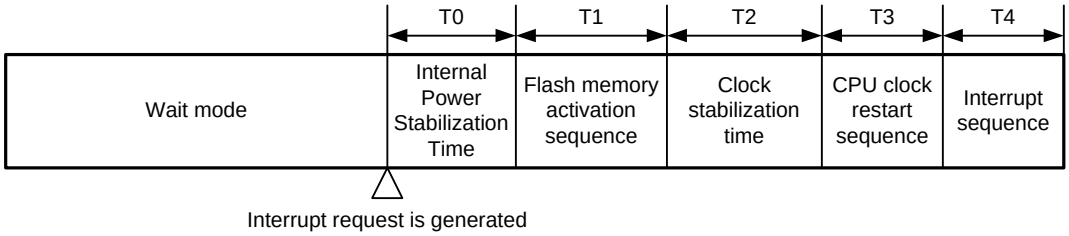


Figure 10.2 Sequence from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

11.5 $\overline{\text{INT}}$ Interrupt

11.5.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 3)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity can be selected by bits INTiSA to INTiSB in the ISCR0 register. The input pins used as the $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ input can be selected.
Inputs can be passed through a digital filter with three different sampling clocks.
The interrupt by the $\overline{\text{INTi}}$ input can be used as a wakeup function to cancel wait mode or stop mode.
Table 11.11 lists the Pin Configuration for $\overline{\text{INTi}}$ Interrupt.

Table 11.11 Pin Configuration for $\overline{\text{INTi}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P1_4, P4_5	I	$\overline{\text{INT0}}$ interrupt input
$\overline{\text{INT1}}$	P1_5, P1_7, P4_6	I	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P3_4, P4_7	I	$\overline{\text{INT2}}$ interrupt input
$\overline{\text{INT3}}$	P3_3	I	$\overline{\text{INT3}}$ interrupt input

12.3.7 Port 1 Function Mapping Register 1 (PMH1)

Address 000C9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P17SEL1	P17SEL0	P16SEL1	P16SEL0	P15SEL1	P15SEL0	P14SEL1	P14SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P14SEL0	Port P1_4 function select bits	bx b1 b0 0 0 0: I/O port or AN4 input 0 0 1: TXD0 0 1 0: RXD0 0 1 1: INT0 1 0 0: TRCIOB Other than the above: Do not set. (bx: P14SEL2 bit in the PMH1E register)	R/W
b1	P14SEL1			R/W
b2	P15SEL0	Port P1_5 function select bits	bx b3 b2 0 0 0: I/O port 0 0 1: RXD0 0 1 0: TRJIO 0 1 1: INT1 1 0 0: VCOUT1 Other than the above: Do not set. (bx: P15SEL2 bit in the PMH1E register)	R/W
b3	P15SEL1			R/W
b4	P16SEL0	Port P1_6 function select bits	b5 b4 0 0: I/O port or IVREF1 input 0 1: CLK0 1 0: TRJO 1 1: TRCIOB	R/W
b5	P16SEL1			R/W
b6	P17SEL0	Port P1_7 function select bits	b7 b6 0 0: I/O port or AN7 input or IVCMP1 input 0 1: INT1 1 0: TRJIO 1 1: TRCCLK	R/W
b7	P17SEL1			R/W

The PMH1 register is used to select the functions of pins P1_4 to P1_7.

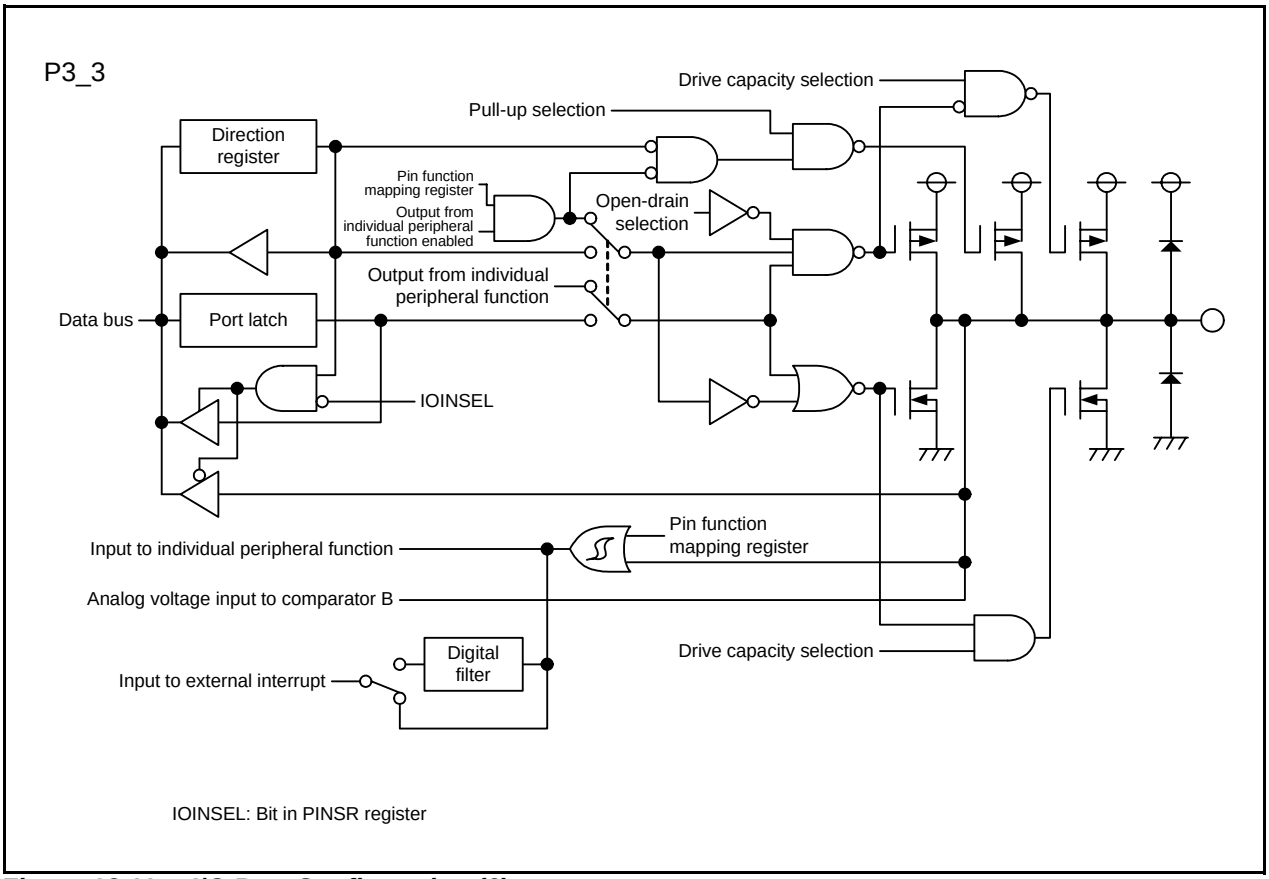


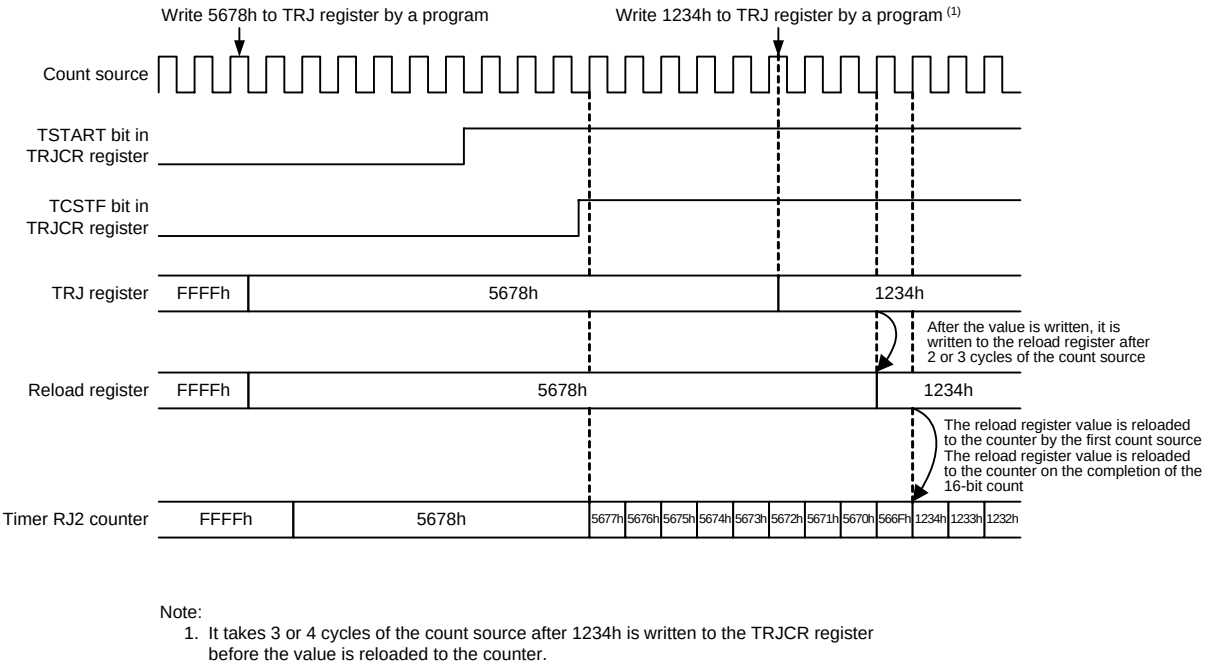
Figure 12.11 I/O Port Configuration (6)

13.4 Operation

13.4.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value in the TSTART bit in the TRJCR register. When the TSTART bit is 0 (count is stopped), the count value is directly written to the reload register, and then to the counter in synchronization with the system clock (f). When the TSTART bit is 1 (count is started), the value is written to the reload register in synchronization with the count source after two or three cycles, and then to the counter in synchronization with the next count source.

Figure 13.2 shows the Timing of Rewrite Operation with TSTART Bit Value.



Note:
1. It takes 3 or 4 cycles of the count source after 1234h is written to the TRJCR register before the value is reloaded to the counter.

Figure 13.2 Timing of Rewrite Operation with TSTART Bit Value

14.4 Operation

14.4.1 Timer Mode

In this mode, an internally generated count source or the timer RJ2 underflow is counted. Registers TRBOCR and TRBSC are not used.

When 1 (count is started) is written to the TSTART bit in the TRBCR register, the count is started after the count source is sampled three times. When 0 (count is stopped) is written to the TSTART bit, the count is stopped after the count source is sampled three times. When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped. The actual count state should be monitored with the TCSTF bit in the TRBCR register.

An interrupt request is generated when timer RB2 underflows.

When registers TRBPRE and TRBPR are read, each count value can be read. When registers TRBPRE and TRBPR are written to while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to both the reload register and counter. When the TWRC bit is 1, values are written to the reload register only.

Figure 14.2 shows an Operation Example in Timer Mode.

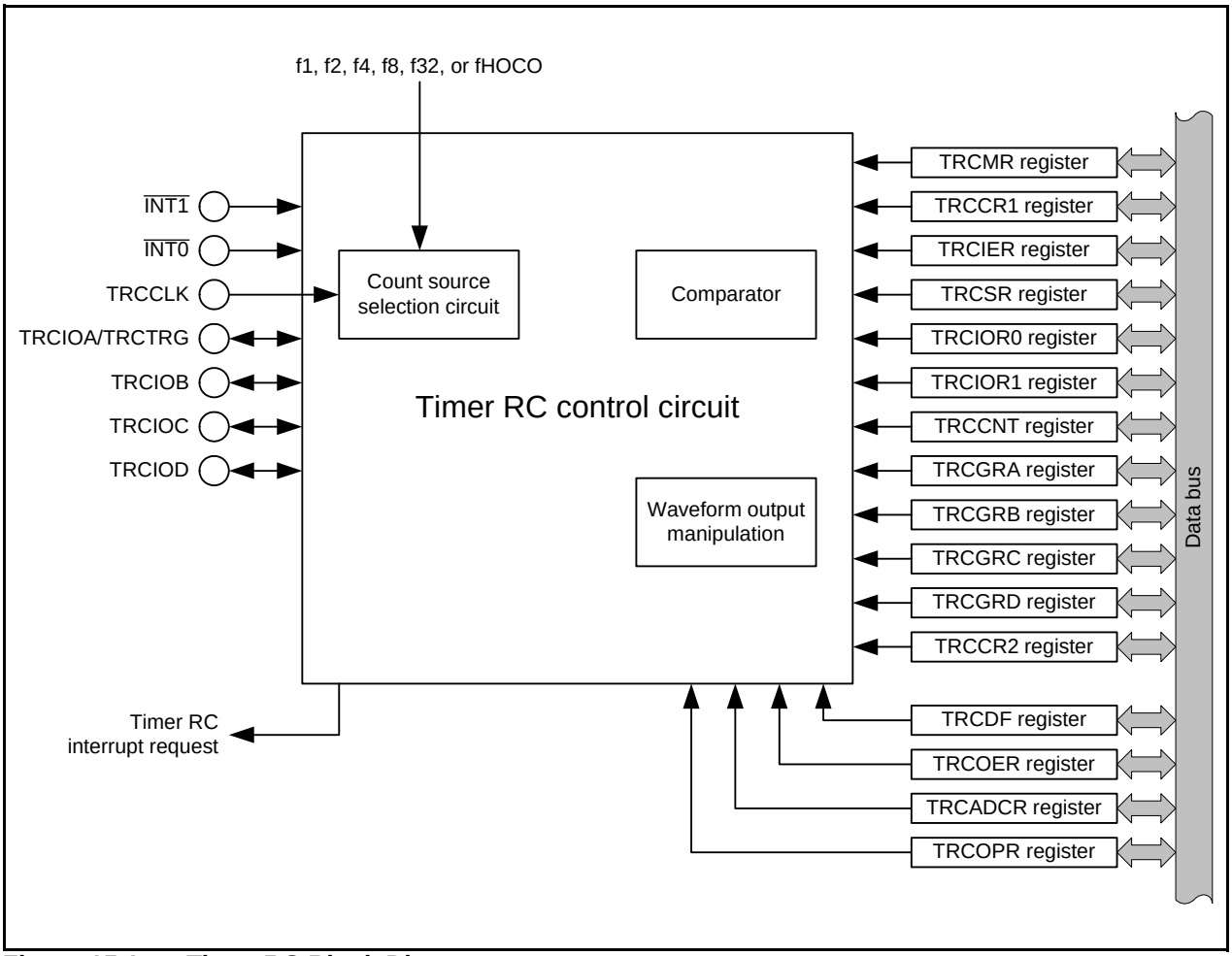


Figure 15.1 Timer RC Block Diagram

Table 15.3 Timer RC Pin Configuration

Pin Name	I/O	Function
TRCCLK	I	External clock input
TRCIOA/TRCTRG	I/O	TRCGRA output compare output/TRCGRA input capture input/external trigger input (TRCTRG)
TRCIOB	I/O	TRCGRB output compare output/TRCGRB input capture input/PWM output (in PWM mode)
TRCIOC	I/O	TRCGRC output compare output/TRCGRC input capture input/PWM output (in PWM mode)
TRCIOD	I/O	TRCGRD output compare output/TRCGRD input capture input/PWM output (in PWM mode)
$\overline{\text{INT0}}$	I	Timer output disabling control input
$\overline{\text{INT1}}$	I	Waveform output manipulation event input

15.2.7 Timer RC I/O Control Register 0 (TRCIOR0)

Address 000F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control A0 bit	[IOA2 = 0 (output compare function)]	R/W
b1	IOA1	TRCGRA control A1 bit	b1 b0 0 0: Pin output by compare match A is disabled 0 1: Low-level output from TRCIOA pin at compare match A 1 0: High-level output from TRCIOA pin at compare match A 1 1: Toggle output from TRCIOA pin at compare match A [IOA2 = 1 (input capture function)] b1 b0 0 0: Rising edge on TRCIOA pin 0 1: Falling edge on TRCIOA pin 1 0: Two-way edge on TRCIOA pin 1 1: Do not set.	R/W
b2	IOA2	TRCGRA control A2 bit (1)	0: Output compare function 1: Input capture function	R/W
b3	—	Reserved	Set to 1.	R/W
b4	IOB0	TRCGRB control B0 bit	[IOB2 = 0 (output compare function)]	R/W
b5	IOB1	TRCGRB control B1 bit	b5 b4 0 0: Pin output by compare match B is disabled 0 1: Low-level output from TRCIOB pin at compare match B 1 0: High-level output from TRCIOB pin at compare match B 1 1: Toggle output from TRCIOB pin at compare match B [IOB2 = 1 (input capture function)] b5 b4 0 0: Rising edge on TRCIOB pin 0 1: Falling edge on TRCIOB pin 1 0: Two-way edge on TRCIOA pin 1 1: Do not set.	R/W
b6	IOB2	TRCGRB control B2 bit (1)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. The write value must be 1. The read value is 1.		—

Note:
1. When bits BUFEA and BUFEB in the TRCMR register are set to 1, registers TRCGRA and TRCGRC, and registers TRCGRB and TRCGRD are paired. The same values must be set in the IOA2 bit and the IOC2 bit in the TRCIOR1 register, and in the IOB2 bit and the IOD2 bit in the TRCIOR1 register, respectively.

The setting of the TRCIOR0 register is invalid in PWM and PWM2 modes.

17.2 Registers

Table 17.3 lists the A/D Converter Register Configuration.

Table 17.3 A/D Converter Register Configuration

Register Name		Symbol	After Reset	Address	Access Size
A/D Register 0	Lower 8 bits	AD0L	XXh	00098h	8 or 16 (1)
	Higher 2 bits	AD0H	000000XXb	00099h	
A/D Register 1	Lower 8 bits	AD1L	XXh	0009Ah	8 or 16 (1)
	Higher 2 bits	AD1H	000000XXb	0009Bh	
A/D Mode Register		ADMOD	00h	0009Ch	8
A/D Input Select Register		ADINSEL	00h	0009Dh	8
A/D Control Register 0		ADCON0	00h	0009Eh	8
A/D Interrupt Control Status Register		ADICSR	00h	0009Fh	8

X: Undefined

Note:

1. For details on access, see the description of the individual registers.

19.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved).
Figure 19.1 shows the Flash Memory Block Diagram.
The user ROM area contains program ROM and data flash.
• Program ROM: Flash memory mainly used for storing programs
• Data flash: Flash memory mainly used for storing data to be rewritten
The user ROM area is divided into several blocks.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area when the MCU is shipped. The boot ROM area is allocated separately from the user ROM area.

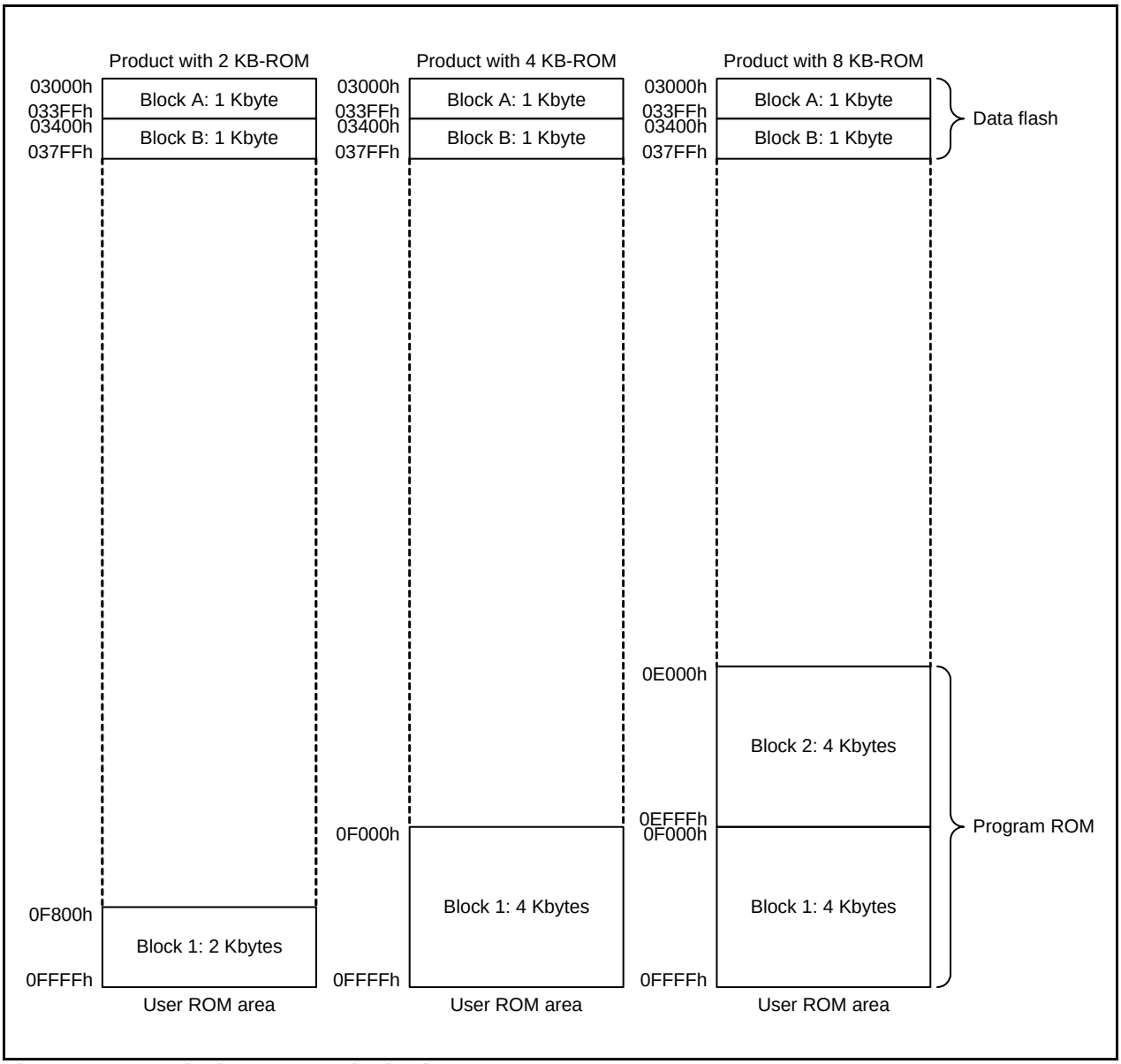


Figure 19.1 Flash Memory Block Diagram

FMR27 Bit (Low-current-consumption read mode enable bit)

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **10.5.11 Low-Current-Consumption Read Mode** for details.

When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-current-consumption read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-current-consumption read mode.

After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).

Table 20.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	—	ns
$t_{W(CKH)}$	CLK0 input high width	150	—	ns
$t_{W(CKL)}$	CLK0 input low width	150	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	80	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	70	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

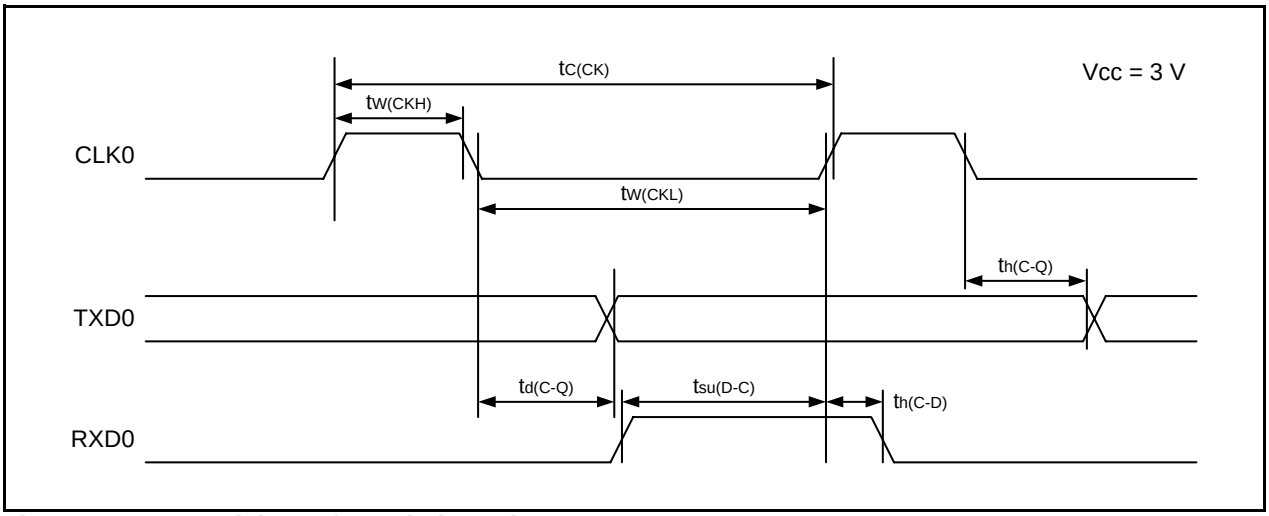


Figure 20.10 Serial Interface Timing When Vcc = 3 V

Table 20.24 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	380 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

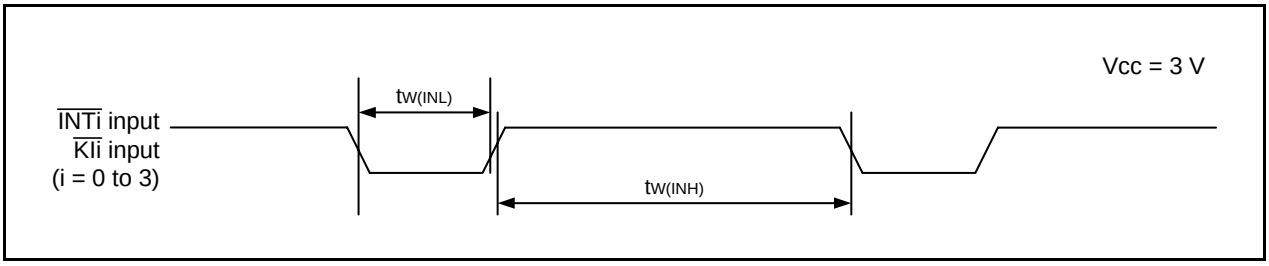


Figure 20.11 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 3 V

21.7 Notes on Timer RJ2

(1) Timer RJ2 stops counting after a reset. Start the count only after setting the value in the timer.

(2) After 1 (count is started) is written to the TSTART bit in the TRJCR register while the count is stopped, the TCSTF bit in the TRJCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started from the first active edge of the count source after the TCSTF bit is set to 1. After 0 (count is stopped) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 0.
Note:
1. Registers associated with timer RJ2: TRJ, TRJCR, TRJIOC, and TRJMR

(3) In event counter mode, set the TSTART bit in the TRJCR register to 1 (count is started) and then input an external pulse.

(4) In pulse width/pulse period measurement modes, bits TEDGF and TUNDF in the TRJCR register used are set to 0 by writing 0 by a program but remain unchanged even if 1 is written to these bits. If a read-modify-write instruction is used to set the TRJCR register, bits TEDGF and TUNDF may be erroneously set to 0 depending on the timing, even when the TEDGF bit is set to 1 (active edge received) and the TUNDF bit is set to 1 (underflow) during execution of the instruction.
In this case, write 1 using the MOV instruction to the TEDGF or TUNDF bit which is not supposed to be set to 0.

(5) Insert NOP instructions between writing to and reading from registers associated with the TRJ counter while the counter is stopped.

(6) When the TSTART bit in the TRJCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), allow at least three cycles of the count source clock for each write interval when writing to the TRJ register successively.

(7) Note the following when writing 0 to the TEDGF bit in the TRJCR register in pulse width measurement mode or pulse period measurement mode.
Set the TRJIF bit in the TRJIR register to 0 before setting the TEDGF bit to 0.
When reading the TEDGF bit immediately after setting it to 0, it is read as 0. However the internal signal of the TEDGF bit remains 1 for one to two cycles of the count source. If an active edge is input during this period, the internal signal of the TEDGF bit does not become 0 and the TEDGF bit is read as 1.
Since the TRJIF bit becomes 1 when the internal signal of the TEDGF bit changes from 0 to 1, the TRJIF bit does not become 1 and no interrupt is generated.
After setting the TEDGF bit to 0, confirm that 0 can be read after waiting for three or more count source cycles in order to accept the next interrupt request.