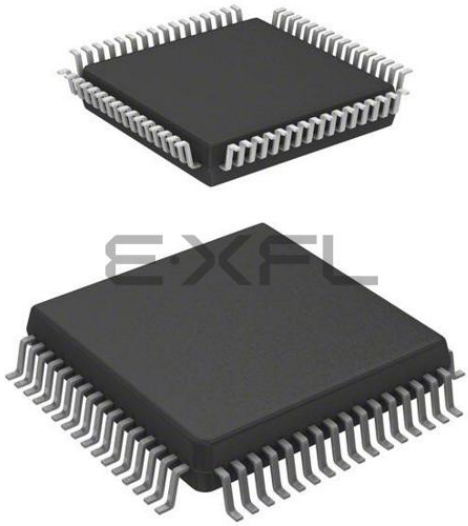

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Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36077ghv

Address	Register Name	Symbol	Page
00080h	UART0 Transmit/Receive Mode Register	U0MR	280
00081h	UART0 Bit Rate Register	U0BRG	281
00082h	UART0 Transmit Buffer Register	U0TBL	281
00083h		U0TBH	
00084h	UART0 Transmit/Receive Control Register 0	U0C0	282
00085h	UART0 Transmit/Receive Control Register 1	U0C1	283
00086h	UART0 Receive Buffer Register	U0RBL	284
00087h		U0RBH	
00088h	UART0 Interrupt Flag and Enable Register	U0IR	285
00089h			
0008Ah			
0008Bh			
0008Ch			
0008Dh			
0008Eh			
0008Fh			
00090h			
00091h			
00092h			
00093h			
00094h			
00095h			
00096h			
00097h			
00098h	A/D Register 0	AD0L	302
00099h		AD0H	
0009Ah	A/D Register 1	AD1L	302
0009Bh		AD1H	
0009Ch	A/D Mode Register	ADMOD	303
0009Dh	A/D Input Select Register	ADINSEL	304
0009Eh	A/D Control Register 0	ADCON0	305
0009Fh	A/D Interrupt Control Status Register	ADICSR	306
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h			
000A9h	Port P1 Direction Register	PD1	144
000AAh			
000ABh	Port P3 Direction Register	PD3	152
000ACh	Port P4 Direction Register	PD4	158
000ADh	Port PA Direction Register	PDA	164
000AEh			
000AFh	Port P1 Register	P1	144
000B0h			
000B1h	Port P3 Register	P3	152
000B2h	Port P4 Register	P4	158
000B3h	Port PA Register	PA	164
000B4h			
000B5h	Pull-Up Control Register 1	PUR1	145
000B6h			
000B7h	Pull-Up Control Register 3	PUR3	153
000B8h	Pull-Up Control Register 4	PUR4	159
000B9h	Port I/O Function Control Register	PINSR	142
000BAh			
000BBh	Drive Capacity Control Register 1	DRR1	145
000BCh			
000BDh	Drive Capacity Control Register 3	DRR3	153
000BEh			
000BFh			

Note:
1. The blank areas are reserved. No access is allowed.

Address	Register Name	Symbol	Page
000C0h			
000C1h	Open-Drain Control Register 1	POD1	146
000C2h			
000C3h	Open-Drain Control Register 3	POD3	154
000C4h	Open-Drain Control Register 4	POD4	159
000C5h	Port PA Mode Control Register	PAMCR	165
000C6h			
000C7h			
000C8h	Port 1 Function Mapping Register 0	PML1	146
000C9h	Port 1 Function Mapping Register 1	PMH1	147
000CAh			
000CBh			
000CCh	Port 3 Function Mapping Register 0	PML3	154
000CDh	Port 3 Function Mapping Register 1	PMH3	155
000CEh	Port 4 Function Mapping Register 0	PML4	160
000CFh	Port 4 Function Mapping Register 1	PMH4	160
000D0h			
000D1h	Port 1 Function Mapping Expansion Register	PMH1E	148
000D2h			
000D3h			
000D4h			
000D5h	Port 4 Function Mapping Expansion Register	PMH4E	161
000D6h			
000D7h			
000D8h	Timer RJ Counter Register	TRJ	180
000D9h			
000DAh	Timer RJ Control Register	TRJCR	181
000DBh	Timer RJ I/O Control Register	TRJIOC	182
000DCh	Timer RJ Mode Register	TRJMR	184
000DDh	Timer RJ Event Select Register	TRJISR	184
000DEh	Timer RJ Interrupt Control Register	TRJIR	185
000DFh			
000E0h	Timer RB Control Register	TRBCR	199
000E1h	Timer RB One-Shot Control Register	TRBOCR	200
000E2h	Timer RB I/O Control Register	TRBIOC	201
000E3h	Timer RB Mode Register	TRBMR	202
000E4h	Timer RB Prescaler Register Timer RB Primary/Secondary Register (Lower 8 Bits)	TRBPRE	203
000E5h	Timer RB Primary Register Timer RB Primary Register (Higher 8 Bits)	TRBPR	204
000E6h	Timer RB Secondary Register Timer RB Secondary Register (Higher 8 Bits)	TRBSC	205
000E7h	Timer RB Interrupt Control Register	TRBIR	206
000E8h	Timer RC Counter	TRCCNT	232
000E9h			
000EAh	Timer RC General Register A	TRCGRA	233
000EBh			
000ECh	Timer RC General Register B	TRCGRB	233
000EDh			
000EEh	Timer RC General Register C	TRCGRC	233
000EFh			
000F0h	Timer RC General Register D	TRCGRD	233
000F1h			
000F2h	Timer RC Mode Register	TRCMR	235
000F3h	Timer RC Control Register 1	TRCCR1	236
000F4h	Timer RC Interrupt Enable Register	TRCIER	237
000F5h	Timer RC Status Register	TRCSR	238
000F6h	Timer RC I/O Control Register 0	TRCIOR0	239
000F7h	Timer RC I/O Control Register 1	TRCIOR1	240
000F8h	Timer RC Control Register 2	TRCCR2	241
000F9h	Timer RC Digital Filter Function Select Register	TRCDF	242
000FAh	Timer RC Output Enable Register	TRCOER	243
000FBh	Timer RC A/D Conversion Trigger Control Register	TRCADCR	244
000FCh	Timer RC Waveform Output Manipulation Register	TRCOPR	245
000FDh			
000FEh			
000FFh			

WDR Bit (Watchdog timer reset detect flag)

This flag indicates that a reset has been generated by the watchdog timer.

[Condition for setting to 0]
• When a software reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a watchdog timer reset occurs.

8. Watchdog Timer

The watchdog timer is a function for detecting program malfunctions. Using this function is recommended, since it can improve system reliability.
The watchdog timer also has a function that can be used as a periodic timer.

8.1 Overview

The watchdog timer has a 14-bit down counter, and count source protection mode can be enabled or disabled.
Table 8.1 lists the Watchdog Timer Specifications.
For details on the watchdog timer reset, see **6.3.5 Watchdog Timer Reset**.
For details on the periodic timer, see **8.3.4 Periodic Timer Function**.
Figure 8.1 shows the Watchdog Timer Block Diagram.

Table 8.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock or low-speed on-chip oscillator clock (1/16)	Low-speed on-chip oscillator clock
Count operation	Decrement	
Count start condition	Either of the following can be selected: • The count is automatically started after a reset. • The count is started by writing to the WDTS register.	
Count stop conditions	When wait mode or stop mode is entered while the count source is the CPU clock	None
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register during the refresh acceptance period (when a refresh acceptance period is set) • Underflow	
Operation at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Selection of the count source Selected by bits WDTC6 to WDTC7 in the WDTC register. • Count source protection mode - Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register. - If count source protection mode is disabled, whether count source protection mode is enabled or disabled is selected by the CSPRO bit in the CSPR register. • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register. • Initial value of the watchdog timer (underflow period) Selected by bits WDTUFS0 to WDTUFS1 in the OFS2 register. • Refresh acceptance period for the watchdog timer Selected by bits WDTRCS0 to WDTRCS1 in the OFS2 register.	

11.2.8 Interrupt Monitor Flag Register 2 (IRR2)

Address 00052h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IRCMP3	IRCMP1	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0.	R
b1	—			
b2	IRCMP1	Comparator B1 interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b3	IRCMP3	Comparator B3 interrupt request monitor flag		R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

The IRR2 register is the monitor flag register for comparator B1 and comparator B3 interrupt requests. See **11.4.2.1 Registers IRR0 to IRR2** for the relation between interrupt monitor flag bits and peripheral function interrupts.

12.3.1 Port P1 Direction Register (PD1)

Address 000A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD1_7	PD1_6	PD1_5	PD1_4	PD1_3	PD1_2	PD1_1	PD1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD1_0	Port P1_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PD1_1	Port P1_1 direction bit		R/W
b2	PD1_2	Port P1_2 direction bit		R/W
b3	PD1_3	Port P1_3 direction bit		R/W
b4	PD1_4	Port P1_4 direction bit		R/W
b5	PD1_5	Port P1_5 direction bit		R/W
b6	PD1_6	Port P1_6 direction bit		R/W
b7	PD1_7	Port P1_7 direction bit		R/W

The PD1 register is used to select whether I/O ports are used as input or output.
Each bit in the PD1 register corresponds to individual ports.

12.3.2 Port P1 Register (P1)

Address 000AFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P1_0	Port P1_0 bit	0: Low level 1: High level	R/W
b1	P1_1	Port P1_1 bit		R/W
b2	P1_2	Port P1_2 bit		R/W
b3	P1_3	Port P1_3 bit		R/W
b4	P1_4	Port P1_4 bit		R/W
b5	P1_5	Port P1_5 bit		R/W
b6	P1_6	Port P1_6 bit		R/W
b7	P1_7	Port P1_7 bit		R/W

The P1 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P1 register. The P1 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pins. Each bit in the P1 register corresponds to individual ports.

12.3.8 Port 1 Function Mapping Expansion Register (PMH1E)

Address 000D1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	P15SEL2	—	P14SEL2
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P14SEL2	The P1_4 pin function is selected in conjunction with bits P14SEL0 to P14SEL1 in the PMH1 register. For details, see **12.3.7 Port 1 Function Mapping Register 1 (PMH1)**.		R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	P15SEL2	The P1_5 pin function is selected in conjunction with bits P15SEL0 to P15SEL1 in the PMH1 register. For details, see **12.3.7 Port 1 Function Mapping Register 1 (PMH1)**.		R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

The PMH1E register is used to select the port 1 function in conjunction with registers PML1 and PMH1.

12.8 Pin Settings for Peripheral Function I/O

Tables 12.21 to 12.24 list the pin settings for peripheral function I/O.

Table 12.21 TRCIOA Pin Settings

Register	TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	TCEG1	TCEG0	
Setting value	0	1	0	0	1	X	X	Timer mode waveform output (output compare function)
				1	X			
	0	1	1	X	X	X	X	Timer mode (input capture function)
	1							
	1	0	X	X	X	0	1	PWM2 mode (TRCTRG input)
						1	X	

X: 0 or 1

Table 12.22 TRCIOB Pin Settings

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 12.23 TRCIOC Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 12.24 TRCIOD Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

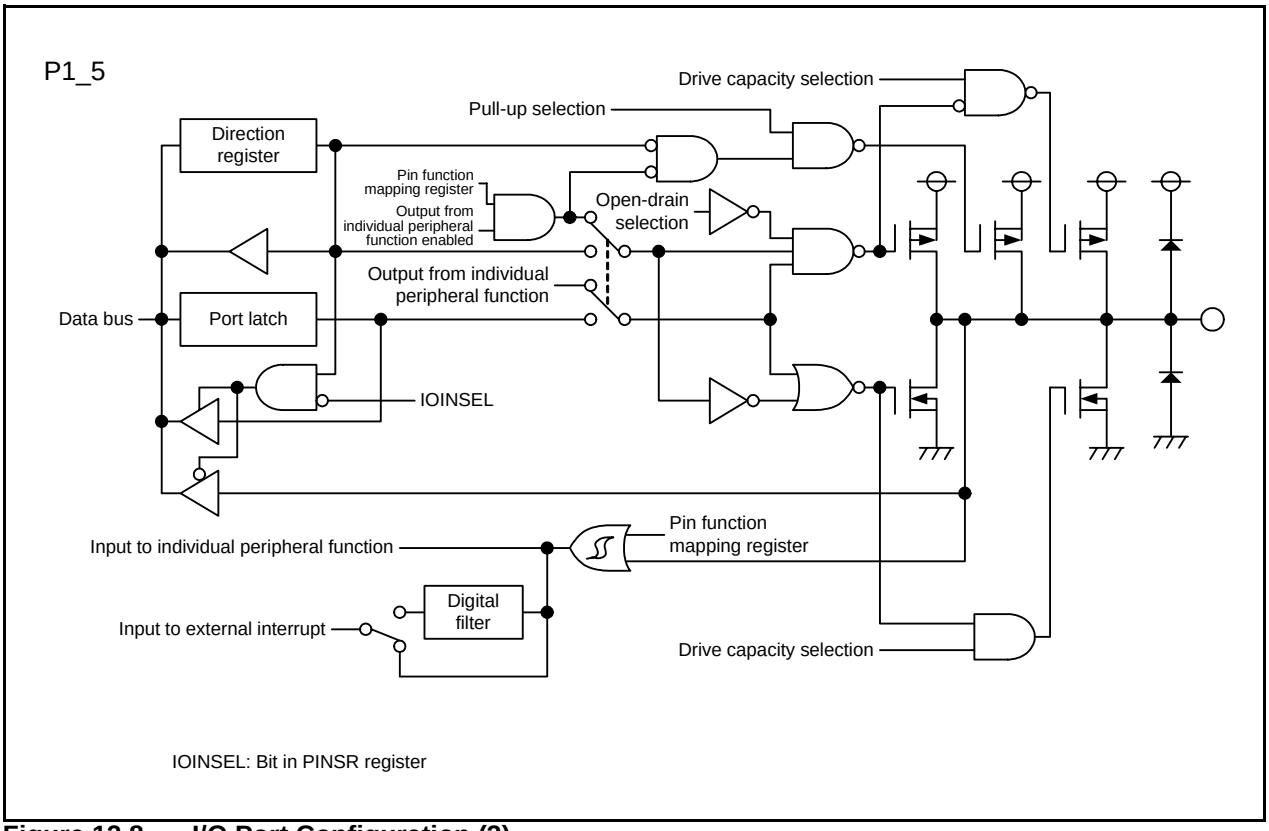


Figure 12.8 I/O Port Configuration (3)

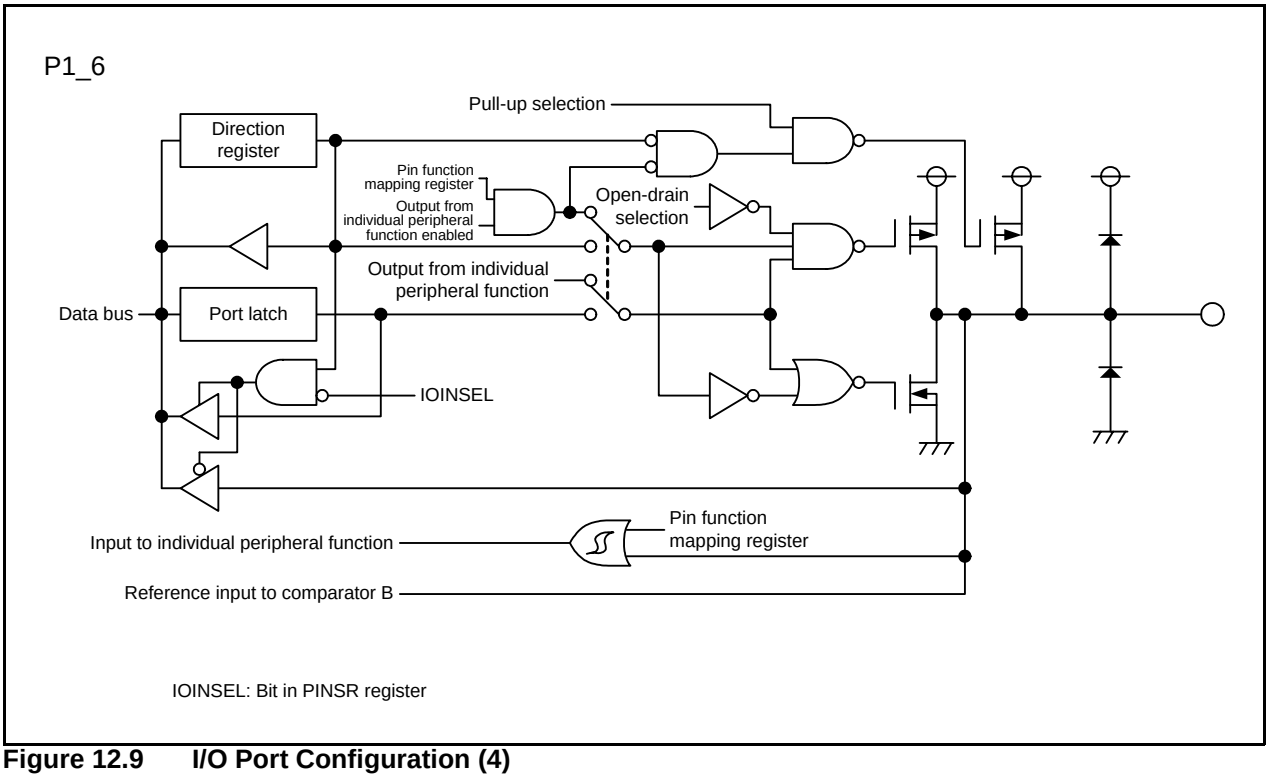


Figure 12.9 I/O Port Configuration (4)

14. Timer RB2

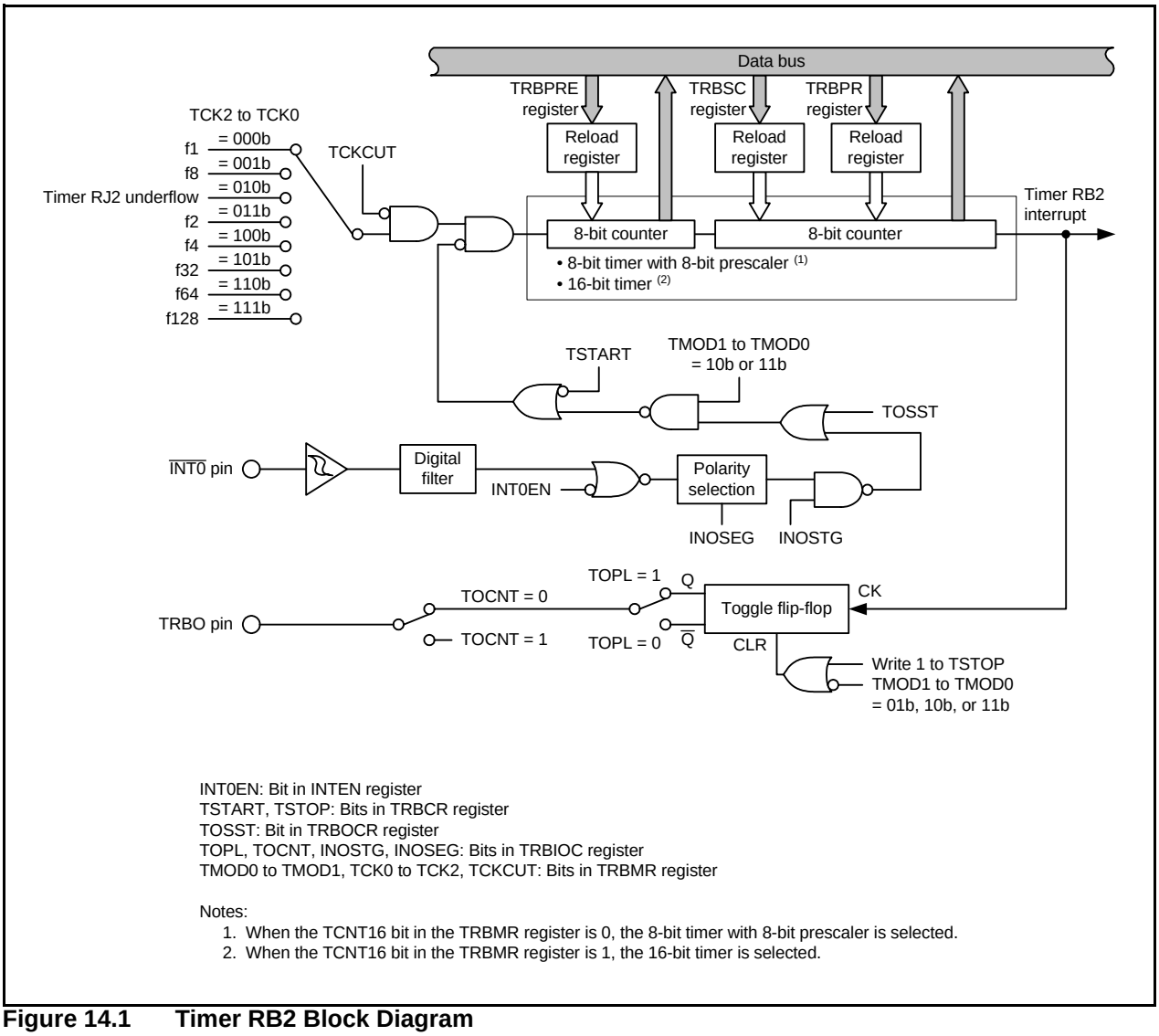
Timer RB2 can be used as an 8-bit timer with an 8-bit prescaler or as a 16-bit timer. The prescaler and timer each consist of a reload register and counter which are allocated to the same address. Timer RB2 has timer RB primary and timer RB secondary reload registers.

14.1 Overview

Table 14.1 lists the Timer RB2 Specifications. Figure 14.1 shows the Timer RB2 Block Diagram.

Table 14.1 Timer RB2 Specifications

Item		Description
Operating modes	Timer mode	An internal count source or timer RJ2 underflow is counted.
	Programmable waveform generation mode	An arbitrary pulse width is output successively.
	Programmable one-shot generation mode	A one-shot pulse is output.
	Programmable wait one-shot generation mode	A delayed one-shot pulse is output.
Count source		Selectable from f1, f2, f4, f8, f32, f64, f128, and timer RJ2 underflow.
Interrupt		Timer RB2 underflow

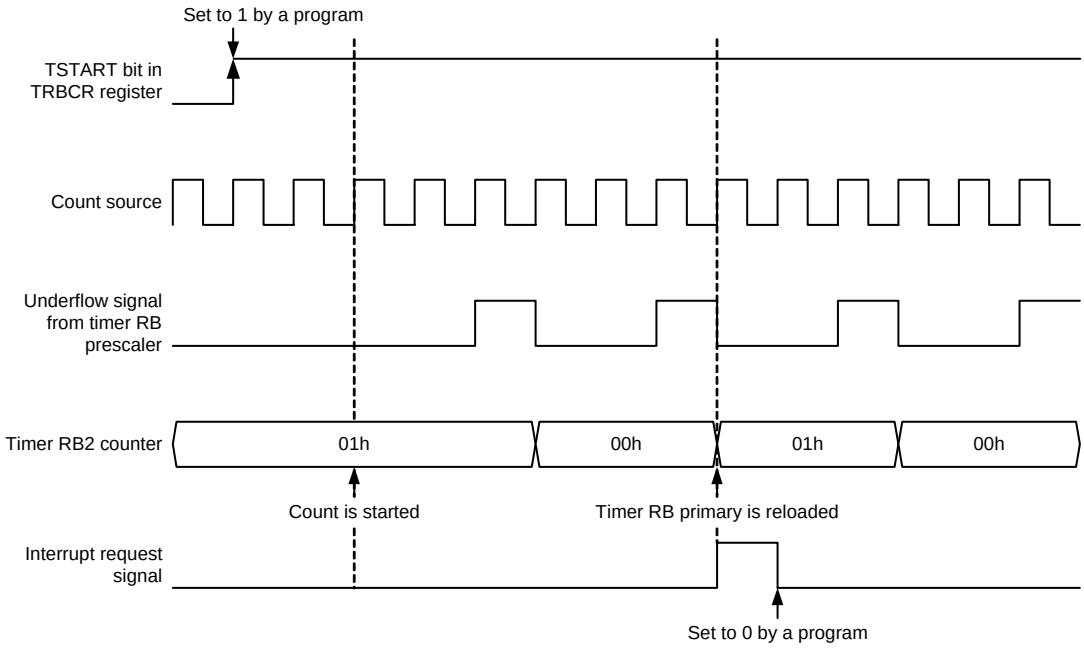


INT0EN: Bit in INTEN register
TSTART, TSTOP: Bits in TRBCR register
TOSST: Bit in TRBOCR register
TOPL, TOCNT, INOSTG, INOSEG: Bits in TRBIOC register
TMOD0 to TMOD1, TCK0 to TCK2, TCKCUT: Bits in TRBMR register

Notes:
1. When the TCNT16 bit in the TRBMR register is 0, the 8-bit timer with 8-bit prescaler is selected.
2. When the TCNT16 bit in the TRBMR register is 1, the 16-bit timer is selected.

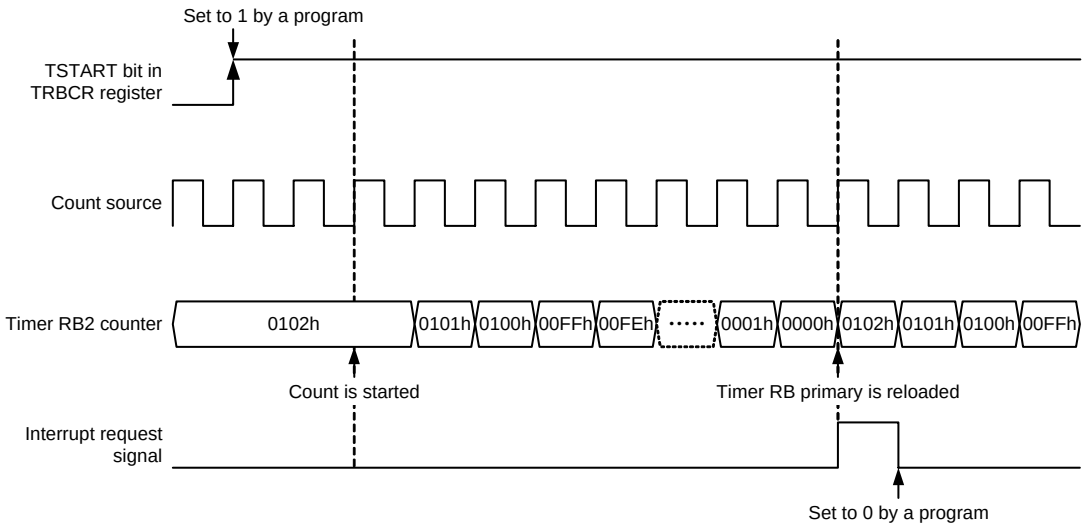
Figure 14.1 Timer RB2 Block Diagram

• 8-bit timer with 8-bit prescaler in timer mode



The above diagram applies under the following conditions:
- TRBPRE register = 02h, TRBPR register = 01h
- TOCNT bit in TRBIOC register = 0 (waveform output)
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

• 16-bit timer in timer mode



The above diagram applies under the following conditions:
- TRBPRE register = 02h, TRBPR register = 01h
- TOCNT bit in TRBIOC register = 0 (waveform output)
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

Figure 14.2 Operation Example in Timer Mode

15.4.3 Changing Output Pins and General Registers

The settings for bits IOC3 and IOD3 in the TRCIOR1 register can redirect the compare match output with registers TRCGRC and TRCGRD from pins TRCIOC and TRCIOD to pins TRCIOA and TRCIOB, respectively. The TRCIOA pin can output a combination of compare matches A and C and the TRCIOB pin can output a combination of compare matches B and D.
Figure 15.21 shows the Block Diagram for Changing Output Pins and General Registers.

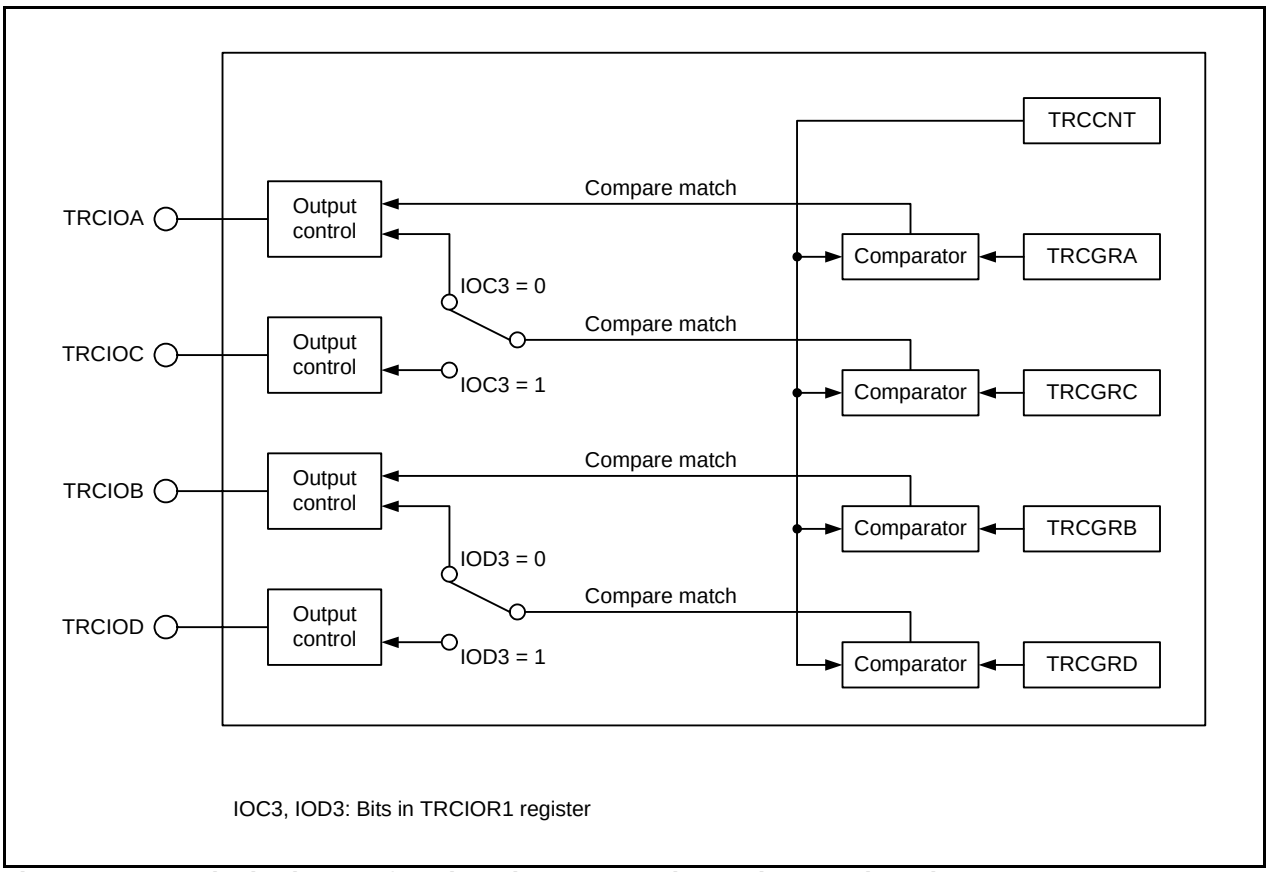


Figure 15.21 Block Diagram for Changing Output Pins and General Registers

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and the IOD3 bit to 0 (TRCIOB output register).
- Set bits BUFEA and BUFEB in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRA and TRCGRC. Also, set different values in registers TRCGRB and TRCGRD.

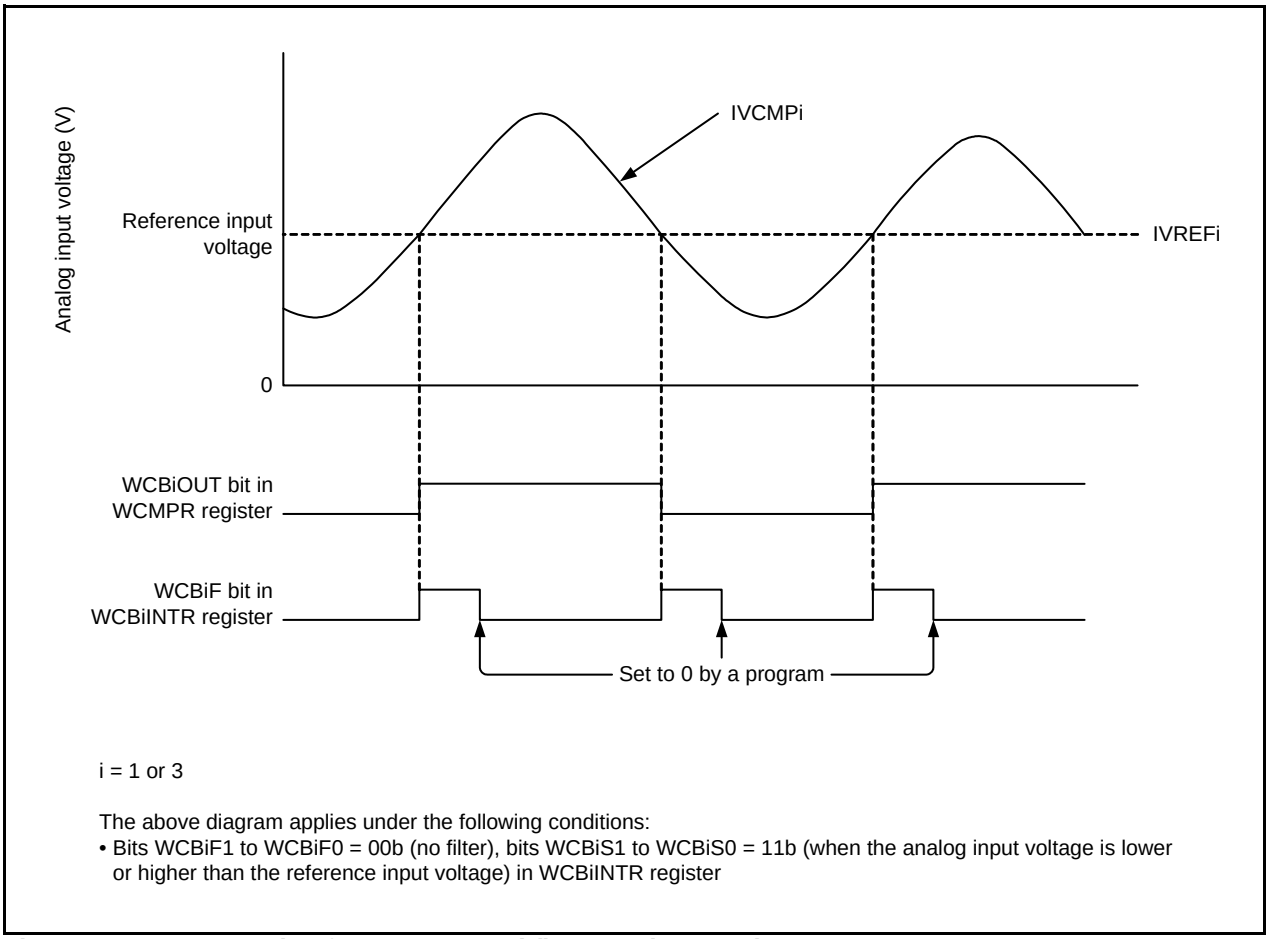


Figure 18.3 Example of Comparator Bi (i = 1 or 3) Operation

FMR27 Bit (Low-current-consumption read mode enable bit)

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **10.5.11 Low-Current-Consumption Read Mode** for details.

When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-current-consumption read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-current-consumption read mode.

After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).

19.6.4 Setting and Cancelling Each Mode

Figure 19.5 shows Setting and Cancelling EW0 Mode. Figure 19.6 shows Setting and Cancelling EW1 Mode.

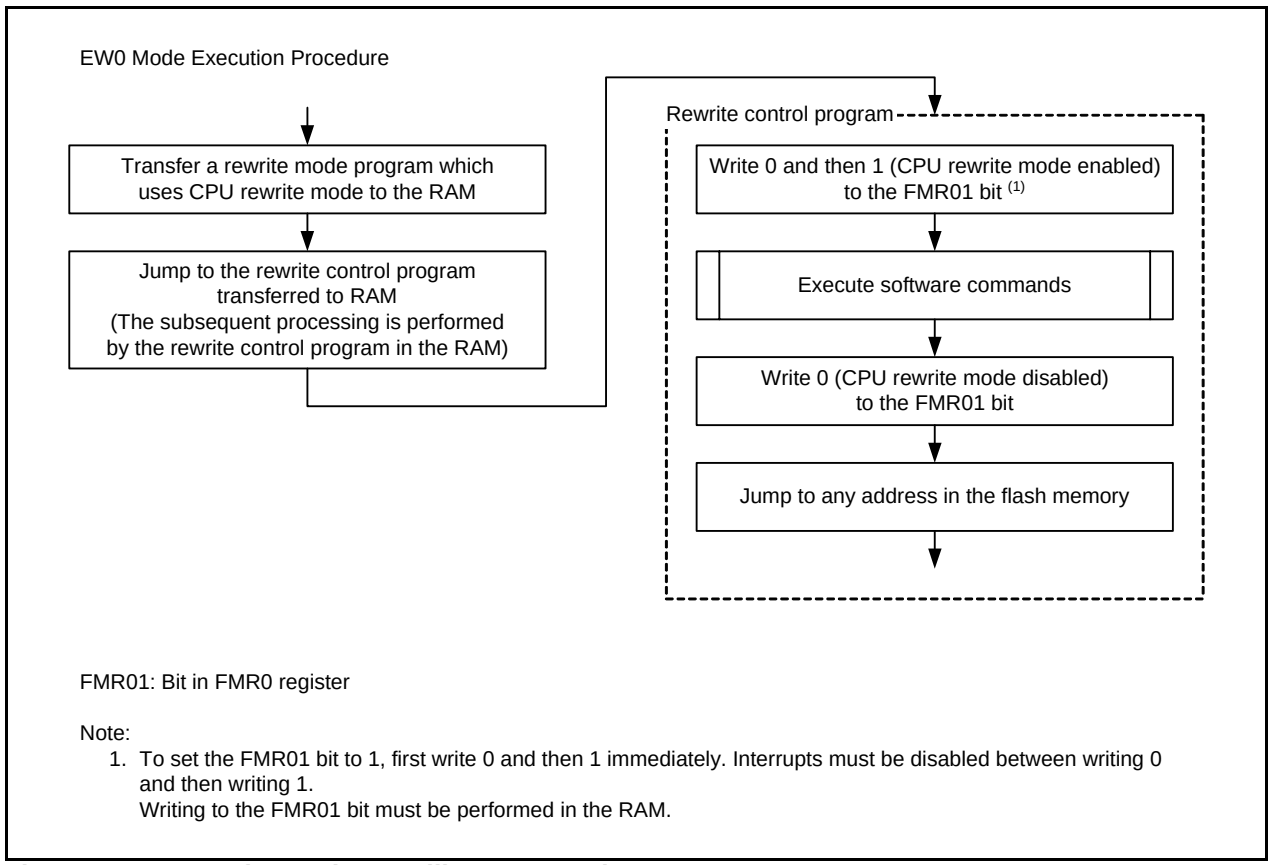


Figure 19.5 Setting and Cancelling EW0 Mode

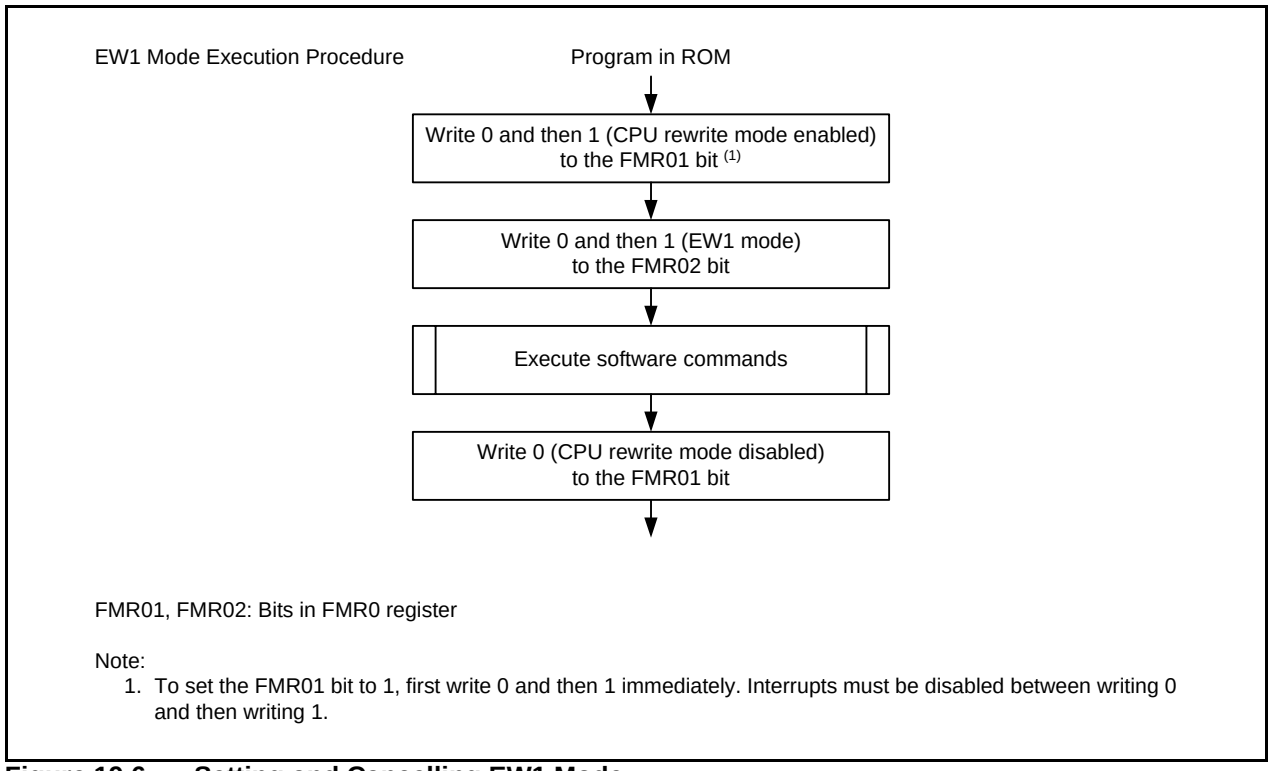
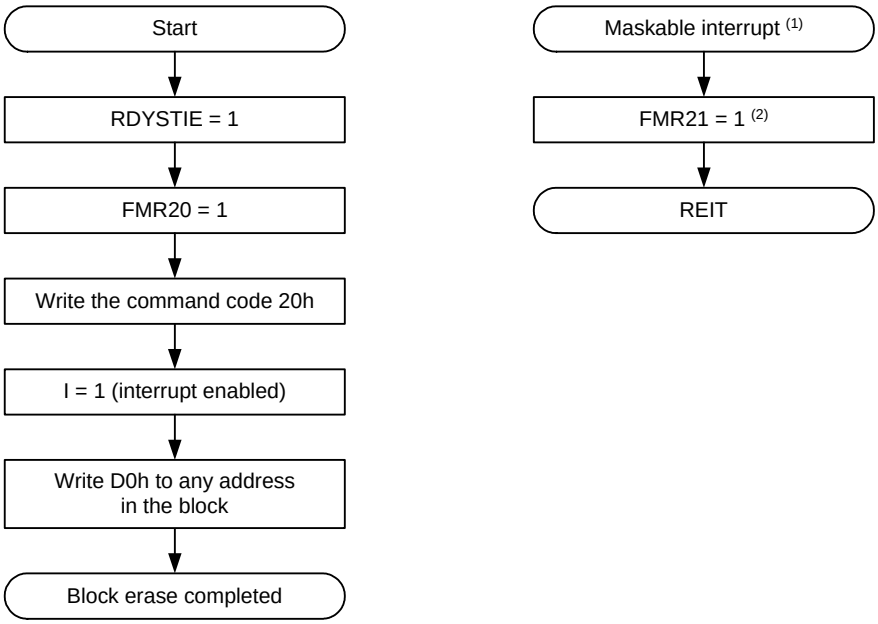
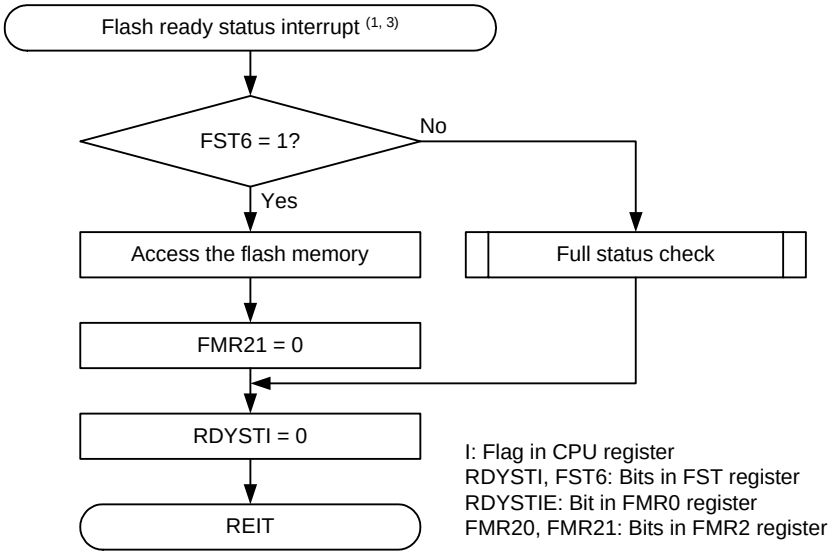


Figure 19.6 Setting and Cancelling EW1 Mode





Notes:
1. The interrupt vector table and interrupt routine to be used must be allocated to an area other than the erase-target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.
3. A flash ready status interrupt is generated when auto-erase is suspended.

Figure 19.14 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

21.5 Notes on Interrupts

21.5.1 Reading Address 00000h

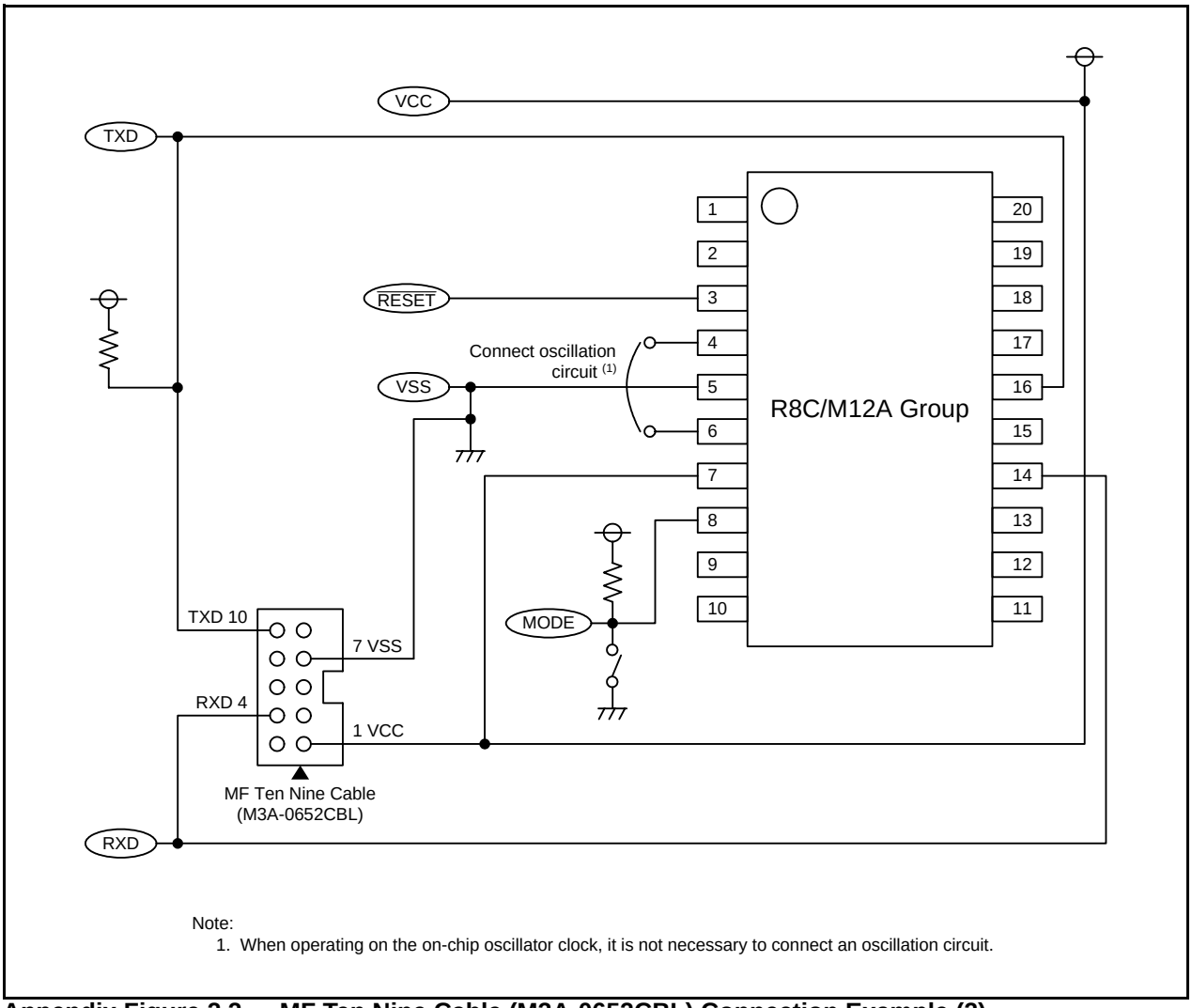
Do not read address 00000h by a program. When an external interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from address 00000h in the interrupt sequence. At this time, the corresponding bit in the IRR3 register for the acknowledged interrupt is set to 0.
If a program is used to read address 00000h, the corresponding bit in the IRR3 register for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

21.5.2 SP Setting

Set a value in the SP before any interrupt is acknowledged. The SP is 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

21.5.3 External Interrupt and Key Input Interrupt

Signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ must meet either the low-level width or the high-level width requirements shown in External Interrupt $\overline{\text{INTi}}$ Input (i = 0 to 3) in the Electrical Characteristics, regardless of the CPU operating clock. For details, see **Table 20.18** (Vcc = 5 V), **Table 20.24** (Vcc = 3 V), and **Table 20.30** (Vcc = 2.2 V) **External Interrupt $\overline{\text{INTi}}$ Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)**.



Note:
1. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Appendix Figure 2.2 MF Ten Nine Cable (M3A-0652CBL) Connection Example (2)

Appendix Table 4.3 Register Comparison between R8C/M12A Group and R8C/M13B Group (2)

Related Function	Register	Address	Bit	Remarks
Timer RK	TMKM	00188h		Registers added
	TMKCR	00189h		
	TMKLD	0018Ah		
	TMKCMP	0018Bh		
	TMKIR	0018Ch		
Timer RE2	TRESEC (TRECNT)	00130h		Registers added
	TREMIN	00131h		
	TREHR	00132h		
	TREWK	00133h		
	TREDY	00134h		
	TREMON	00135h		
	TREYR	00136h		
	TRECR	00137h		
	TRECSR	00138h		
	TREADJ	00139h		
	TREIFR	0013Ah		
	TREIER	0013Bh		
	TREAMN	0013Ch		
	TREAHR	0013Dh		
	TREAWK	0013Eh		
	TREPRC	0013Fh		
UART1	U1MR	00190h		Registers added
	U1BRG	00191h		
	U1TBL	00192h		
	U1TBH	00193h		
	U1C0	00194h		
	U1C1	00195h		
	U1RBL	00196h		
	U1RBH	00197h		
	U1IR	00198h		
IrDA	IRCR	0019Ch		Register added
IIC/SSU	IICCR	00160h		Registers added
	SSBR	00161h		
	SITDR	00162h		
	SIRDR	00164h		
	SICR1	00166h		
	SICR2	00167h		
	SIMR1	00168h		
	SIER	00169h		
	SISR	0016Ah		
	SIMR2	0016Bh		

REVISION HISTORY	R8C/M11A Group, R8C/M12A Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
0.01	Jan 29, 2010	—	First Edition issued
0.10	Jun 14, 2010	All pages	Revised
0.11	Jun 29, 2010	180	13.4.1 "... next count source" → "... next system clock (f)"
		231	15.2.11 revised
		232	15.2.12 revised
		233	15.2.13 Note 1 revised
0.12	Jul 06, 2010	400, 401	Appendix Figures 2.3 and 2.4 Connection line between E8a emulator and VCC revised
1.00	Nov 30, 2010	All pages	"Preliminary" and "Under development" deleted
		B-1	00021h, 00025h, 00030h and 00035h revised
		B-2	000DEh and 000E7h revised
		1	1.1 revised
		3	Table 1.2 IRR3 and IRR2 revised
		4	Table 1.3 Watchdog timer revised
		5	Table 1.4 Note 1 revised
		6	Table 1.5 revised
		10	Table 1.7 revised
		11	Figure 2.1 revised
		15	Table 3.1 00021h, 00025h, 00030h to 00033h, and 00035h revised
		18	Table 3.4 000DEh and 000E7h revised
		23	Table 3.9 Notes 1 and 2 revised
		24	4 revised
		25	Table 5.1 Notes 3 and 4 revised
		26, 37	5.2.1, 6.2.1 SRST Bit revised
		27	5.2.2 After Reset, Note 3 revised, "When changing ... peripheral function beforehand." added
		29, 38	5.2.5, 6.2.2 revised
		31, 40	5.2.6, 6.2.3 Note 1 revised
		32, 41	5.2.7, 6.2.4 Note 1 revised
		33	"Table 5.3 ... 5.2.4 Hardware Reset Protect Register (HRPR)" and Table 5.3 added
		37	Table 6.2 Notes 2 and 3 revised
		42	Figure 6.2 Note 1 revised
		43	6.3.2 revised, the last Figure 6.3 deleted
		53	7.2.2 Note 1 revised
		61	7.6 and Figure 7.6 added
		62	Table 8.1 revised, Note 1 deleted
		63	Figure 8.1 revised
		64	Table 8.2 and 8.2.1 revised
		65	8.2.2 to 8.2.4 After Reset revised
		66	8.2.6 revised
		67	8.3.1.1 and Figure 8.2 revised

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Rev.	Date	Description	
		Page	Summary
1.00	Nov 30, 2010	169	Figure 12.11 revised
		172	Figures 12.15 and 12.16 revised
		173	Figure 12.17 revised
		175, 385	12.11.2, 21.6.2 added
		176	13 and Table 13.1 revised
		177	Figure 13.1 and Table 13.2 revised
		178	Table 13.3 and 13.3.1 revised
		181	TOPCR Bit and Table 13.6 revised
		183	13.3.6 revised
		186	13.4.3 revised
		187	13.4.4 revised
		191, 386	13.5, 21.7 revised
		193, 388	Figures 13.10, 13.11, 21.6, and 21.7 revised
		195	14.2 revised
		196	Table 14.3 revised
		197	14.3.1 Notes 2 and 3 deleted
		217	Tables 14.6 and 14.7 revised
		228	Table 15.2 revised
		230	15.2.1 revised
		231	15.2.2 revised
		232	15.2.3 revised
		233	15.2.4 revised
		238	15.2.9 revised
		244	15.3.1 revised
		252	Figure 15.12 revised
		259	Figure 15.19 revised
		262	"toggle output from TRCIOD pin ..." → "toggle output from TRCIOB pin ..."
		263	Figure 15.23 revised
		264	Figures 15.24 and 15.25 revised
		265	Figure 15.26 revised
		266	Figure 15.27 revised
		271, 391	15.6.2, 15.6.4, 15.6.7, 21.9.2, 21.9.4, and 21.9.7 revised
		275	Figure 16.2 revised
		280	16.2.6 revised
		289	Figure 16.6 revised
		291	Table 16.8 Note 1 revised
		295	Table 17.1 revised
		296	Figure 17.1 and Table 17.2 revised
		298	17.2.1 revised
		299	17.2.2 revised
		300	17.2.3 revised
		301	17.2.4 revised