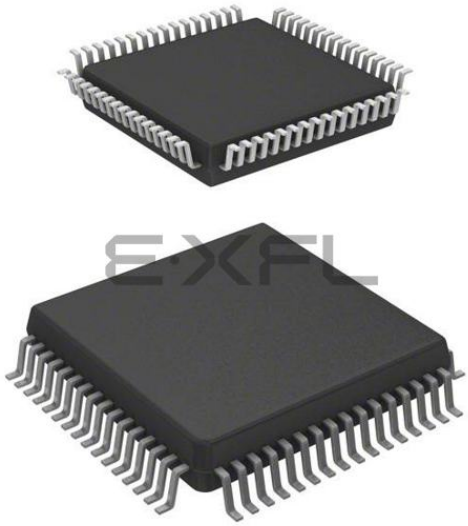

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36077ghwv

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. For details, see the text of the manual.

The following documents apply to the R8C/M11A Group and R8C/M12A Group. Make sure to see the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/M11A Group, R8C/M12A Group Datasheet	R01DS0010EJ
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: For details on using peripheral functions, see the application notes.	R8C/M11A Group, R8C/M12A Group User's Manual: Hardware	This User's manual
User's manual: Software	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled. If IPL is set to levels from 2 to 7, all maskable interrupt requests are disabled.

2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

Table 3.3 SFR Information (3) (1)

Address	Register Name	Symbol	After Reset
0007Ah			
0007Bh			
0007Ch			
0007Dh			
0007Eh			
0007Fh			
00080h	UART0 Transmit/Receive Mode Register	U0MR	00h
00081h	UART0 Bit Rate Register	U0BRG	XXh
00082h	UART0 Transmit Buffer Register	U0TBL	XXh
00083h		U0TBH	XXh
00084h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00085h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00086h	UART0 Receive Buffer Register	U0RBL	XXh
00087h		U0RBH	XXh
00088h	UART0 Interrupt Flag and Enable Register	U0IR	00h
00089h			
0008Ah			
0008Bh			
0008Ch			
0008Dh			
0008Eh			
0008Fh			
00090h			
00091h			
00092h			
00093h			
00094h			
00095h			
00096h			
00097h			
00098h	A/D Register 0	AD0L	XXh
00099h		AD0H	000000XXb
0009Ah	A/D Register 1	AD1L	XXh
0009Bh		AD1H	000000XXb
0009Ch	A/D Mode Register	ADMOD	00h
0009Dh	A/D Input Select Register	ADINSEL	00h
0009Eh	A/D Control Register 0	ADCON0	00h
0009Fh	A/D Interrupt Control Status Register	ADICSR	00h
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h			
000A9h	Port P1 Direction Register	PD1	00h
000AAh			
000ABh	Port P3 Direction Register	PD3	00h
000ACh	Port P4 Direction Register	PD4	00h
000ADh	Port PA Direction Register	PDA	00h
000AEh			
000AFh	Port P1 Register	P1	00h
000B0h			
000B1h	Port P3 Register	P3	00h
000B2h	Port P4 Register	P4	00h
000B3h	Port PA Register	PA	00h
000B4h			
000B5h	Pull-Up Control Register 1	PUR1	00h
000B6h			
000B7h	Pull-Up Control Register 3	PUR3	00h
000B8h	Pull-Up Control Register 4	PUR4	00h
000B9h	Port I/O Function Control Register	PINSR	00h
000BAh			
000BBh	Drive Capacity Control Register 1	DRR1	00h
000BCh			
000BDh	Drive Capacity Control Register 3	DRR3	00h
000BEh			
000BFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

11.4.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are restored. The program that was running before the interrupt request was acknowledged starts running again.

The registers saved by a program in the interrupt routine should be restored using the POPM or similar instruction before executing the REIT instruction.

11.4.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Any maskable interrupt (peripheral function) priority level can be selected by bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5. However, if two or more maskable interrupts have the same priority level, the interrupt with higher priority given by hardware is acknowledged.

The priority of special interrupts such as the watchdog timer interrupt is set by hardware.

Figure 11.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If a software interrupt instruction is executed, the MCU will execute the corresponding interrupt routine.

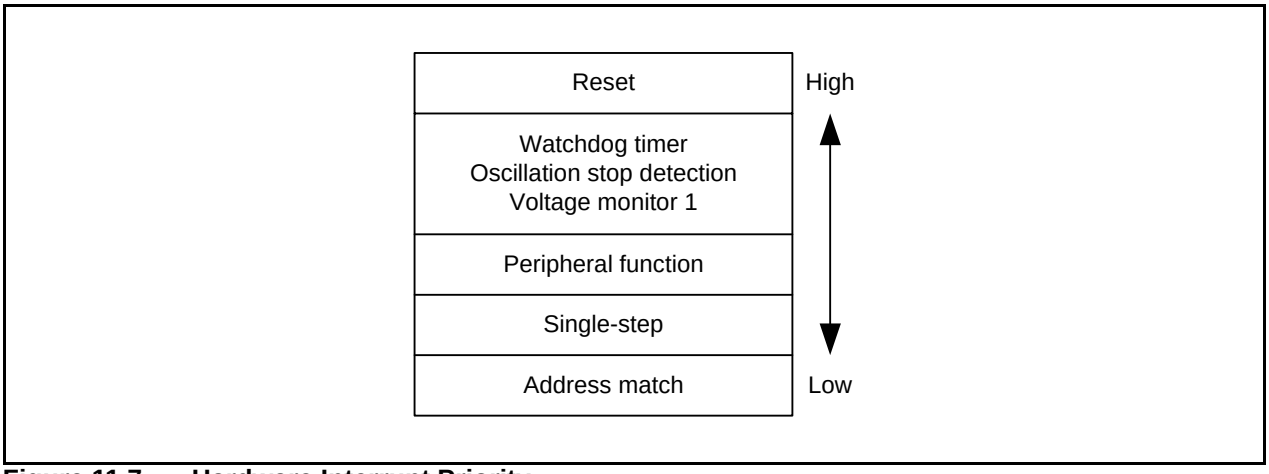
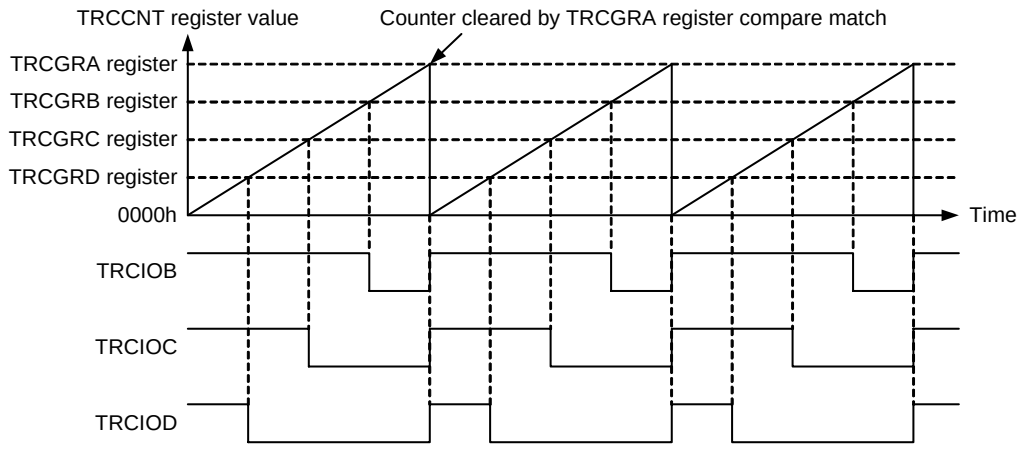


Figure 11.7 Hardware Interrupt Priority

Figure 15.9 shows an Operation Example in PWM Mode.

• High-level output when TRCCNT register is cleared at compare match A. Low-level output at compare matches B, C, and D. (POLB bit = 0, POLC bit = 0, and POLD bit = 0 in TRCCR2 register)



• Low-level output when TRCCNT register is cleared at compare match A. High-level output at compare matches B, C, and D. (POLB bit = 1, POLC bit = 1, and POLD bit = 1 in TRCCR2 register)

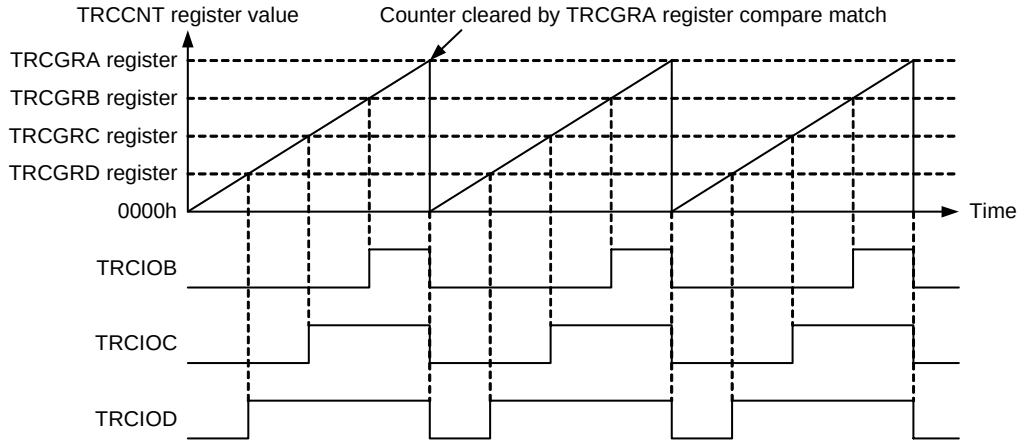


Figure 15.9 Operation Example in PWM Mode

15.3.3 PWM2 Mode

Unlike PWM mode in PWM2 mode, a waveform is output from the TRCIOB pin at a compare match with registers TRCGRB and TRCGRC. When the BUFEB bit in the TRCMR register is set to 1 (TRCGRD register is used as a buffer register for TRCGRB register), the TRCGRD register functions as a buffer register for the TRCGRB register. The output level is determined by the TOB bit in the TRCCR1 register.

When the TOB bit is 0 (output value 0), a low level is output at a compare match with the TRCGRB register and a high level is output at a compare match with the TRCGRC register. When the TOB bit is 1 (output value 1), a high level is output at a compare match with the TRCGRB register and a low level is output at a compare match with the TRCGRC register.

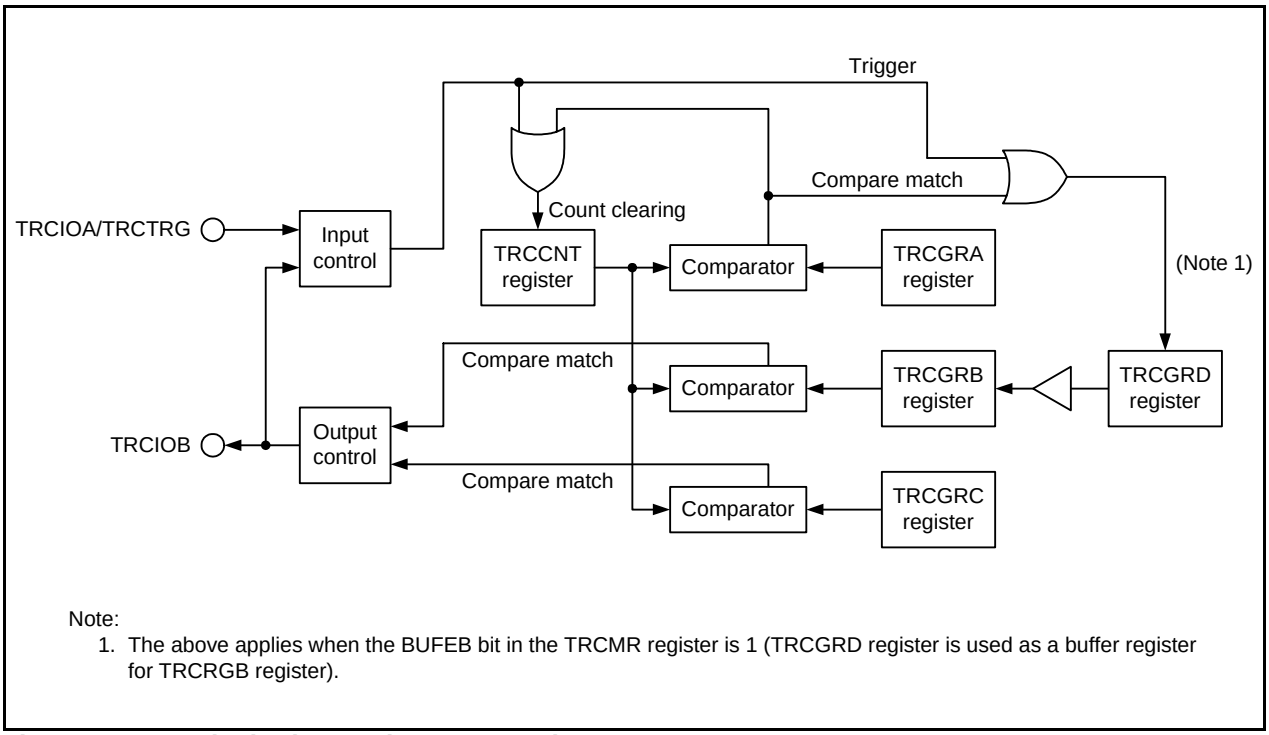
Table 15.16 lists the Combinations of Pin Functions and General Registers for PWM2 Mode and General Registers for PWM2 Mode. Figure 15.12 shows the Block Diagram in PWM2 Mode. Figure 15.13 shows the Timing of Buffer Operations for Registers TRCGRD and TRCGRB in PWM2 Mode.

The value in the TRCGRD register is transferred to the TRCGRB register and the counter is cleared by a compare match with the TRCGRA register. However, the counter is cleared only when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A). Also, when trigger input is enabled by bits TCEG0 to TCEG1 in the TRCCR2 register in PWM2 mode, the value in the TRCGRD register is transferred to the TRCGRB register and the counter is cleared by a trigger. The timer I/O pins that are not used in PWM2 mode can be used as I/O ports.

Table 15.16 Combinations of Pin Functions and General Registers for PWM2 Mode

Pin Name	I/O	Compare Match Register	Buffer Register
TRCIOA	I/O	Port function (1)/TRCTRG input	
TRCIOB	O	TRCGRB register	TRCGRD register
		TRCGRC register	—
TRCIOC	I/O	Port function (1)	
TRCIOD			

Note:
1. To use the port function, set the corresponding bit in registers PMLi and PMHi (i = 1, 3, or 4) to 0.



Note:
1. The above applies when the BUFEB bit in the TRCMR register is 1 (TRCGRD register is used as a buffer register for TRCRGB register).

Figure 15.12 Block Diagram in PWM2 Mode

• When the OPE bit in the TRCOPR register is 1 (waveform output manipulation control enabled), bits OPOL1 to OPOL0 are 11b (timer RC output level is fixed at high during waveform output manipulation period), and the RESTATS bit is 1 (output is automatically restarted).

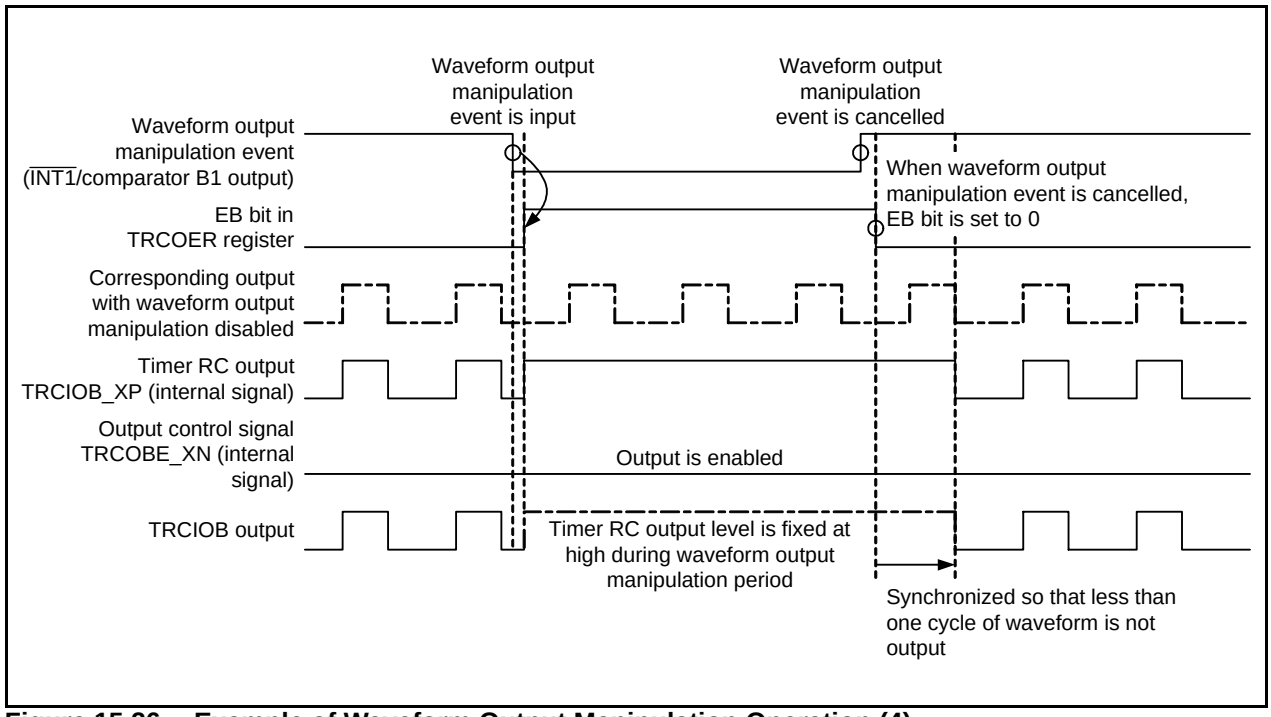


Figure 15.26 Example of Waveform Output Manipulation Operation (4)

15.7 Notes on Timer RC

15.7.1 TRCCNT Register

The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A).

- When writing a value to the TRCCNT register by a program while the CTS bit in the TRCMR register is set to 1 (count is started), ensure that the write timing does not coincide with when the TRCCNT register is set to 0000h.
- If the timing when the TRCCNT register is set to 0000h and is written coincide with each other, the value is not be written and the TRCCNT register is set to 0000h.

If the TRCCNT register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.W   #XXXXh, TRCCNT      ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.W   TRCCNT, DATA        ; Read
```

15.7.2 TRCCR1 Register

To set bits CKS2 to CKS0 in the TRCCR1 register to 110b (fHOCO), set fHOCO to the clock frequency higher than the system clock frequency.

15.7.3 TRCSR Register

If the TRCSR register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.B   #XXh, TRCSR         ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.B   TRCSR, DATA         ; Read
```

15.7.4 Count Source Switching

When switching the count sources, stop the count before switching. After switching the count sources, wait for at least two cycles of the system clock before writing to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Write to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

When changing the count source from fHOCO to another source and stopping fHOCO, wait for at least two cycles of the system clock after changing the clock setting before stopping fHOCO.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Set the HOCOE bit in the OCOCR register to 0 (high-speed on-chip oscillator off).

16.2.6 UART0 Receive Buffer Register (U0RB)

Address 00086h (U0RBL)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Address 00087h (U0RBH)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Receive data (D8 to D0)		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—			R
b7	—			R
b8	—			R
b9	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error has occurred 1: An overrun error has occurred	R
b13	FER	Framing error flag (1, 2)	0: No framing error has occurred 1: A framing error has occurred	R
b14	PER	Parity error flag (1, 2)	0: No parity error has occurred 1: A parity error has occurred	R
b15	SUM	Error sum flag (1, 2)	0: No error has occurred 1: An error has occurred	R

Notes:

1. Bits OER, FER, PER, and SUM are set to 0 (no error has occurred) when bits SMD2 to SMD0 in the U0MR register are set to 000b (serial interface disabled) or the RE bit in the U0C1 register is set to 0 (reception disabled).
   The SUM bit is set to 0 (no error has occurred) when all of bits OER, FER, and PER are set to 0 (no error has occurred). In addition, bits FER and PER are set to 0 when the U0RBH register is read.
   When setting bits SMD2 to SMD0 in the U0MR register to 000b, set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are invalid when bits SMD2 to SMD0 in the U0MR register are set to 001b (clock synchronous serial I/O mode). When these bits are read, the values are undefined.

The U0RB register must be read in 16-bit units. Do not access this register in 8-bit units. When this register is accessed as 16-bit units, it is accessed twice in 8-bit units.

16.3.2 Clock Asynchronous Serial I/O (UART) Mode

In clock asynchronous serial I/O mode, transmission and reception are performed at an arbitrary bit rate and in an arbitrary format.
Table 16.6 lists the Clock Asynchronous Serial I/O Mode Specifications. Table 16.7 lists the Registers and Settings Used in Clock Asynchronous Serial I/O Mode.

Table 16.6 Clock Asynchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Character bits (transfer data): Selectable from 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable from odd, even, or none • Stop bits: Selectable from 1 or 2 bits
Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fj/16 (n + 1) fj = f1, f8, or f32 n = Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT/16 (n + 1) fEXT (input from the CLK0 pin) n = Value set in the U0BRG register (00h to FFh)
Transmit start conditions	To start transmission, the following requirements must be met: • The TE bit in the U0C1 register must be 1 (transmission enabled). • The TI bit in the U0C1 register must be 0 (data present in the U0TB register).
Receive start conditions	To start reception, the following requirements must be met: • The RE bit in the U0C1 register must be 1 (reception enabled). • Start bit detection
Interrupt request generation timing	• For transmission: One of the following can be selected. - The U0IRS bit in the U0C1 register is 0 (transmit buffer is empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit in the U0C1 register is 1 (transmission is completed): When data transmission from the UART0 transmit register is completed. • For reception: When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the next data reception is started and the next to last bit is received before the U0RB register is read. • Framing error This error occurs when the set number of stop bits is not detected. (2) • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. (2) • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

Notes:
1. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register is undefined. The U0RIF bit in the U0IR register remains unchanged.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART0 receive register to the U0RB register.

16.4 UART0 Interrupt

The UART0 interrupt requests are the transmit buffer empty or transmit complete interrupt, and the receive complete interrupt.
Table 16.9 lists the Interrupt Requests.

Table 16.9 Interrupt Requests

Interrupt Request	Interrupt Generation Condition
Transmit buffer empty	U0TIF = 1 (transmit interrupt requested) and U0TIE = 1 (transmit interrupt enabled)
Transmit complete	
Receive complete	U0RIF = 1 (receive interrupt requested) and U0RIE = 1 (receive interrupt enabled)

U0TIF, U0TIE, U0RIF, U0RIE: Bits in U0IR register
Note:
1. The CPU executes interrupt exception handling when the interrupt generation conditions are met and the I flag in the FLG register is 1.

17.2.4 A/D Control Register 0 (ADCON0)

Address 0009Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start bit	0: A/D conversion stops 1: A/D conversion starts	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The ADCON0 register is used to control A/D conversion operation.

ADST Bit (A/D conversion start bit)

The ADST bit is used to start or stop A/D conversion.

[Conditions for setting to 0]
- When A/D conversion is completed in one-shot mode or single sweep mode.
- When 0 is written to this bit by software. (A/D conversion stops)

[Conditions for setting to 1]
- When 1 is written to this bit by software. (A/D conversion starts)
- When the A/D conversion start trigger enabled by the TRCADCR register is input.
- When an external trigger ($\overline{\text{ADTRG}}$) is input.

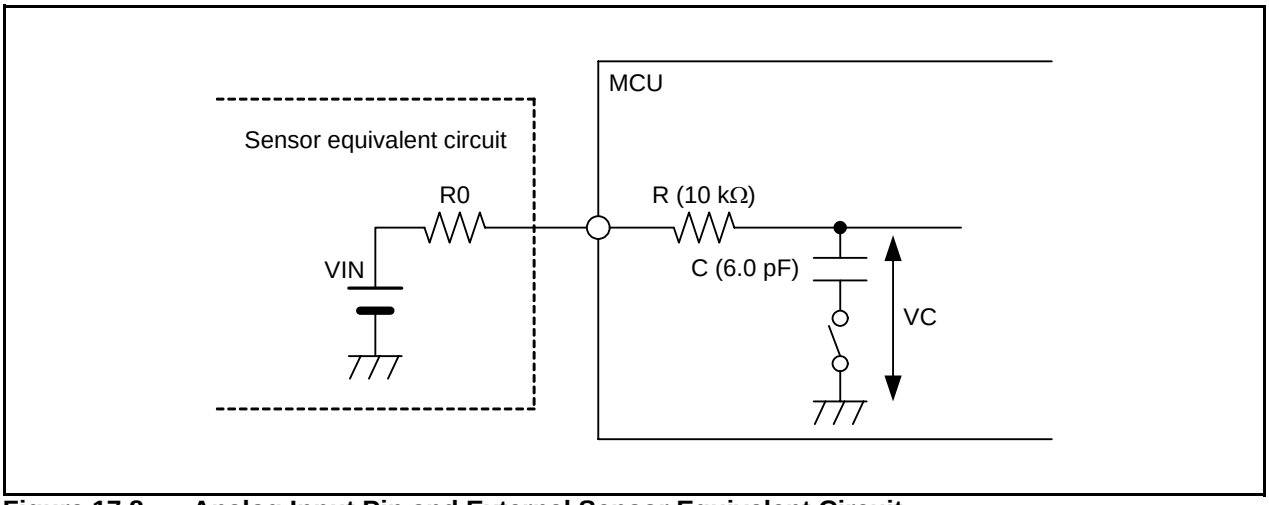


Figure 17.8 Analog Input Pin and External Sensor Equivalent Circuit

17.5.3 Register Setting

- Registers ADMOD and ADINSEL must be written only when A/D conversion is stopped.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion while the WCKSTP bit in the CKSTPR register is 1 (system clock is stopped in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory is stopped) or the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled) during A/D conversion.
- During A/D conversion, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate the conversion, the conversion result from the A/D converter will be undefined and no interrupt will be generated. The value of the ADi register (i = 0 or 1) which is not engaged in A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use any of the values of the ADi register.
- When using the A/D converter, it is recommended that the average of the conversion results be taken.

18.2.2 Comparator B1 Interrupt Control Register (WCB1INTR)

Address 00181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WCB1F	WCB1INTEN	WCB1S1	WCB1S0	—	—	WCB1F1	WCB1F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WCB1F0	Comparator B1 filter select bits	b1 b0 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b1	WCB1F1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	WCB1S0	Comparator B1 interrupt edge select bits	b5 b4 0 0: When the analog input voltage is lower than the reference input voltage 0 1: When the analog input voltage is higher than the reference input voltage 1 0: Do not set. 1 1: When the analog input voltage is lower or higher than the analog input voltage	R/W
b5	WCB1S1			R/W
b6	WCB1INTEN	Comparator B1 interrupt enable signal bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b7	WCB1F	Comparator B1 interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W

WCB1F Bit (Comparator B1 interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit.
[Condition for setting to 1]
• When an interrupt request is generated.

19.6.6.4 Block Erase

When 20h is written as the first command and then D0h is written to any address in the block with the second command, an auto-erase (erase and erase-verify operation) is started in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erase is completed. The FST7 bit is set to 0 during auto-erase and changed to 1 when auto-erase is completed. After auto-erase completes, all data in the block is set to FFh.
After auto-erase is completed, the result can be confirmed by the FST5 bit in the FST register (see **19.6.7 Full Status Check**).
For each block in the program ROM, the program erase command can be disabled using the lock bit.
When the FMR16 bit in the FMR1 register is 1 (rewrite disabled), the block erase command for block A of data flash is not accepted. When the FMR17 bit is 1 (rewrite disabled), the block erase command for block B is not accepted.
Figure 19.12 shows the Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled). Figure 19.13 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled). Figure 19.14 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled). Figure 19.15 shows the Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled).

In EW1 mode, do not execute this command for the block where the rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled), a flash ready status interrupt is generated when auto-erase is completed. When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled) and the FMR20 bit in the FMR2 register is 1 (suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (suspend request) and auto-erase is suspended. The result can be confirmed by reading the FST register in the interrupt routine.

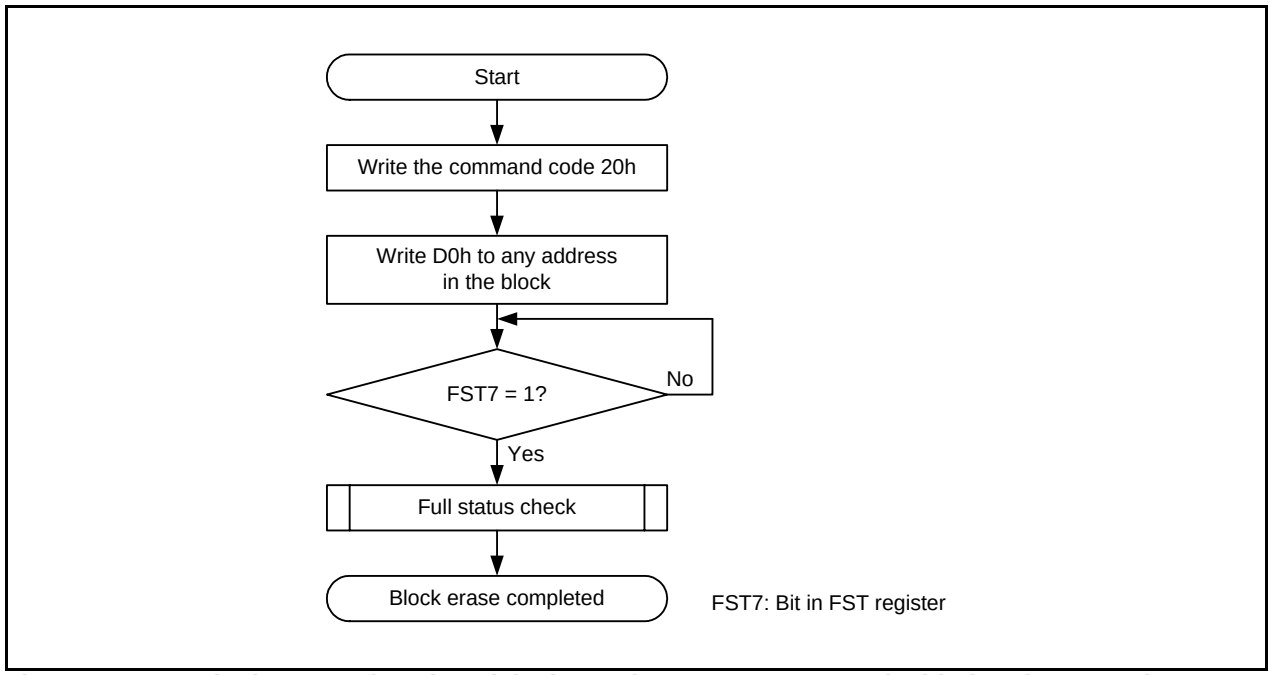


Figure 19.12 Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled)

19.8 Notes on Flash Memory

19.8.1 ID Code Area Setting Example

The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set 55h in all of the ID code area

```
.org 00FFDCH
.lword dummy | (55000000h)      ; UND
.lword dummy | (55000000h)      ; INTO
.lword dummy                    ; BREAK
.lword dummy | (55000000h)      ; ADDRESS MATCH
.lword dummy | (55000000h)      ; SET SINGLE STEP
.lword dummy | (55000000h)      ; WDT
.lword dummy | (55000000h)      ; RESERVE
.lword dummy | (55000000h)      ; RESERVE
```

Programming formats vary depending on the compiler. Check the compiler manual.

21.7 Notes on Timer RJ2

(1) Timer RJ2 stops counting after a reset. Start the count only after setting the value in the timer.

(2) After 1 (count is started) is written to the TSTART bit in the TRJCR register while the count is stopped, the TCSTF bit in the TRJCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started from the first active edge of the count source after the TCSTF bit is set to 1. After 0 (count is stopped) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 0.
Note:
1. Registers associated with timer RJ2: TRJ, TRJCR, TRJIOC, and TRJMR

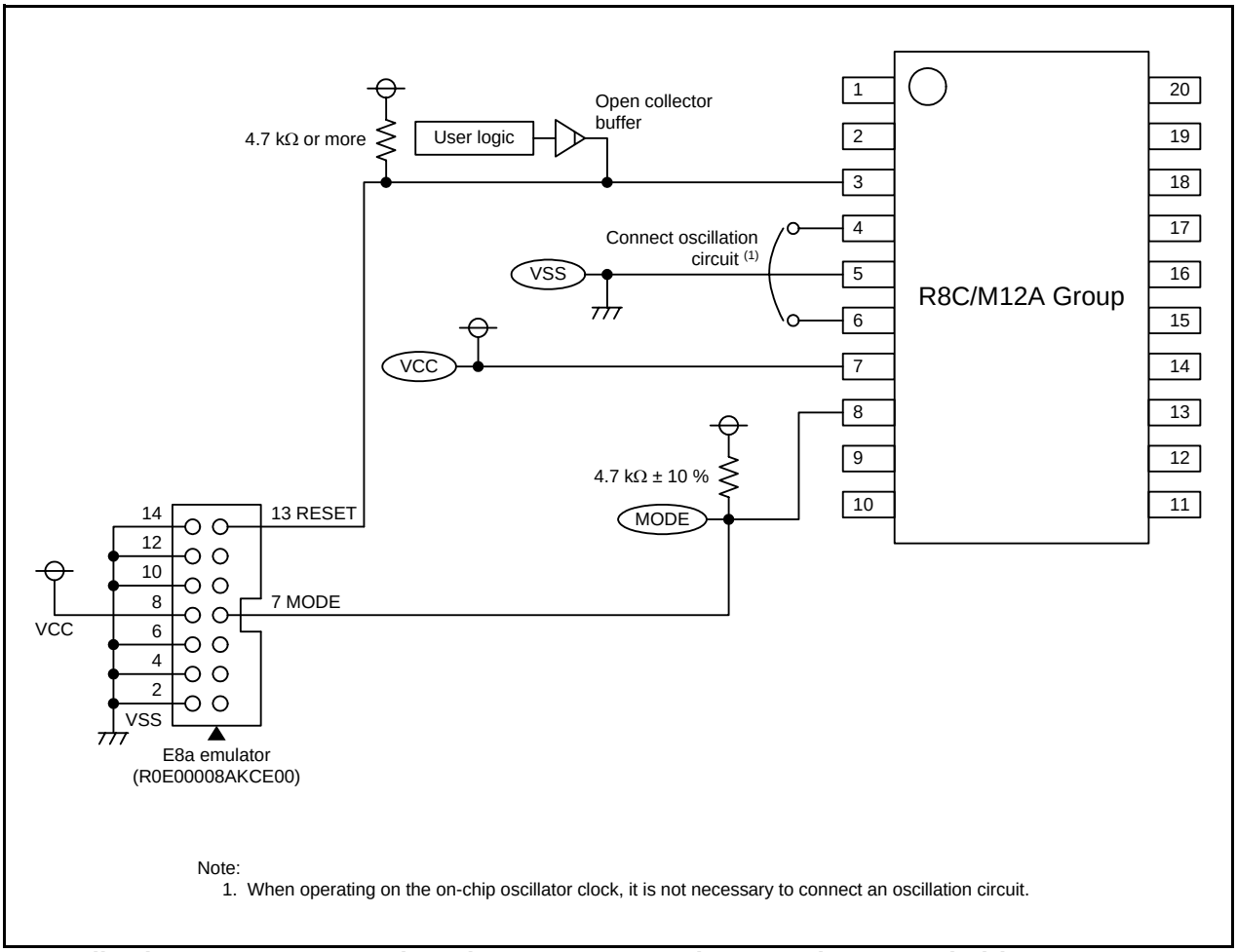
(3) In event counter mode, set the TSTART bit in the TRJCR register to 1 (count is started) and then input an external pulse.

(4) In pulse width/pulse period measurement modes, bits TEDGF and TUNDF in the TRJCR register used are set to 0 by writing 0 by a program but remain unchanged even if 1 is written to these bits. If a read-modify-write instruction is used to set the TRJCR register, bits TEDGF and TUNDF may be erroneously set to 0 depending on the timing, even when the TEDGF bit is set to 1 (active edge received) and the TUNDF bit is set to 1 (underflow) during execution of the instruction.
In this case, write 1 using the MOV instruction to the TEDGF or TUNDF bit which is not supposed to be set to 0.

(5) Insert NOP instructions between writing to and reading from registers associated with the TRJ counter while the counter is stopped.

(6) When the TSTART bit in the TRJCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), allow at least three cycles of the count source clock for each write interval when writing to the TRJ register successively.

(7) Note the following when writing 0 to the TEDGF bit in the TRJCR register in pulse width measurement mode or pulse period measurement mode.
Set the TRJIF bit in the TRJIR register to 0 before setting the TEDGF bit to 0.
When reading the TEDGF bit immediately after setting it to 0, it is read as 0. However the internal signal of the TEDGF bit remains 1 for one to two cycles of the count source. If an active edge is input during this period, the internal signal of the TEDGF bit does not become 0 and the TEDGF bit is read as 1.
Since the TRJIF bit becomes 1 when the internal signal of the TEDGF bit changes from 0 to 1, the TRJIF bit does not become 1 and no interrupt is generated.
After setting the TEDGF bit to 0, confirm that 0 can be read after waiting for three or more count source cycles in order to accept the next interrupt request.



Note:
1. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Appendix Figure 2.4 E8a Emulator (R0E00008AKCE00) Connection Example (2)

Appendix 4. Comparison between R8C/M12A Group and R8C/M13B Group

Appendix Table 4.1 lists Specification Comparison between R8C/M12A Group and R8C/M13B Group.
For details on the R8C/M13B Group specifications, refer to the R8C/M13B Group User's Manual: Hardware.

Appendix Table 4.1 Specification Comparison between R8C/M12A Group and R8C/M13B Group

Item	Function	R8C/M12AGroup	R8C/M13B Group
Memory	ROM	2 KB, 4 KB, 8 KB	4 KB, 8 KB, 16 KB
	RAM	256 bytes, 384 bytes, 512 bytes	384 bytes, 512 bytes, 1K byte
Clock generation circuit	XCIN clock generation circuit	Not available	Available
I/O port	Number of pins	20	32 Added ports: P2_2/TRCIOD/TRKI/SSO/SDA P2_1/TRCIOC/TRKO/SSCK/SCL P2_0/TRCIOB/TRKO/INT1 P3_1/XIN/TRBO P0_7/TRCIOC/TRKO P0_6/TRCIOD P0_5/TRCIOB P0_4/TRCIOB/TREO P0_3/TRCIOB/CLK1 P0_2/TRCIOA/TRCTRG/RXD1/IrRXD P0_1/TRCIOA/TRCTRG/TXD1/IrTXD P0_0/TRCIOA/TRCTRG
	Number of CMOS I/O ports	17	29 Added ports: P2_2, P2_1, P2_0, P3_1, P0_7, P0_6, P0_5, P0_4, P0_3, P0_2, P0_1, P0_0
Timer	Timer RE2	Not available	Available
	Timer RK	Not available	Available
Serial interface	UART1	Not available	Available
Clock synchronous serial interface	IIC/SSU	Not available	Available
IrDA interface		Not available	Available
A/D converter	Number of A/D channels	6 channels	8 channels Added channels: AN5, AN6
Package		20-pin LSSOP 20-pin DIP	32-pin LQFP

REVISION HISTORY	R8C/M11A Group, R8C/M12A Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Nov 30, 2010	68	Table 8.3 revised, Notes 2 and 3 deleted
		69	Table 8.4 Notes 1 to 3 deleted
		70	Table 8.5 revised, Note 1 added, and Figure 8.3 revised
		71	8.4 revised
		72 to 90	"9. Clock Generation Circuit" revised
		91, 379	9.6, 21.3 revised
		92 to 106	"10. Power Control" revised
		107, 380	10.6, 21.4 revised
		108	Table 11.1 revised
		111	11.2.1 Note 1 added
		113	11.2.4 Note 1 revised
		115	11.2.6 and 11.2.7 revised
		116	11.2.8 revised
		118	11.2.10 and 11.2.11 "The resister remains ... or software reset." added
		119	Table 11.5 "0FFE7h" → "0FFE6h"
		121	11.4.2 revised, Table 11.7 added
		122	11.4.3 revised
		123	11.4.4 (1) revised
		125	11.4.7 revised
		128	Figure 11.8 Note 1 deleted
		129	11.5.1 revised
		130	11.5.2 and Figure 11.9 revised
		131	Figure 11.11 revised
		132	11.7 revised
		133	Figure 11.12 revised
		135, 382	11.9.4,21.5.4, Figure 11.13, and Figure 21.1 revised
		136, 383	11.9.5, 21.5.5 revised, Figure 11.14, Figure 21.2 added
		137, 384	11.9.6, 21.5.6, Figure 11.15, Figure 21.3 added
		140	12.2 and 12.2.1 revised
		142	12.3.2 revised
		143	12.3.4 Note 1 added
		148	Tables 12.9 and 12.10 revised
		150	12.4.2 revised
		151	12.4.4 Note 1 added
		154	Table 12.15 revised
		156	12.5.2 revised
		160	Table 12.16, Table 12.18, and Table 12.19 revised
		162	12.6.2 revised
		163	12.7 added
		166	Figure 12.6 revised, Figure 12.7 added
		167	Figure 12.9 revised
		168	Figure 12.10 revised