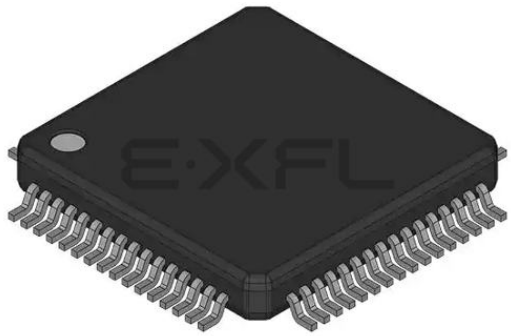

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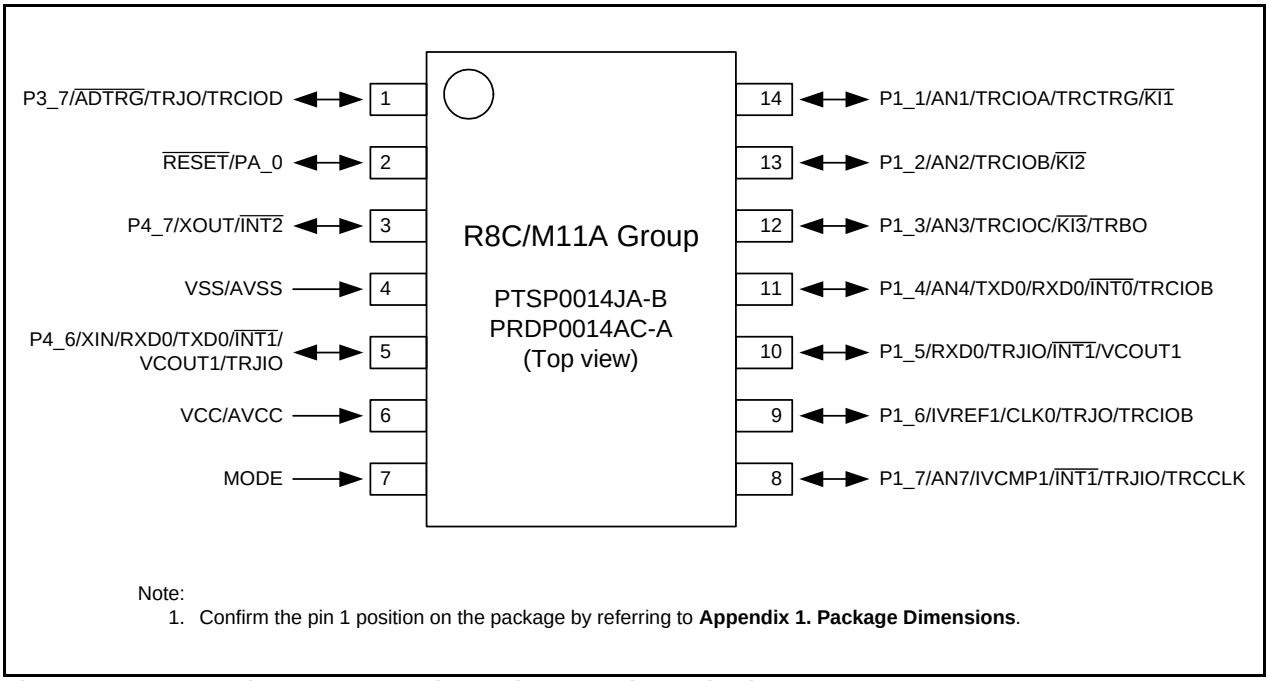
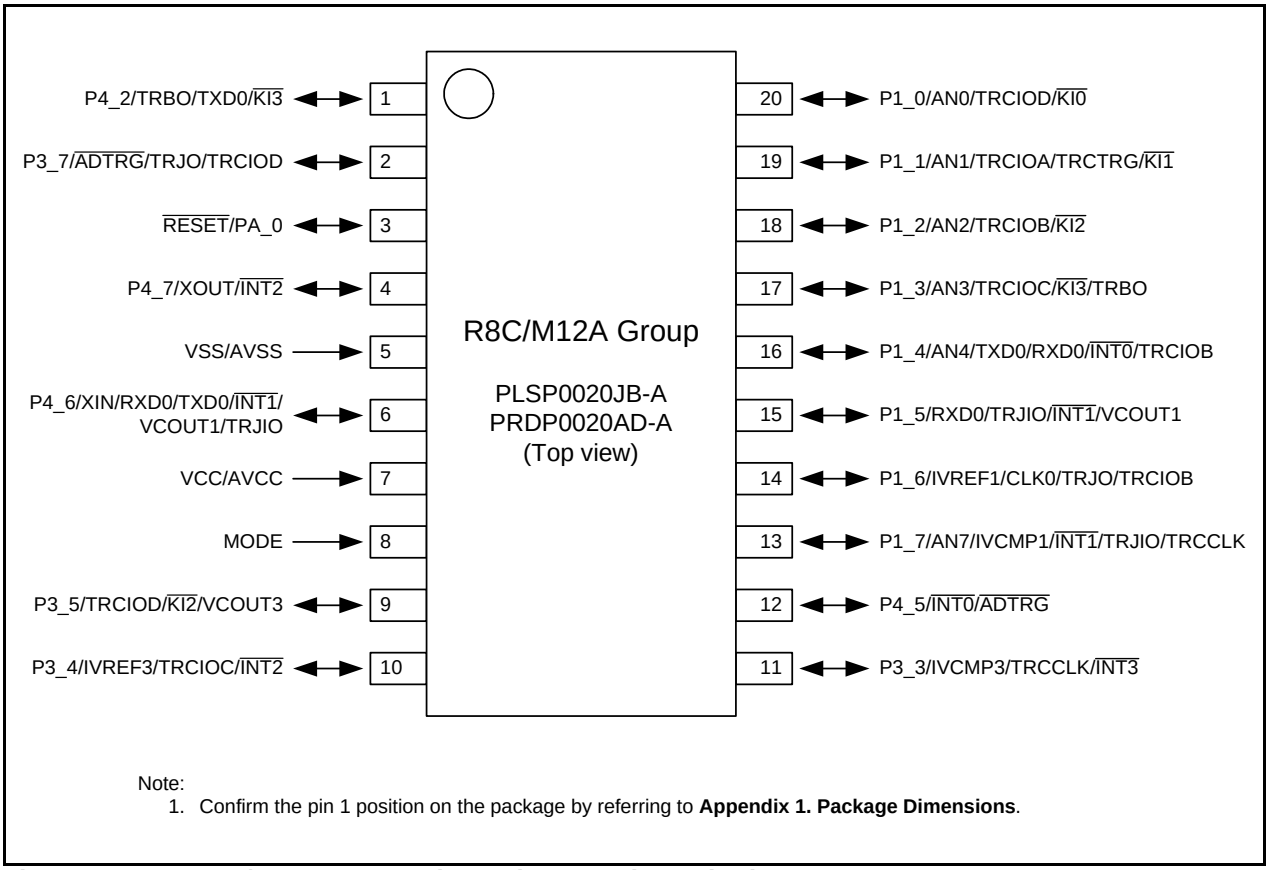
1.4 Pin Assignment

Figures 1.3 and 1.4 show Pin Assignment (Top View). Table 1.6 lists the Pin Name Information by Pin Number.



Note:
1. Confirm the pin 1 position on the package by referring to **Appendix 1. Package Dimensions**.

Figure 1.3 R8C/M11A Group Pin Assignment (Top View)



Note:
1. Confirm the pin 1 position on the package by referring to **Appendix 1. Package Dimensions**.

Figure 1.4 R8C/M12A Group Pin Assignment (Top View)

Table 3.3 SFR Information (3) (1)

Address	Register Name	Symbol	After Reset
0007Ah			
0007Bh			
0007Ch			
0007Dh			
0007Eh			
0007Fh			
00080h	UART0 Transmit/Receive Mode Register	U0MR	00h
00081h	UART0 Bit Rate Register	U0BRG	XXh
00082h	UART0 Transmit Buffer Register	U0TBL	XXh
00083h		U0TBH	XXh
00084h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00085h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00086h	UART0 Receive Buffer Register	U0RBL	XXh
00087h		U0RBH	XXh
00088h	UART0 Interrupt Flag and Enable Register	U0IR	00h
00089h			
0008Ah			
0008Bh			
0008Ch			
0008Dh			
0008Eh			
0008Fh			
00090h			
00091h			
00092h			
00093h			
00094h			
00095h			
00096h			
00097h			
00098h	A/D Register 0	AD0L	XXh
00099h		AD0H	000000XXb
0009Ah	A/D Register 1	AD1L	XXh
0009Bh		AD1H	000000XXb
0009Ch	A/D Mode Register	ADMOD	00h
0009Dh	A/D Input Select Register	ADINSEL	00h
0009Eh	A/D Control Register 0	ADCON0	00h
0009Fh	A/D Interrupt Control Status Register	ADICSR	00h
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h			
000A9h	Port P1 Direction Register	PD1	00h
000AAh			
000ABh	Port P3 Direction Register	PD3	00h
000ACh	Port P4 Direction Register	PD4	00h
000ADh	Port PA Direction Register	PDA	00h
000AEh			
000AFh	Port P1 Register	P1	00h
000B0h			
000B1h	Port P3 Register	P3	00h
000B2h	Port P4 Register	P4	00h
000B3h	Port PA Register	PA	00h
000B4h			
000B5h	Pull-Up Control Register 1	PUR1	00h
000B6h			
000B7h	Pull-Up Control Register 3	PUR3	00h
000B8h	Pull-Up Control Register 4	PUR4	00h
000B9h	Port I/O Function Control Register	PINSR	00h
000BAh			
000BBh	Drive Capacity Control Register 1	DRR1	00h
000BCh			
000BDh	Drive Capacity Control Register 3	DRR3	00h
000BEh			
000BFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.9 ID Code Area and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
0FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
0FFDFh	ID1		(Note 2)
:			
0FFE3h	ID2		(Note 2)
:			
0FFEBh	ID3		(Note 2)
:			
0FFEFh	ID4		(Note 2)
:			
0FFF3h	ID5		(Note 2)
:			
0FFF7h	ID6		(Note 2)
:			
0FFFBh	ID7		(Note 2)
:			
0FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the option function select area. Erasure of the block including the option function select area causes the option function select area to be set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the ID code area. Erasure of the block including the ID code area causes the ID code area to be set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5.2.1 Processor Mode Register 0 (PM0)

Address 00010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	SRST	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	SRST	Software reset bit	0: State is retained 1: Reset is generated	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

SRST Bit (Software reset bit)

When the SRST bit is set to 1, the entire MCU is reset. The read value is 0. For details, see **6. Resets**.

6.2.2 Reset Source Determination Register (RSTFR)

Address 0005Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDR	SWR	HWR	CWR
After Reset	0	0	0	0	X (1)	X (1)	X (1)	X (1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. The value after a reset differs depending on the reset source.

CWR Bit (Cold start-up/warm start-up determine flag)

This flag indicates whether a cold start-up or warm start-up has occurred. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
The CWR bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.

[Condition for setting to 0]
• When a reset occurs after power-on or voltage detection 0.
[Condition for setting to 1]
• When 1 is written to this bit by a program.

HWR Bit (Hardware reset detect flag)

This flag indicates that a hardware reset has occurred.

[Condition for setting to 0]
• When a software reset, watchdog timer reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a hardware reset occurs.

SWR Bit (Software reset detect flag)

This flag indicates that a reset has been generated by software.

[Condition for setting to 0]
• When a watchdog timer reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a software reset occurs.

6.3.4 Voltage Monitor 0 Reset

The voltage monitor 0 reset is due to the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the voltage applied to the VCC pin. Vdet0 is the detection level. The Vdet0 level is set with bits VDSEL0 to VDSEL1 in the OFS register.

When the input voltage to the VCC pin falls to the Vdet0 level or lower, the CPU, SFRs and I/O ports are initialized. The internal RAM is not initialized. If the supply voltage falls to Vdet0 or lower while writing to the internal RAM, the RAM values will be undefined.

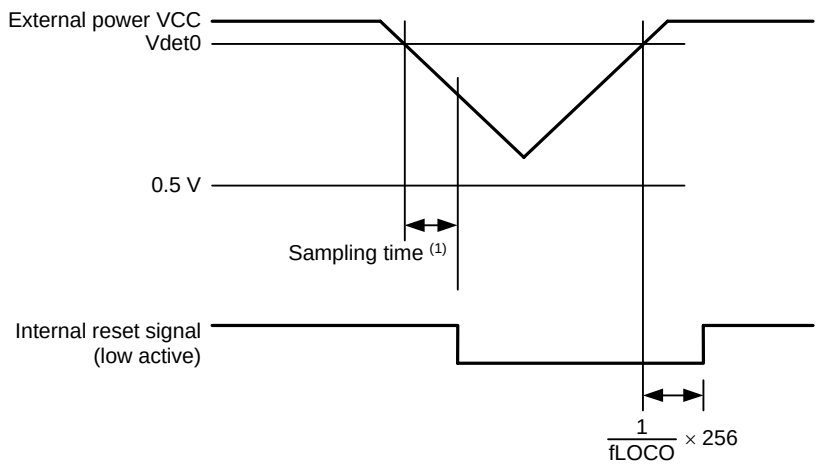
When the voltage applied to the VCC pin next rises to the Vdet0 level or higher, counting of the low-speed on-chip oscillator clock starts. When the low-speed on-chip oscillator clock count reaches 256, the internal reset signal goes high and the MCU proceeds to the reset sequence (see Figure 6.2). The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset.

The LVDAS bit in the OFS register can be used to enable or disable the voltage monitor 0 reset after a reset. The setting of the LVDAS bit is valid at all resets.

Bits VDSEL0 to VDSEL1, and LVDAS cannot be changed by a program. To change these bits, write values to b4 to b6 at address 0FFFFh using a flash programmer. For details on the OFS register, see **6.2.4 Option Function Select Register (OFS)**.

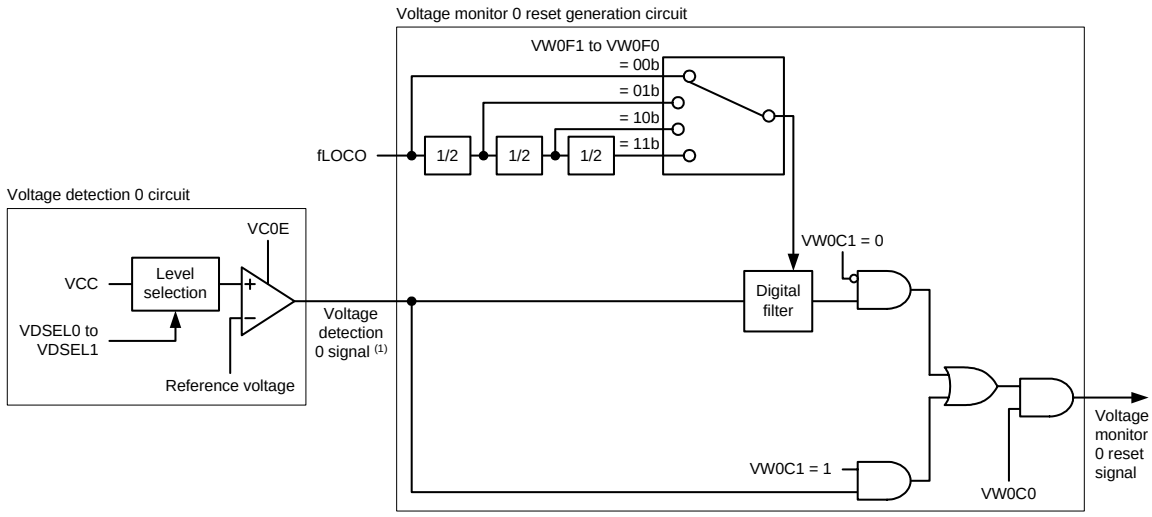
For details on the voltage monitor 0 reset, see **7. Voltage Detection Circuit**.

Figure 6.5 shows an Example of Voltage Monitor 0 Reset Operation.



Note:
1. The voltage monitor 0 digital filter samples VCC to monitor the voltage. If VCC falls below the operating voltage range (1.8 V or more), the voltage cannot be correctly measured. This factor should be considered when selecting the sampling clock for the digital filter. For details, see **7. Voltage Detection Circuit**.

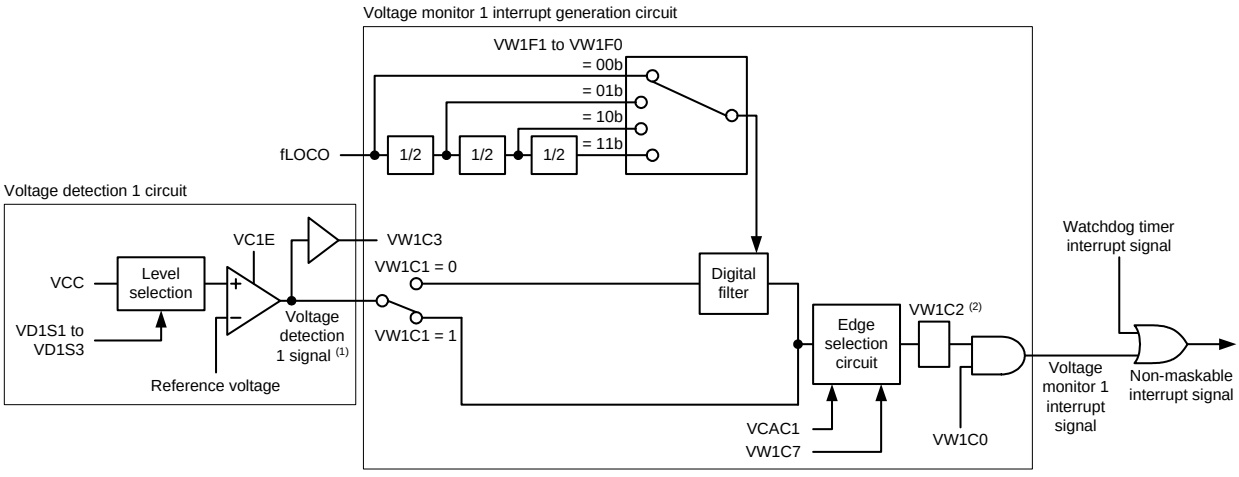
Figure 6.5 Example of Voltage Monitor 0 Reset Operation



VC0E: Bit in VCA2 register
VW0C0, VW0C1, VW0F0 to VW0F1: Bits in VW0C register
VDSEL0 to VDSEL1: Bits in OFS register

Note:
1. When the VC0E bit is 0 (voltage detection 0 circuit disabled), the voltage detection 0 signal will be high.

Figure 7.2 Voltage Monitor 0 Reset Generation Circuit Block Diagram



VCAC1: Bit in VCAC register
VC1E: Bit in VCA2 register
VD1S1 to VD1S3: Bits in VD1LS register
VW1C0, VW1C1, VW1C2, VW1C3, VW1F0 to VW1F1, VW1C7: Bits in VW1C register

Notes:
1. When the VC1E bit is 0 (voltage detection 1 circuit disabled), the voltage detection 1 signal will be high.
2. The VW1C2 bit is set to 0 by writing 0 by a program. When the VC1E bit is 0 (voltage detection 1 circuit disabled), the VW1C2 bit will be 0 (not detected).

Figure 7.3 Voltage Monitor 1 Interrupt Generation Circuit Block Diagram

7.2.3 Voltage Detection 1 Level Select Register (VD1LS)

Address 0005Bh

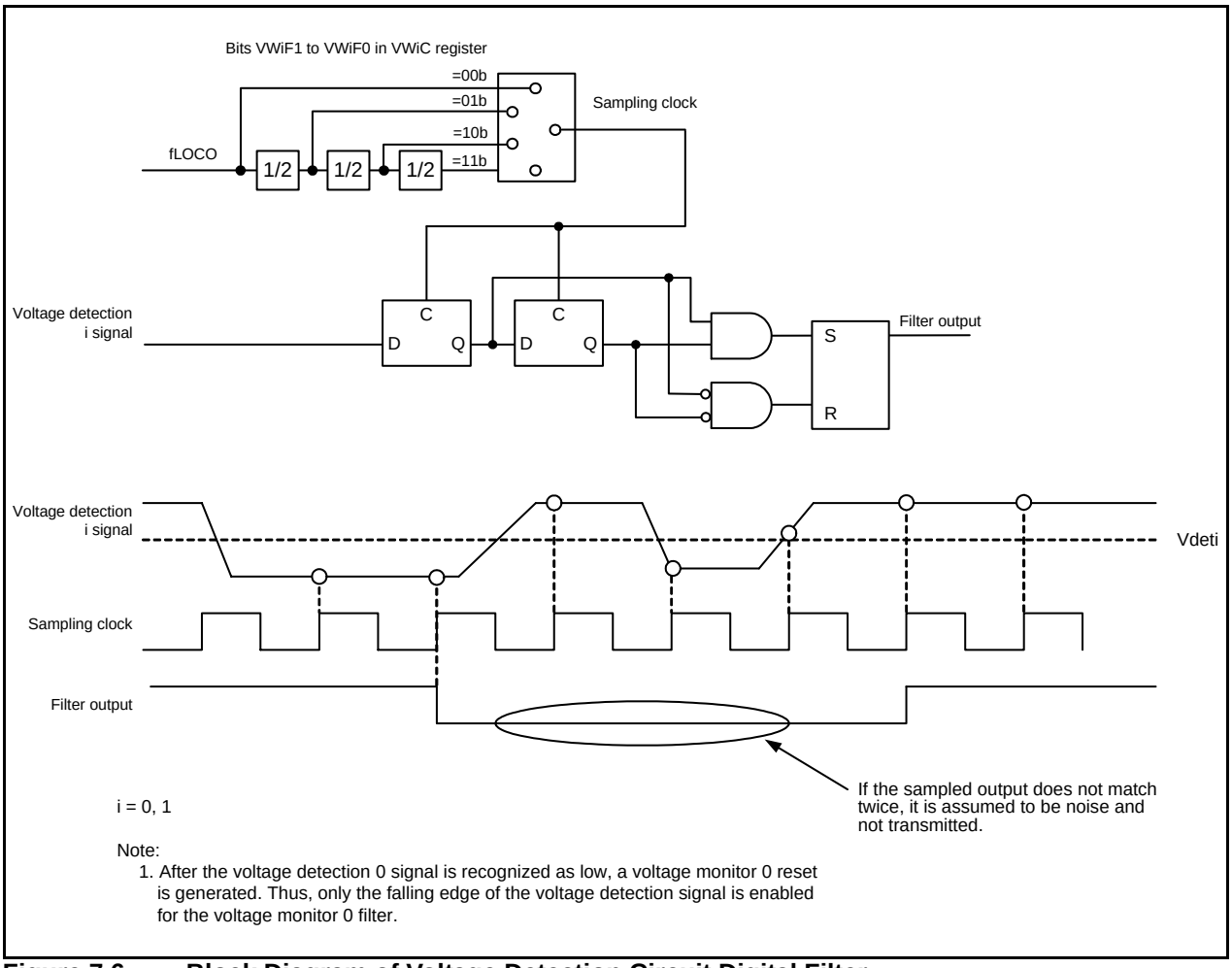
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	—
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 1.	R/W
b1	VD1S1	Voltage detection 1 level select bits	b3 b2 b1 0 0 0: 2.35 V (Vdet1_1) 0 0 1: 2.65 V (Vdet1_3) 0 1 0: 2.95 V (Vdet1_5) 0 1 1: 3.25 V (Vdet1_7) 1 0 0: 3.55 V (Vdet1_9) 1 0 1: 3.85 V (Vdet1_B) 1 1 0: 4.15 V (Vdet1_D) 1 1 1: 4.45 V (Vdet1_F)	R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

7.6 Digital Filter for Voltage Detection Circuits 0 and 1

Figure 7.6 shows a Block Diagram of Voltage Detection Circuit Digital Filter. In digital filter enabled mode, the voltage detection signal from the voltage detection circuit is used to generate a voltage monitor 0 reset signal and a voltage monitor 1 interrupt signal individually through the digital filter circuit. The filter width of the digital filter circuit is the sampling clock × 2.



Note:
1. After the voltage detection 0 signal is recognized as low, a voltage monitor 0 reset is generated. Thus, only the falling edge of the voltage detection signal is enabled for the voltage monitor 0 filter.

Figure 7.6 Block Diagram of Voltage Detection Circuit Digital Filter

9.2.3 System Clock f Control Register (SCKCR)

Address 00022h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	HSCKSEL	WAITM	—	—	PHISSEL2	PHISSEL1	PHISSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PHISSEL0	CPU clock division ratio select bits	These bits are used to select the division ratio of the system clock (f) to generate the CPU clock (fs). b2 b1 b0 0 0 0: fs = System clock with no division 0 0 1: fs = System clock divided by 2 0 1 0: fs = System clock divided by 4 0 1 1: fs = System clock divided by 8 1 0 0: fs = System clock divided by 16 1 0 1: fs = System clock divided by 32 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	PHISSEL1			R/W
b2	PHISSEL2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	WAITM	Wait control bit	0: Not in wait mode 1: Wait mode is entered	R/W
b6	HSCKSEL	High-speed on-chip oscillator/XIN clock select bit	0: XIN clock 1: High-speed on-chip oscillator clock	R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the SCKCR register.

Bits PHISSEL0 to PHISSEL2 (CPU clock division ratio select bits)

Bits PHISSEL2 to PHISSEL0 are set to 000b (system clock with no division) if the PHISRS bit in the CKRSCR register is 1 (no division) when the MCU returns from wait mode or stop mode.

WAITM Bit (Wait control bit)

[Condition for setting to 0]
• When a peripheral function interrupt is used to return from wait mode.
[Condition for setting to 1]
• When 1 is written to the WAITM bit after the PRC0 bit in the PRCR register is set to 1 (write enabled).

11.3.2 Relocatable Vector Table

The relocatable vector table occupies 256 bytes beginning from the start address set in the INTB register. Table 11.6 lists the Relocatable Vector Table.

Table 11.6 Relocatable Vector Table

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Priority Level Setting (ILVL0 or ILVL2 to ILVLE)
BRK instruction (2)	+0 to +3 (+00000h to +00003h)	0	—
Flash ready	+4 to +7 (+00004h to +00007h)	1	ILVL05 to ILVL04
Reserved		2 to 3	—
Comparator B1	+16 to +19 (+00010h to +00013h)	4	ILVL21 to ILVL20
Comparator B3	+20 to +23 (+00014h to +00017h)	5	ILVL25 to ILVL24
Reserved	+24 to +27 (+00018h to +0001Bh)	6	—
Timer RC	+28 to +31 (+0001Ch to +0001Fh)	7	ILVL35 to ILVL34
Reserved	+32 to +35 (+00020h to +00023h)	8	—
Reserved	+36 to +39 (+00024h to +00027h)	9	—
Reserved	+40 to +43 (+00028h to +0002Bh)	10	—
Reserved	+44 to +47 (+0002Ch to +0002Fh)	11	—
Reserved	+48 to +51 (+00030h to +00033h)	12	—
Key input	+52 to +55 (+00034h to +00037h)	13	ILVL65 to ILVL64
A/D conversion	+56 to +59 (+00038h to +0003Bh)	14	ILVL71 to ILVL70
Reserved	+60 to +63 (+0003Ch to +0003Fh)	15	—
Reserved		16	—
UART0 transmission	+68 to +71 (+00044h to +00047h)	17	ILVL85 to ILVL84
UART0 reception	+72 to +75 (+00048h to +0004Bh)	18	ILVL91 to ILVL90
Reserved	+76 to +79 (+0004Ch to +0004Fh)	19	—
Reserved	+80 to +83 (+00050h to +00053h)	20	—
$\overline{\text{INT2}}$	+84 to +87 (+00054h to +00057h)	21	ILVLA5 to ILVLA4
Timer RJ2	+88 to +91 (+00058h to +0005Bh)	22	ILVLB1 to ILVLB0
Periodic timer	+92 to +95 (+0005Ch to +0005Fh)	23	ILVLB5 to ILVLB4
Timer RB2	+96 to +99 (+00060h to +00063h)	24	ILVLC1 to ILVLC0
$\overline{\text{INT1}}$	+100 to +103 (+00064h to +00067h)	25	ILVLC5 to ILVLC4
$\overline{\text{INT3}}$	+104 to +107 (+00068h to +0006Bh)	26	ILVLD1 to ILVLD0
Reserved		27 to 28	—
$\overline{\text{INT0}}$	+116 to +119 (+00074h to +00077h)	29	ILVLE5 to ILVLE4
Reserved		30	—
Reserved		31	—
Software (2)	+128 to +131 (+00080h to +00083h) to +252 to +255 (+000FCh to +000FFh)	32 to 63	—

Notes:
1. These addresses are relative to those indicated by the INTB register.
2. These interrupts are not disabled by the I flag.

11.5 $\overline{\text{INT}}$ Interrupt

11.5.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 3)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity can be selected by bits INTiSA to INTiSB in the ISCR0 register. The input pins used as the $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ input can be selected.
Inputs can be passed through a digital filter with three different sampling clocks.
The interrupt by the $\overline{\text{INTi}}$ input can be used as a wakeup function to cancel wait mode or stop mode.
Table 11.11 lists the Pin Configuration for $\overline{\text{INTi}}$ Interrupt.

Table 11.11 Pin Configuration for $\overline{\text{INTi}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P1_4, P4_5	I	$\overline{\text{INT0}}$ interrupt input
$\overline{\text{INT1}}$	P1_5, P1_7, P4_6	I	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P3_4, P4_7	I	$\overline{\text{INT2}}$ interrupt input
$\overline{\text{INT3}}$	P3_3	I	$\overline{\text{INT3}}$ interrupt input

12.3 Port 1

Figure 12.1 shows the Port 1 Pin Configuration.

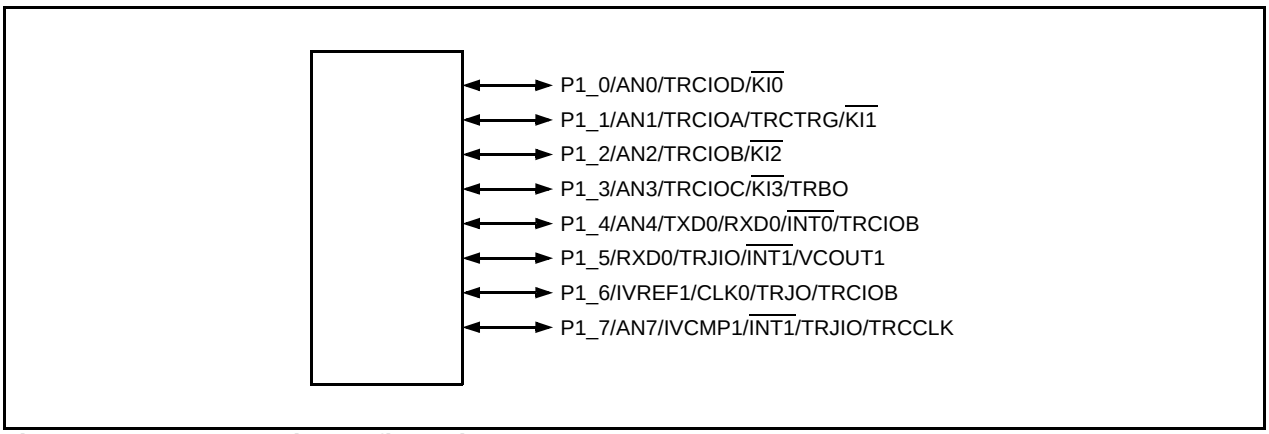


Figure 12.1 Port 1 Pin Configuration

12.3.1 Port P1 Direction Register (PD1)

Address 000A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD1_7	PD1_6	PD1_5	PD1_4	PD1_3	PD1_2	PD1_1	PD1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD1_0	Port P1_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PD1_1	Port P1_1 direction bit		R/W
b2	PD1_2	Port P1_2 direction bit		R/W
b3	PD1_3	Port P1_3 direction bit		R/W
b4	PD1_4	Port P1_4 direction bit		R/W
b5	PD1_5	Port P1_5 direction bit		R/W
b6	PD1_6	Port P1_6 direction bit		R/W
b7	PD1_7	Port P1_7 direction bit		R/W

The PD1 register is used to select whether I/O ports are used as input or output.
Each bit in the PD1 register corresponds to individual ports.

12.3.2 Port P1 Register (P1)

Address 000AFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P1_0	Port P1_0 bit	0: Low level 1: High level	R/W
b1	P1_1	Port P1_1 bit		R/W
b2	P1_2	Port P1_2 bit		R/W
b3	P1_3	Port P1_3 bit		R/W
b4	P1_4	Port P1_4 bit		R/W
b5	P1_5	Port P1_5 bit		R/W
b6	P1_6	Port P1_6 bit		R/W
b7	P1_7	Port P1_7 bit		R/W

The P1 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P1 register. The P1 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pins. Each bit in the P1 register corresponds to individual ports.

12.8 Pin Settings for Peripheral Function I/O

Tables 12.21 to 12.24 list the pin settings for peripheral function I/O.

Table 12.21 TRCIOA Pin Settings

Register	TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	TCEG1	TCEG0	
Setting value	0	1	0	0	1	X	X	Timer mode waveform output (output compare function)
				1	X			
	0	1	1	X	X	X	X	Timer mode (input capture function)
	1							
	1	0	X	X	X	0	1	PWM2 mode (TRCTRG input)
						1	X	

X: 0 or 1

Table 12.22 TRCIOB Pin Settings

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 12.23 TRCIOC Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 12.24 TRCIOD Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

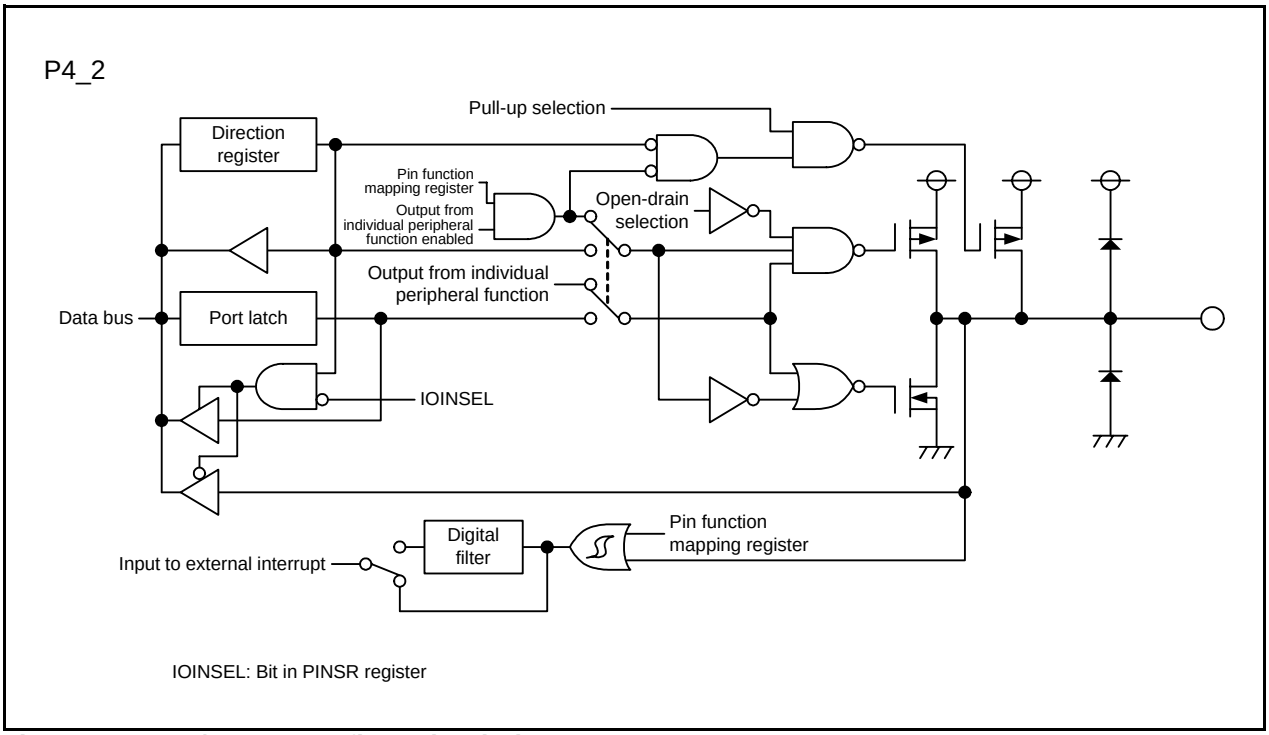


Figure 12.15 I/O Port Configuration (10)

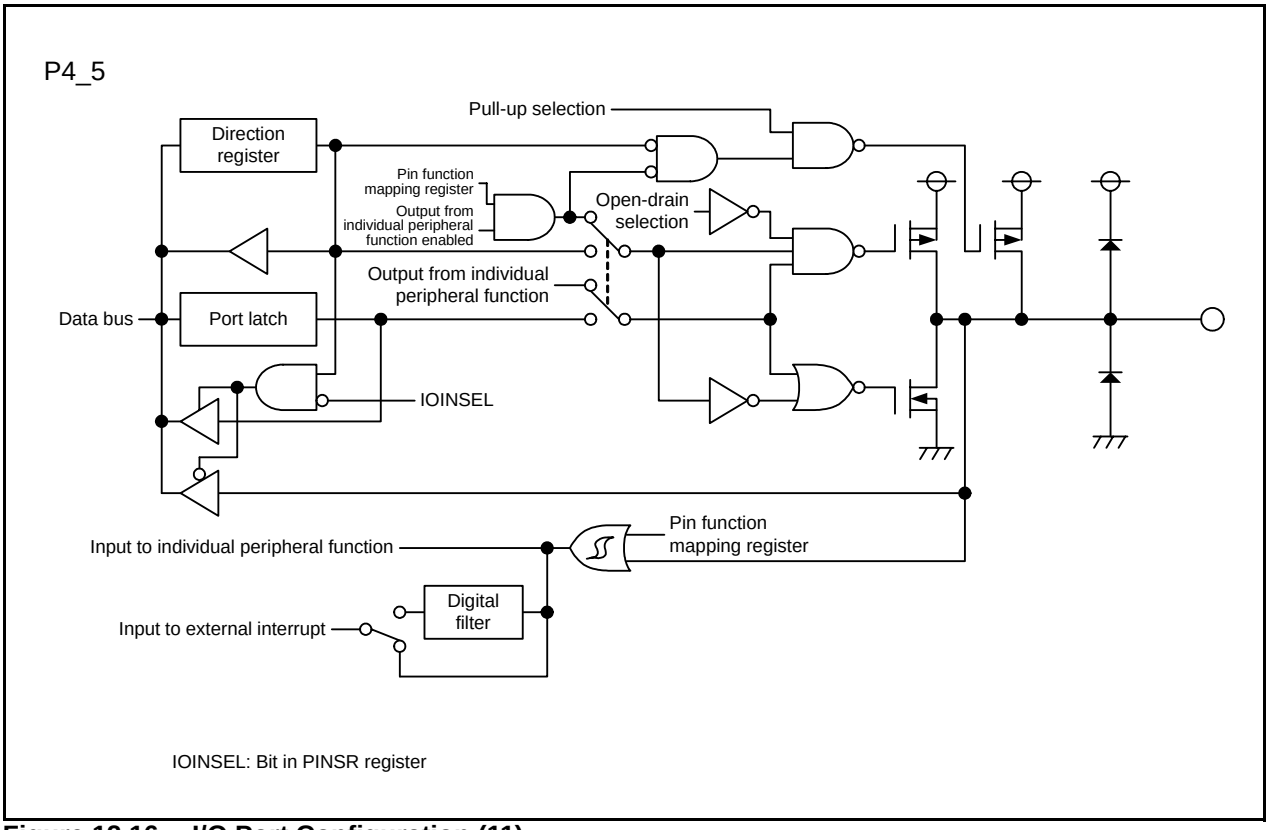


Figure 12.16 I/O Port Configuration (11)

Figure 15.17 shows an Example of One-Shot Pulse Waveform Output Operation in PWM2 Mode.
The count is started when the CTS bit in the TRCMR register is set to 1 (count is started) under the following conditions. Then, the counter is changed to 0000h by a compare match with the TRCGRA register, the count operation is stopped, and a one-shot waveform is output.

- Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG input disabled) to disable the TRCTRG input.
- The CSTP bit in the TRCCR2 register is set to 1 (increment is stopped) to stop the increment when compare match A with the TRCGRA register occurs.
- The CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by compare match A.
- The TOB bit in the TRCCR1 register is set to 0 (output value 0) to set the initial value of the output level to 0.

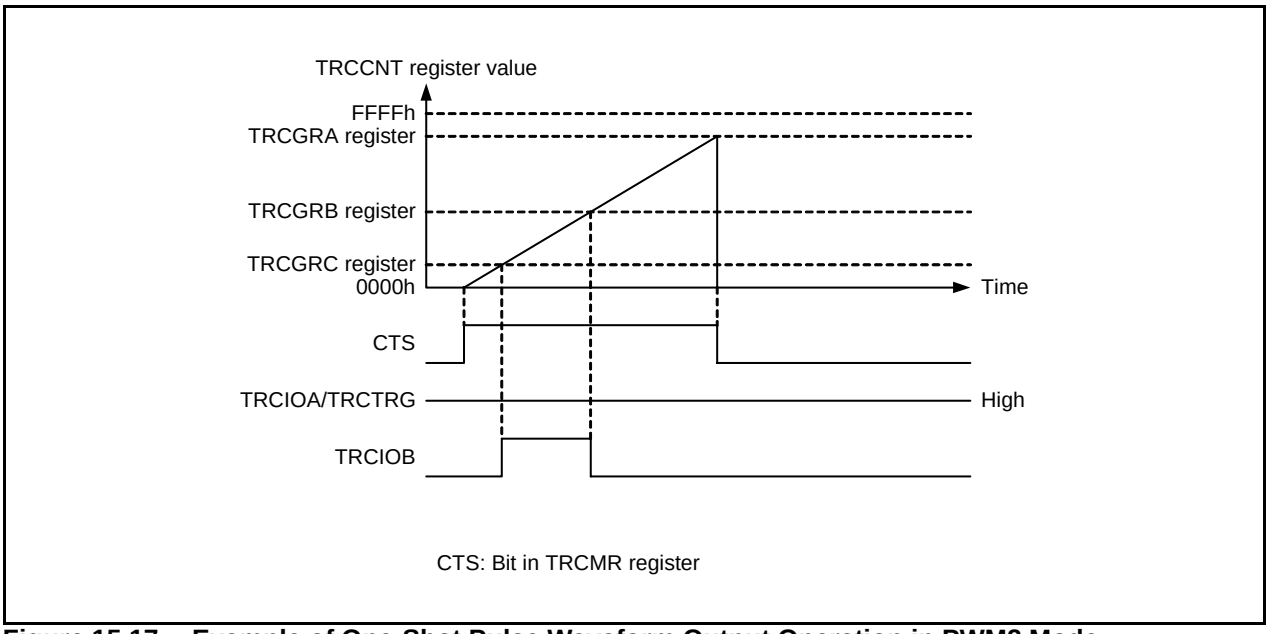


Figure 15.17 Example of One-Shot Pulse Waveform Output Operation in PWM2 Mode

19.6.5 Data Protect Function

Each block in the program ROM in the flash memory has a nonvolatile lock bit. The lock bit is enabled when the FMR13 bit in the FMR1 register is 0 (lock bit enabled). The lock bit can be used to disable (lock) programming/erasing each block. This prevents data from being written or erased inadvertently. The block status changes according to the lock bit as follows:

- When the lock bit data is 0: locked (the block cannot be programmed/erased)
- When the lock bit data is 1: not locked (the block can be programmed/erased)

The lock bit data is set to 0 (locked) when the lock bit program command is executed, and 1 (not locked) when the block is erased. There are no commands that can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and no blocks are locked. The lock bit data remains unchanged. When the FMR13 bit is set to 0 (lock bit enabled), the lock bit function is enabled. The lock bit data is retained.
When the block erase command is executed while the FMR13 bit is 1 (lock bit disabled), the target block is erased regardless of the lock bit status. The lock bit for the erase-target block is set to 1 after erase is completed. For details on individual commands, see **19.6.6 Software Commands**.
The FMR13 bit is set to 0 after auto-erase is completed. This bit is also set to 0 when one of the following conditions is met. To program/erase a block with a lock bit in a different state, set the FMR 13 bit to 1 (lock bit disabled) again and execute the program command or the block erase command.

- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and the program/erase command completes.
- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and program-suspend/erase-suspend is entered.
- When a command sequence error occurs.
- When the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- When the FMSTP bit in the FMR0 register is set to 1 (flash memory is stopped).
- When the CMDRST bit in the FMR0 register is set to 1 (erase/write sequence reset).

Figure 19.7 shows the Timing for FMR13 Bit Operation.

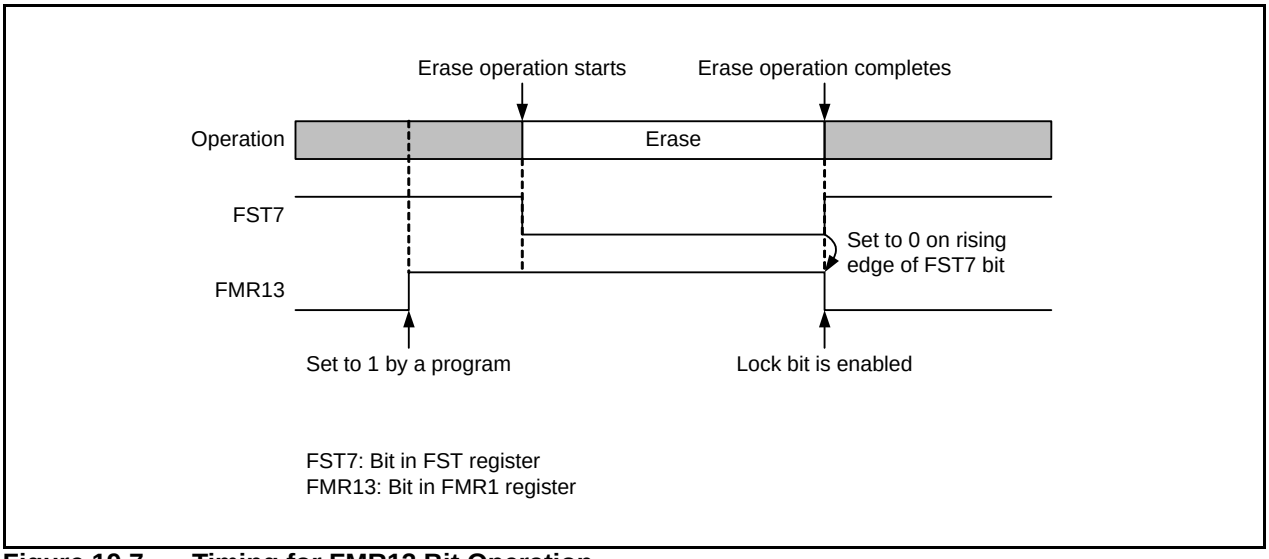


Figure 19.7 Timing for FMR13 Bit Operation

21.5.5 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) When Returning from Wait Mode or Stop Mode to Standard Mode

When a transition is made to wait mode or stop mode with the WCKSTP bit in the CKSTPR register set to 1 (system clock stopped in wait mode) while in use of the $\overline{\text{INTi}}$ input filter, the $\overline{\text{INTi}}$ interrupt cannot be used to return to standard operating mode.

When the $\overline{\text{INTi}}$ interrupt is used to return, set the WCKSTP bit to 1 and bits INTiF1 to INTiF0 in the INTF0 register to 00b (no filter) before a transition is made to wait mode or stop mode. When the $\overline{\text{INTi}}$ input filter is used again, select the sampling clock with bits INTiF0 to INTiF1 to enable the INTiEN bit in the INTEN register.

Figure 21.2 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used.

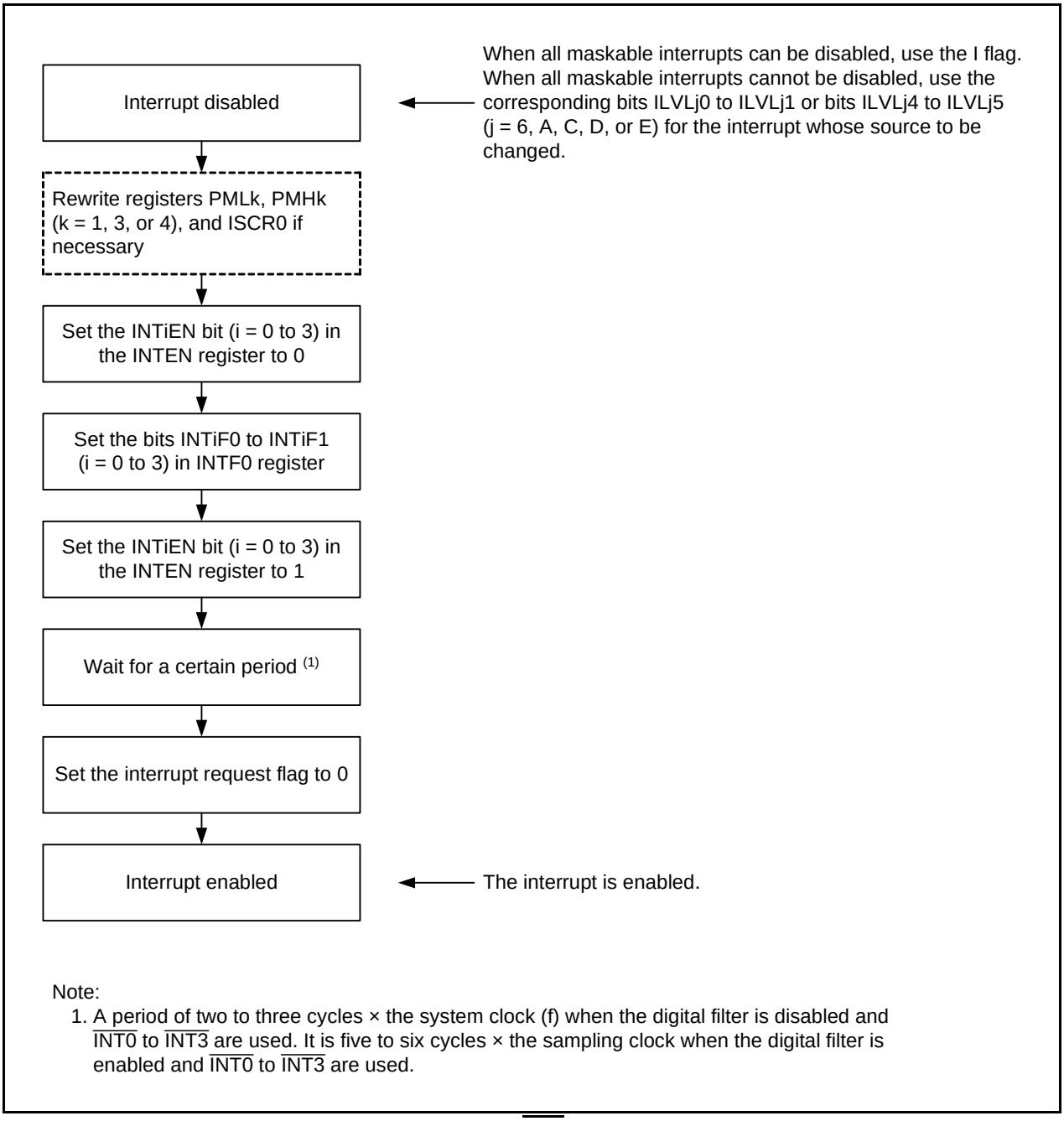


Figure 21.2 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used

21.9.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 15.1 Timer RC Specifications**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 15.19 Digital Filter Circuit Block Diagram**)

- The value of the TRCCNT register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

21.9.6 TRCMR Register in PWM2 Mode

When the CSTP bit in the TRCCR2 register is 1 (increment is stopped), do not set the TRCMR register when a compare match occurs between registers TRCCNT and TRCGRA.

21.9.7 MSTCR Register

After stopping the timer RC count, set the MSTTRC bit in the MSTCR register to 1 (standby).

21.9.8 Mode Switching

- When switching the modes during operation, set the CTS bit in the TRCMR register to 0 (count is stopped) before switching.
- After switching the modes, set each flag in the TRCSR register to 0 before operation is started.

21.9.9 Procedure for Setting Registers Associated with Timer RC

Set the registers associated with timer RC following the procedure below:
(1) Set timer RC operating mode (bits PWMB, PWMC, PWMD, and PWM2 in the TRCMR register).
(2) Set the registers other than that set in (1).
(3) Set the port output to be enabled (bits EA to ED in the TRCOER register).