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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b SAR; D/A 1x10b
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36078gfzv

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the SRST bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

Address	Register Name	Symbol	Page
00080h	UART0 Transmit/Receive Mode Register	U0MR	280
00081h	UART0 Bit Rate Register	U0BRG	281
00082h	UART0 Transmit Buffer Register	U0TBL	281
00083h		U0TBH	
00084h	UART0 Transmit/Receive Control Register 0	U0C0	282
00085h	UART0 Transmit/Receive Control Register 1	U0C1	283
00086h	UART0 Receive Buffer Register	U0RBL	284
00087h		U0RBH	
00088h	UART0 Interrupt Flag and Enable Register	U0IR	285
00089h			
0008Ah			
0008Bh			
0008Ch			
0008Dh			
0008Eh			
0008Fh			
00090h			
00091h			
00092h			
00093h			
00094h			
00095h			
00096h			
00097h			
00098h	A/D Register 0	AD0L	302
00099h		AD0H	
0009Ah	A/D Register 1	AD1L	302
0009Bh		AD1H	
0009Ch	A/D Mode Register	ADMOD	303
0009Dh	A/D Input Select Register	ADINSEL	304
0009Eh	A/D Control Register 0	ADCON0	305
0009Fh	A/D Interrupt Control Status Register	ADICSR	306
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h			
000A9h	Port P1 Direction Register	PD1	144
000AAh			
000ABh	Port P3 Direction Register	PD3	152
000ACh	Port P4 Direction Register	PD4	158
000ADh	Port PA Direction Register	PDA	164
000AEh			
000AFh	Port P1 Register	P1	144
000B0h			
000B1h	Port P3 Register	P3	152
000B2h	Port P4 Register	P4	158
000B3h	Port PA Register	PA	164
000B4h			
000B5h	Pull-Up Control Register 1	PUR1	145
000B6h			
000B7h	Pull-Up Control Register 3	PUR3	153
000B8h	Pull-Up Control Register 4	PUR4	159
000B9h	Port I/O Function Control Register	PINSR	142
000BAh			
000BBh	Drive Capacity Control Register 1	DRR1	145
000BCh			
000BDh	Drive Capacity Control Register 3	DRR3	153
000BEh			
000BFh			

Note:
1. The blank areas are reserved. No access is allowed.

Address	Register Name	Symbol	Page
000C0h			
000C1h	Open-Drain Control Register 1	POD1	146
000C2h			
000C3h	Open-Drain Control Register 3	POD3	154
000C4h	Open-Drain Control Register 4	POD4	159
000C5h	Port PA Mode Control Register	PAMCR	165
000C6h			
000C7h			
000C8h	Port 1 Function Mapping Register 0	PML1	146
000C9h	Port 1 Function Mapping Register 1	PMH1	147
000CAh			
000CBh			
000CCh	Port 3 Function Mapping Register 0	PML3	154
000CDh	Port 3 Function Mapping Register 1	PMH3	155
000CEh	Port 4 Function Mapping Register 0	PML4	160
000CFh	Port 4 Function Mapping Register 1	PMH4	160
000D0h			
000D1h	Port 1 Function Mapping Expansion Register	PMH1E	148
000D2h			
000D3h			
000D4h			
000D5h	Port 4 Function Mapping Expansion Register	PMH4E	161
000D6h			
000D7h			
000D8h	Timer RJ Counter Register	TRJ	180
000D9h			
000DAh	Timer RJ Control Register	TRJCR	181
000DBh	Timer RJ I/O Control Register	TRJIOC	182
000DCh	Timer RJ Mode Register	TRJMR	184
000DDh	Timer RJ Event Select Register	TRJISR	184
000DEh	Timer RJ Interrupt Control Register	TRJIR	185
000DFh			
000E0h	Timer RB Control Register	TRBCR	199
000E1h	Timer RB One-Shot Control Register	TRBOCR	200
000E2h	Timer RB I/O Control Register	TRBIOC	201
000E3h	Timer RB Mode Register	TRBMR	202
000E4h	Timer RB Prescaler Register Timer RB Primary/Secondary Register (Lower 8 Bits)	TRBPRE	203
000E5h	Timer RB Primary Register Timer RB Primary Register (Higher 8 Bits)	TRBPR	204
000E6h	Timer RB Secondary Register Timer RB Secondary Register (Higher 8 Bits)	TRBSC	205
000E7h	Timer RB Interrupt Control Register	TRBIR	206
000E8h	Timer RC Counter	TRCCNT	232
000E9h			
000EAh	Timer RC General Register A	TRCGRA	233
000EBh			
000ECh	Timer RC General Register B	TRCGRB	233
000EDh			
000EEh	Timer RC General Register C	TRCGRC	233
000EFh			
000F0h	Timer RC General Register D	TRCGRD	233
000F1h			
000F2h	Timer RC Mode Register	TRCMR	235
000F3h	Timer RC Control Register 1	TRCCR1	236
000F4h	Timer RC Interrupt Enable Register	TRCIER	237
000F5h	Timer RC Status Register	TRCSR	238
000F6h	Timer RC I/O Control Register 0	TRCIOR0	239
000F7h	Timer RC I/O Control Register 1	TRCIOR1	240
000F8h	Timer RC Control Register 2	TRCCR2	241
000F9h	Timer RC Digital Filter Function Select Register	TRCDF	242
000FAh	Timer RC Output Enable Register	TRCOER	243
000FBh	Timer RC A/D Conversion Trigger Control Register	TRCADCR	244
000FCh	Timer RC Waveform Output Manipulation Register	TRCOPR	245
000FDh			
000FEh			
000FFh			

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.8 list the SFR Information. Table 3.9 lists the ID Code Area and Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Register Name	Symbol	After Reset
00000h			
00001h			
00002h			
00003h			
00004h			
00005h			
00006h			
00007h			
00008h			
00009h			
0000Ah			
0000Bh			
0000Ch			
0000Dh			
0000Eh			
0000Fh			
00010h	Processor Mode Register 0	PM0	00h
00011h			
00012h	Module Standby Control Register	MSTCR	00h (2) 01110111b (3)
00013h	Protect Register	PRCR	00h
00014h			
00015h			
00016h	Hardware Reset Protect Register	HRPR	00h
00017h			
00018h			
00019h			
0001Ah			
0001Bh			
0001Ch			
0001Dh			
0001Eh			
0001Fh			
00020h	External Clock Control Register	EXCKCR	00h
00021h	High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h
00022h	System Clock f Control Register	SCKCR	00h
00023h	System Clock f Select Register	PHISEL	00h
00024h	Clock Stop Control Register	CKSTPR	00h
00025h	Clock Control Register When Returning from Modes	CKRSCR	00h
00026h	Oscillation Stop Detection Register	BAKCR	00h
00027h			
00028h			
00029h			
0002Ah			
0002Bh			
0002Ch			
0002Dh			
0002Eh			
0002Fh			
00030h	Watchdog Timer Function Register	RISR	10000000b (4) 00h (5)
00031h	Watchdog Timer Reset Register	WDTR	XXh
00032h	Watchdog Timer Start Register	WDTS	XXh
00033h	Watchdog Timer Control Register	WDTC	01XXXXXXb
00034h	Count Source Protection Mode Register	CSPR	10000000b (4) 00h (5)
00035h	Periodic Timer Interrupt Control Register	WDTIR	00h
00036h			
00037h			
00038h	External Input Enable Register	INTEN	00h
00039h			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The MSTINI bit in the OFS2 register is 0.
3. The MSTINI bit in the OFS2 register is 1.
4. The CSPROINI bit in the OFS register is 0.
5. The CSPROINI bit in the OFS register is 1.

5.2.5 Reset Source Determination Register (RSTFR)

Address 0005Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDR	SWR	HWR	CWR
After Reset	0	0	0	0	X (1)	X (1)	X (1)	X (1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. The value after a reset differs depending on the reset source.

CWR Bit (Cold start-up/warm start-up determine flag)

This flag indicates whether a cold start-up or warm start-up has occurred. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
The CWR bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.

[Condition for setting to 0]
• When a reset occurs after power-on or voltage detection 0.
[Condition for setting to 1]
• When 1 is written to this bit by a program.

HWR Bit (Hardware reset detect flag)

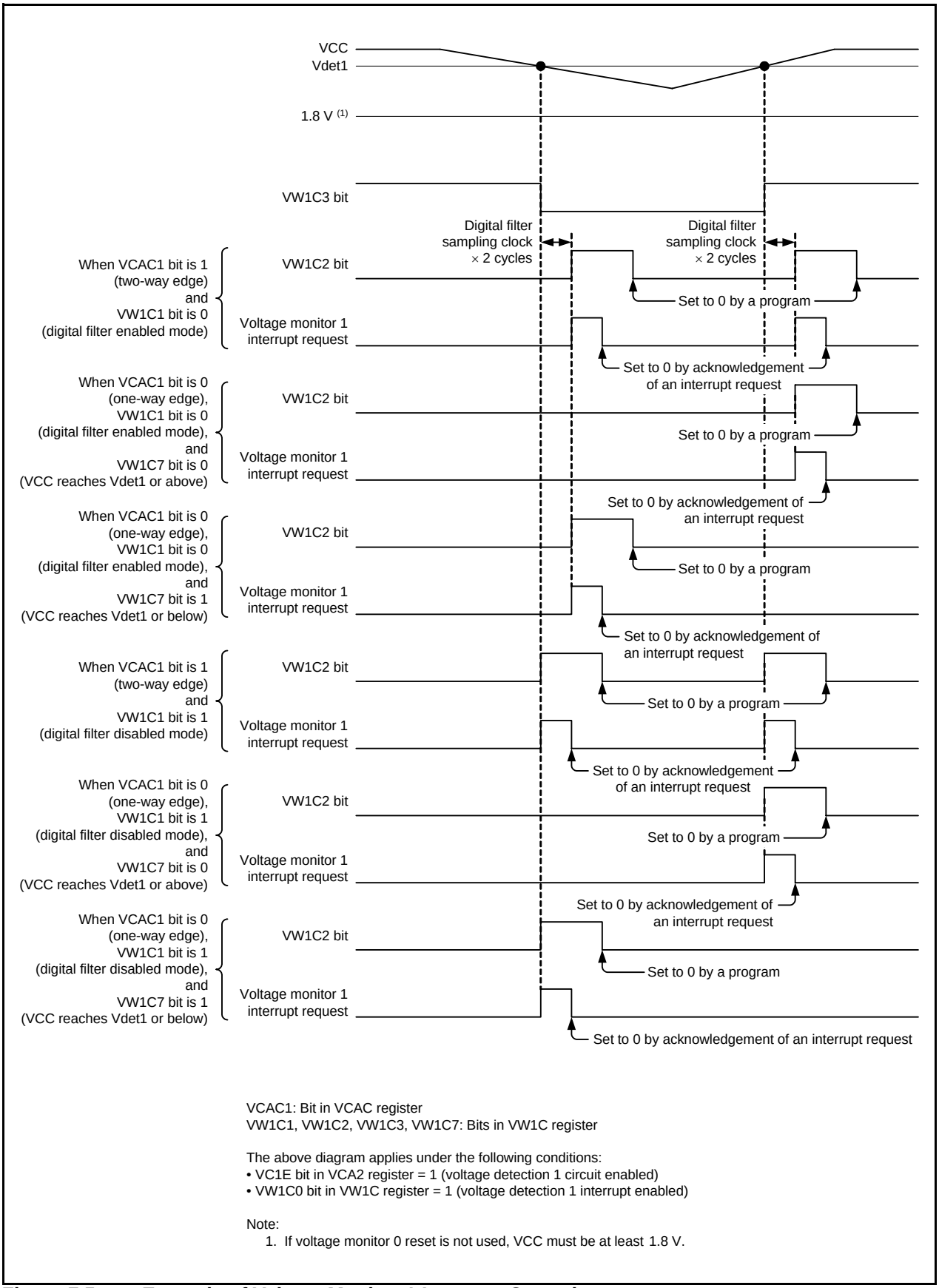
This flag indicates that a hardware reset has occurred.

[Condition for setting to 0]
• When a software reset, watchdog timer reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a hardware reset occurs.

SWR Bit (Software reset detect flag)

This flag indicates that a reset has been generated by software.

[Condition for setting to 0]
• When a watchdog timer reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a software reset occurs.



VCAC1: Bit in VCAC register
VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register

The above diagram applies under the following conditions:
- VC1E bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage detection 1 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, VCC must be at least 1.8 V.

Figure 7.5 Example of Voltage Monitor 1 Interrupt Operation

8.3.2 When Count Source Protection Mode is Disabled

When count source protection mode is disabled, the count source for the watchdog timer is the CPU clock or low-speed on-chip oscillator clock.
Table 8.3 lists the Watchdog Timer Specifications When Count Source Protection Mode is Disabled.

Table 8.3 Watchdog Timer Specifications When Count Source Protection Mode is Disabled

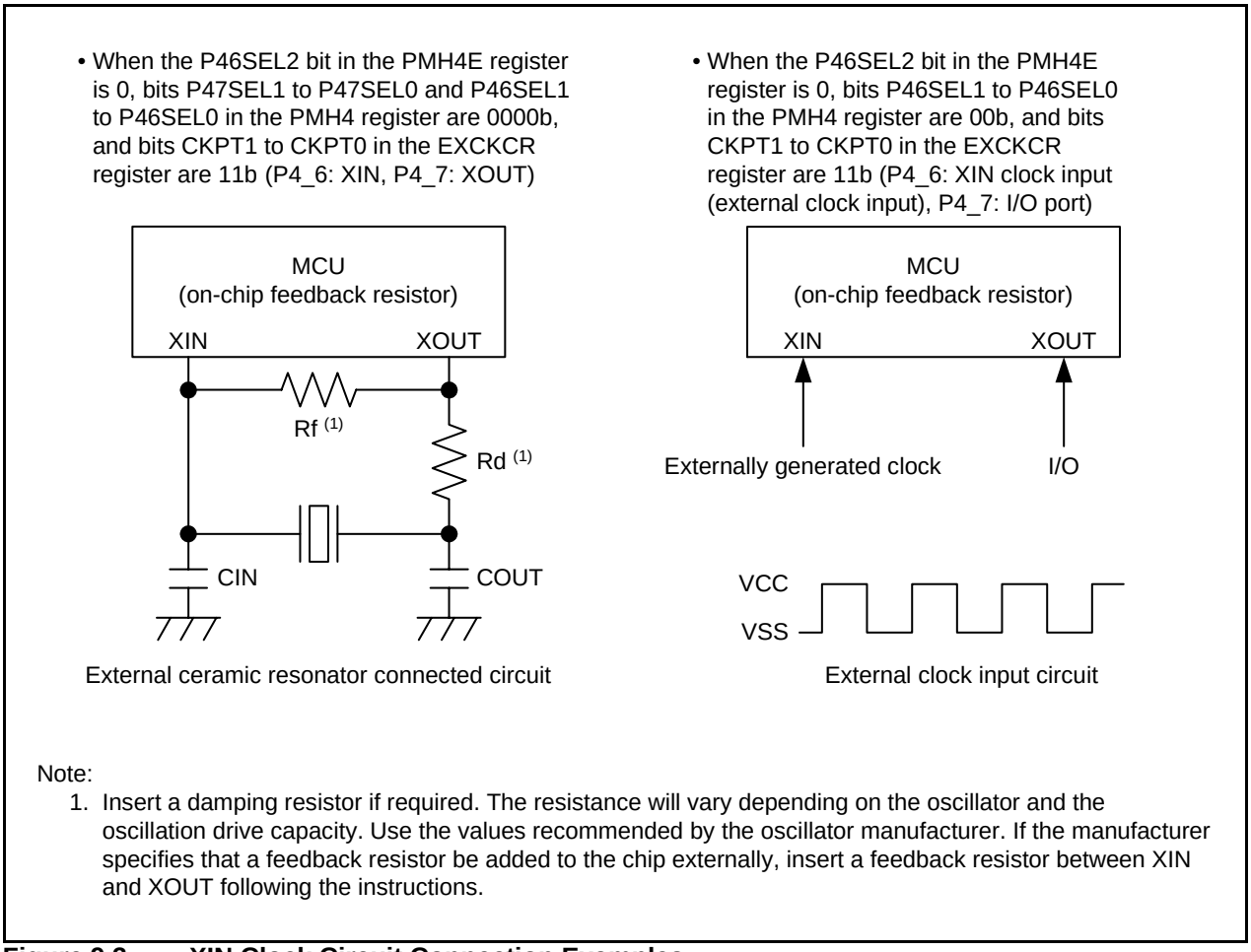
Item	Specification
Count source	CPU clock or low-speed on-chip oscillator clock (1/16)
Count operation	Decrement
Period	$\frac{\text{Prescaler division ratio (n)} \times \text{Count value in the watchdog timer (m)}}{\text{Count source}}$ (1) n: 2, 16, or 128 (selected by bits WDTC6 to WDTC7 in the WDTC register) However, when bits WDTC7 to WDTC6 are 11b (count source is low-speed on-chip oscillator), n is 16. m: Value set by bits WDTUFS0 to WDTUFS1 in the OFS2 register Ex.: When the prescaler divides a CPU clock of 20 MHz by 16, and bits WDTUFS1 to WDTUFS0 are 11b (3FFFh), the period is approx. 13.1 ms.
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit in the OFS register (address 0FFFFh). • When the WDTON bit is 1 (watchdog timer is stopped after reset) The watchdog timer and the prescaler are stopped after a reset, and only start counting when the WDTS register is written. • When the WDTON bit is 0 (watchdog timer is automatically started after reset) The watchdog timer and the prescaler automatically start counting after a reset.
Count stop conditions	When wait mode or stop mode is entered while the count source is the CPU clock
Operation at underflow	• When the RIS bit in the RISR register is 0 Watchdog timer interrupt • When the RIS bit in the RISR register is 1 Watchdog timer reset (See **6.3.5 Watchdog Timer Reset**.)

Note:
1. The watchdog timer is initialized by writing 00h and then writing FFh to the WDTR register. The prescaler is initialized after a reset. This results in discrepancies in the watchdog timer period due to the prescaler.

9.3 Clock Oscillation Circuit

9.3.1 XIN Clock Oscillation Circuit

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU clock and the peripheral function clock. The XIN clock oscillation circuit is configured by connecting an oscillator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode to reduce power consumption. To input an externally generated clock to the XIN pin, set the P46SEL2 bit in the PMH4E register to 0, bits P46SEL1 to P46SEL0 in the PMH4 register to 00b (I/O port or XIN input), and bits CKPT1 to CKPT0 in the EXCKCR register to 01b (XIN clock input).
Figure 9.3 shows the XIN Clock Circuit Connection Examples.
The XIN clock is stopped during and after a reset.
The XIN clock starts oscillating when the P46SEL2 bit in the PMH4E register is set to 0, bits P47SEL1 to P47SEL0 and P46SEL1 to P46SEL0 in the PMH4 register are set to 0000b, and bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b (P4_6: XIN, P4_7: XOUT). After the XIN clock oscillation stabilizes, when the HSCKSEL bit in the SCKCR register is set to 0 (XIN clock) and the SCKSEL bit in the CKSTPR register is set to 1 (fHSCK), the XIN clock is selected to be used as the clock source for the CPU clock and the peripheral function clock.
When the high-speed on-chip oscillator or the low-speed on-chip oscillator is used as the system base clock, the XIN clock oscillation is stopped by setting bits CKPT1 to CKPT0 in the EXCKCR register to 00b. This reduces power consumption.
The XIN clock is stopped in stop mode. When inputting an externally generated clock to the XIN clock, do not use stop mode. See **10. Power Control** for details.



Note:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity. Use the values recommended by the oscillator manufacturer. If the manufacturer specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.

Figure 9.3 XIN Clock Circuit Connection Examples

11.2.9 External Interrupt Flag Register (IRR3)

Address 00053h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	IRKI	—	IRI3	IRI2	IRI1	IRI0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IRI0	$\overline{\text{INT0}}$ interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b1	IRI1	$\overline{\text{INT1}}$ interrupt request flag		R/W
b2	IRI2	$\overline{\text{INT2}}$ interrupt request flag		R/W
b3	IRI3	$\overline{\text{INT3}}$ interrupt request flag		R/W
b4	—	Reserved	Set to 0.	R/W
b5	IRKI	Key input interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

IRI0 Bit ($\overline{\text{INT0}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI0 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT0}}$) is acknowledged.

IRI1 Bit ($\overline{\text{INT1}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI1 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT1}}$) is acknowledged.

IRI2 Bit ($\overline{\text{INT2}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI2 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT2}}$) is acknowledged.

IRI3 Bit ($\overline{\text{INT3}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI3 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT3}}$) is acknowledged.

IRKI Bit (Key input interrupt request flag)

Writing 0 after reading the value 1 sets the IRKI bit to 0. This bit is also automatically set to 0 when the corresponding interrupt (key input) is acknowledged.

The interrupt priority level register must be rewritten only while no interrupt requests corresponding to that register are generated. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers**.

12.5.1 Port P4 Direction Register (PD4)

Address 000ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD4_7	PD4_6	PD4_5	—	—	PD4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	PD4_2	Port P4_2 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	PD4_5	Port P4_5 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b6	PD4_6	Port P4_6 direction bit		R/W
b7	PD4_7	Port P4_7 direction bit		R/W

The PD4 register is used to select whether I/O ports are used as input or output.
Each bit in the PD4 register corresponds to individual ports.

12.5.2 Port P4 Register (P4)

Address 000B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P4_7	P4_6	P4_5	—	—	P4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	P4_2	Port P4_2 bit	0: Low level 1: High level	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	P4_5	Port P4_5 bit	0: Low level 1: High level	R/W
b6	P4_6	Port P4_6 bit		R/W
b7	P4_7	Port P4_7 bit		R/W

The P4 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P4 register. The P4 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pin. Each bit in the P4 register corresponds to individual ports.

12.6 Port A

Figure 12.4 shows the Port A Pin Configuration.

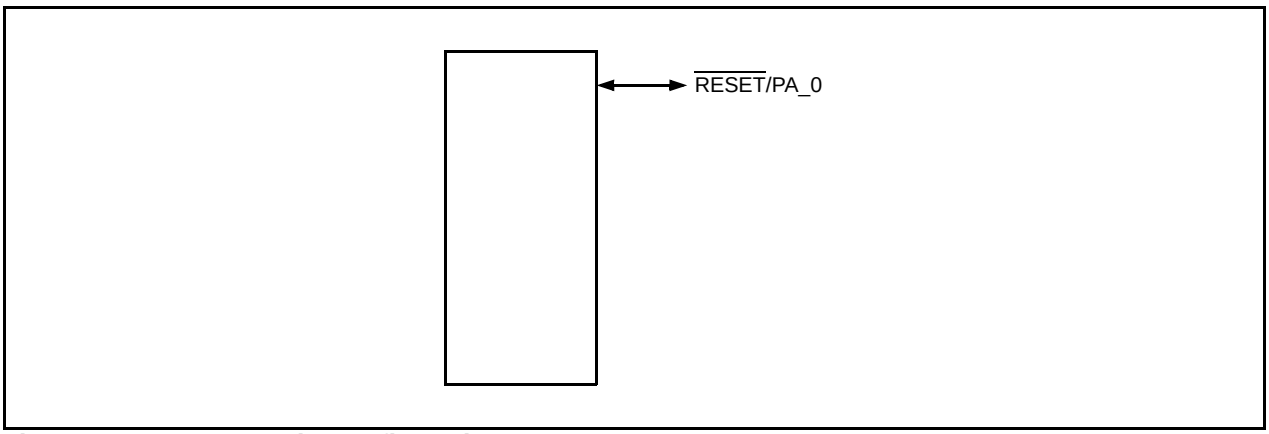


Figure 12.4 Port A Pin Configuration

(8) When the TEDGSEL bit in the TRJIOC register is set to 0 (count on rising edge) and the external signal (TRJIO) is counted in event counter mode, the signal may not be counted correctly depending on the state of the TSTART bit in the TRJCR register (see Figure 13.8).
If the TRJIO pin is set to low before the TSTART bit is set to 1 (count is started) and a valid event is input after the TSTART bit is set to 1, the signal is not counted on the first rising edge of the TRJIO input.
Thus, the number of counted events is obtained as follows:
Number of counted events = {(initial value in the counter – value in the counter on completion of the valid event + 1) + 1}
To avoid this, set the TRJIO pin to low after setting the TSTART bit to 1 (count is started) (see Figure 13.9).

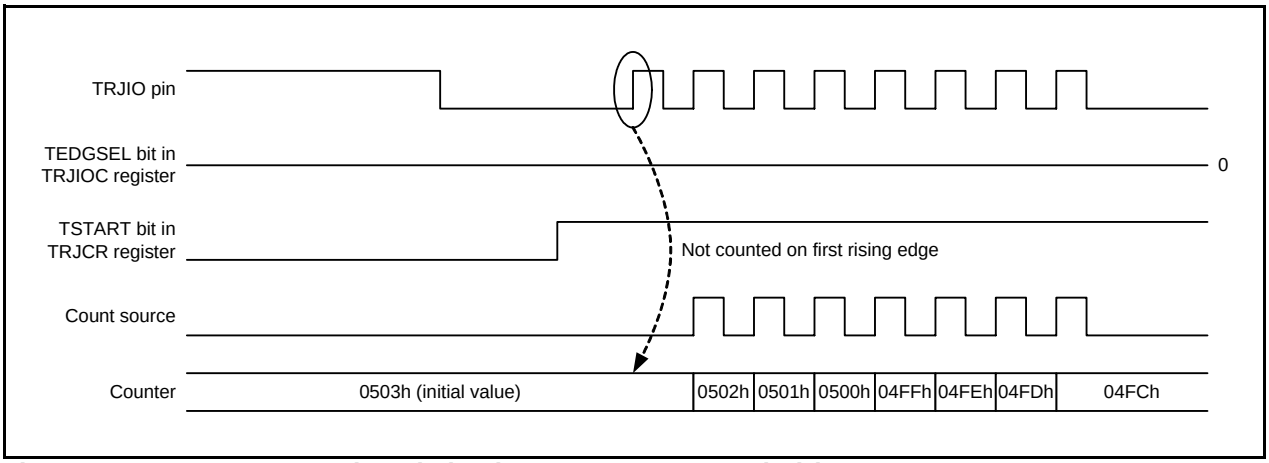


Figure 13.8 TSTART Setting Timing in Event Counter Mode (1)

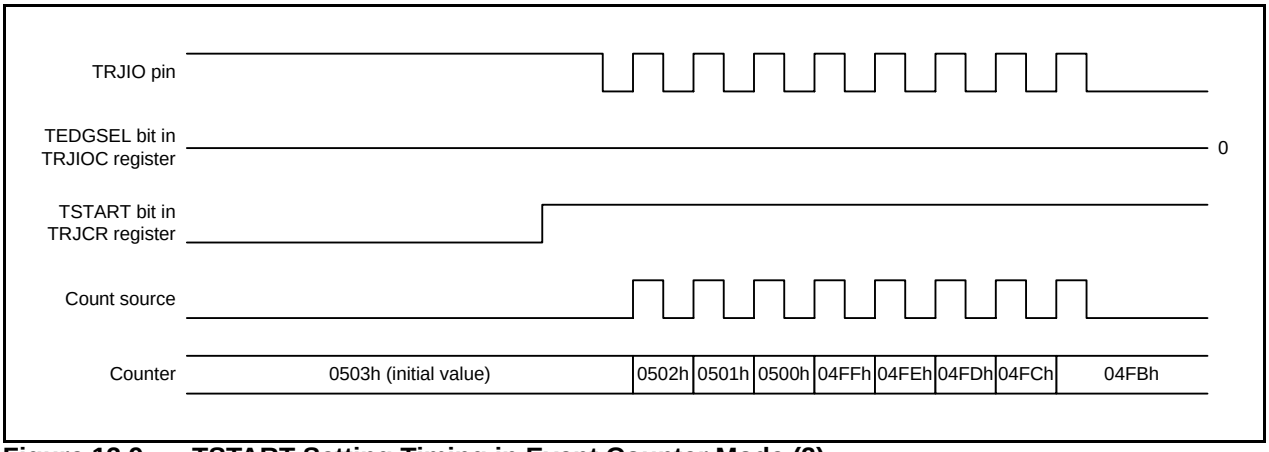


Figure 13.9 TSTART Setting Timing in Event Counter Mode (2)

14.4.3 Programmable One-Shot Generation Mode

In this mode, a one-shot pulse is output from the TRBO pin by a program or the $\overline{\text{INT0}}$ pin input. When a trigger is generated from that point, the timer operates only once to count a given length of the time equal to the setting value of the TRBPR register.
In the 8-bit timer with 8-bit prescaler, the count value is set in the TRBPR register.
In the 16-bit timer, the count value of the higher 8 bits is set in the TRBPR register and that of the lower 8 bits is set in the TRBPRE register.
In programmable one-shot generation mode, the TRBSC register is not used.
When 1 (one-shot count is started) is written to the TOSST bit in the TRBOCR register while the TCSTF bit in the TRBCR register is 1 (count is enabled), the count is started after the count source is sampled three times. If an enabled trigger is input to the $\overline{\text{INT0}}$ pin while the TCSTF bit is 1, the count is started after the count source is sampled three times. When the count value in the timer RB secondary overflows and then it is reloaded, the count is stopped. The count is also stopped with any of the following settings:

- When 1 (one-shot count is stopped) is written to the TOSSP bit in the TRBOCR register, the count is stopped after the count source is sampled three times.
- When 0 (count is stopped) is written to the TSTART bit in the TRBCR register, the count is stopped after the count source is sampled three times.
- When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped.

The actual count state must be monitored with the TCSTF bit in the TRBCR register.
An interrupt request is generated when timer RB2 underflows.
When registers TRBPRE and TRBPR are read, each count value can be read. When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to the reload register and then transferred to the counter at the next reload operation.
For the setting of trigger by the $\overline{\text{INT0}}$ input, see **14.7 INT0 Input Trigger Selection**.
Figure 14.5 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable One-Shot Generation Mode. Figure 14.6 shows an Example of 16-Bit Timer Operation in Programmable One-Shot Generation Mode.

By setting the general register as an output compare register, low-level, high-level, or toggle output is performed by compare matches A to D from pins TRCIOA, TRCIOB, TRCIOC, TRCIOD.
Figure 15.4 shows an Example of Low-Level and High-Level Output Operation. The TRCCNT register is used for the free-running count operation, a low level is output at compare match B, and a high level is output at compare match A. When the set level and the pin level are the same, the pin level remains unchanged.

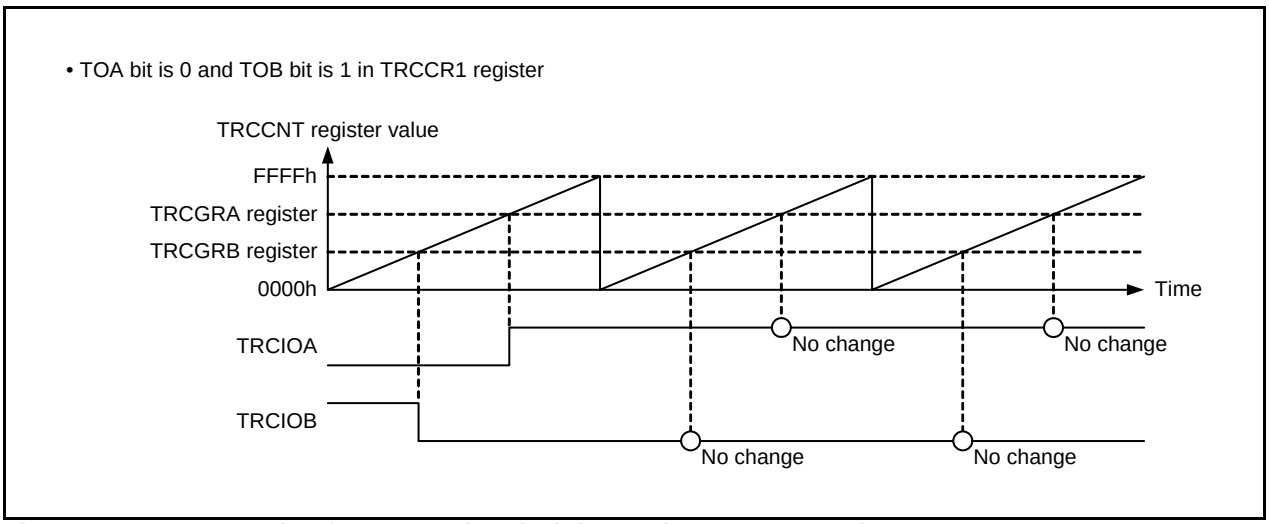


Figure 15.4 Example of Low-Level and High-Level Output Operation

Figure 15.5 shows an Example of Toggle Output Operation during Free-Running Count. The TRCCNT register is used for the free-running count operation, and toggle output is performed at compare matches A and B.

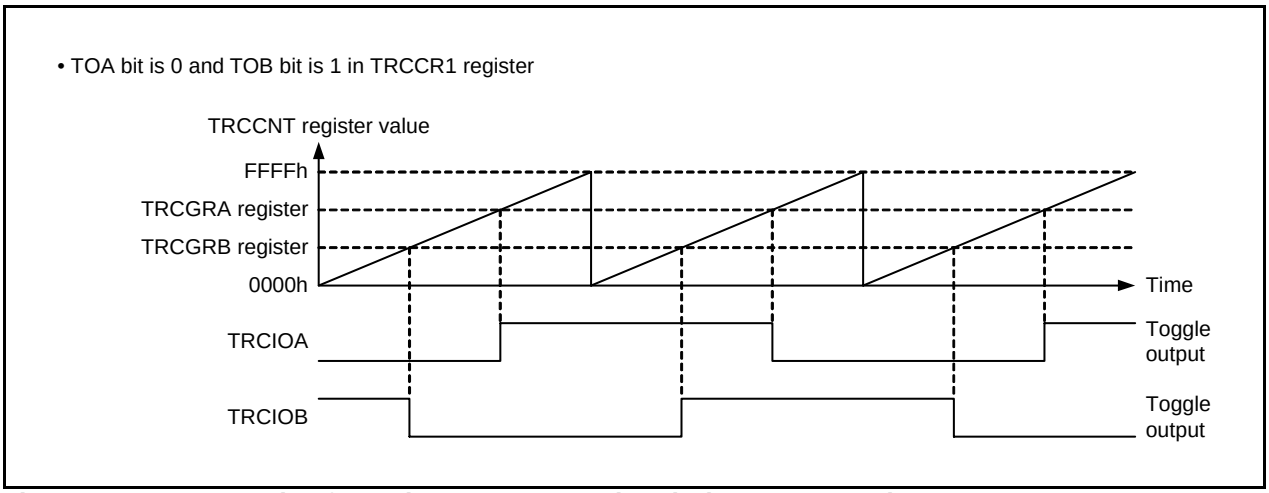


Figure 15.5 Example of Toggle Output Operation during Free-Running Count

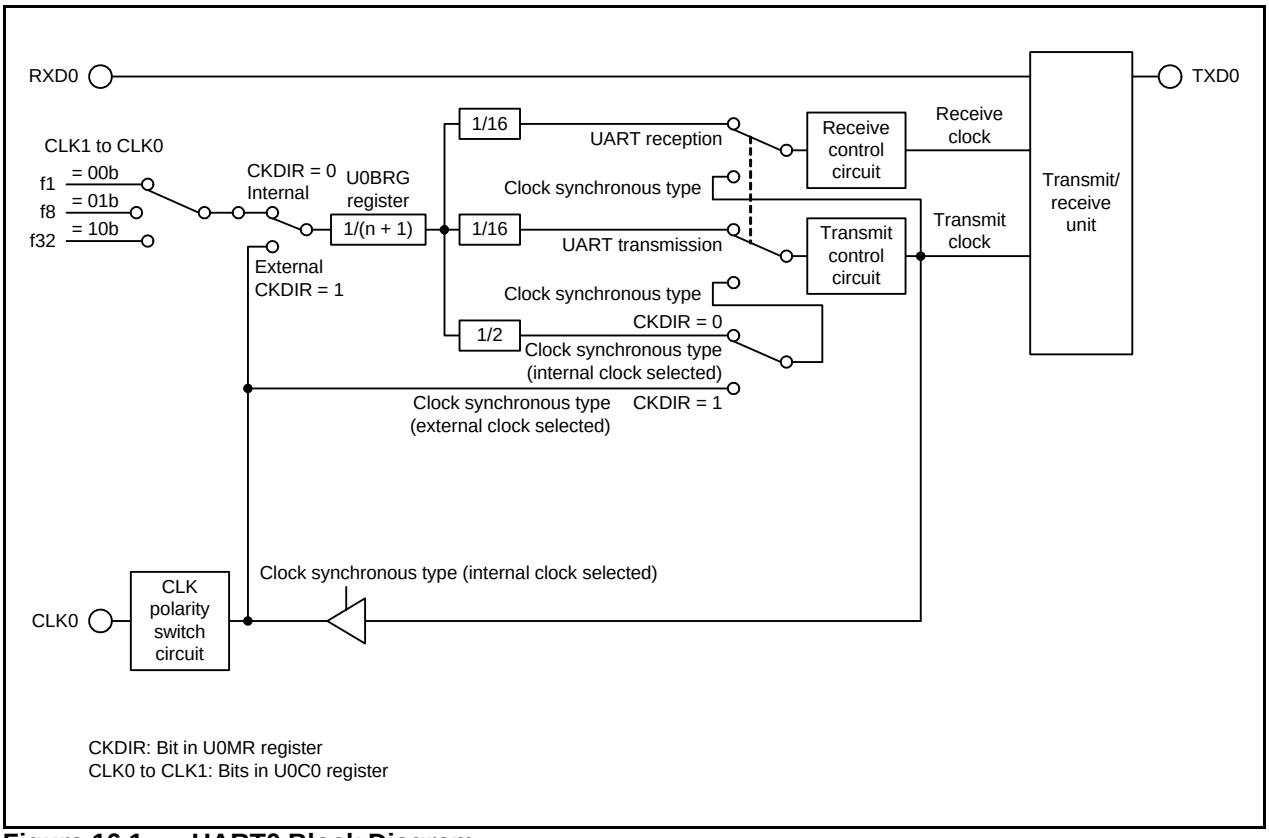


Figure 16.1 UART0 Block Diagram

17.3.5 Repeat Sweep Mode

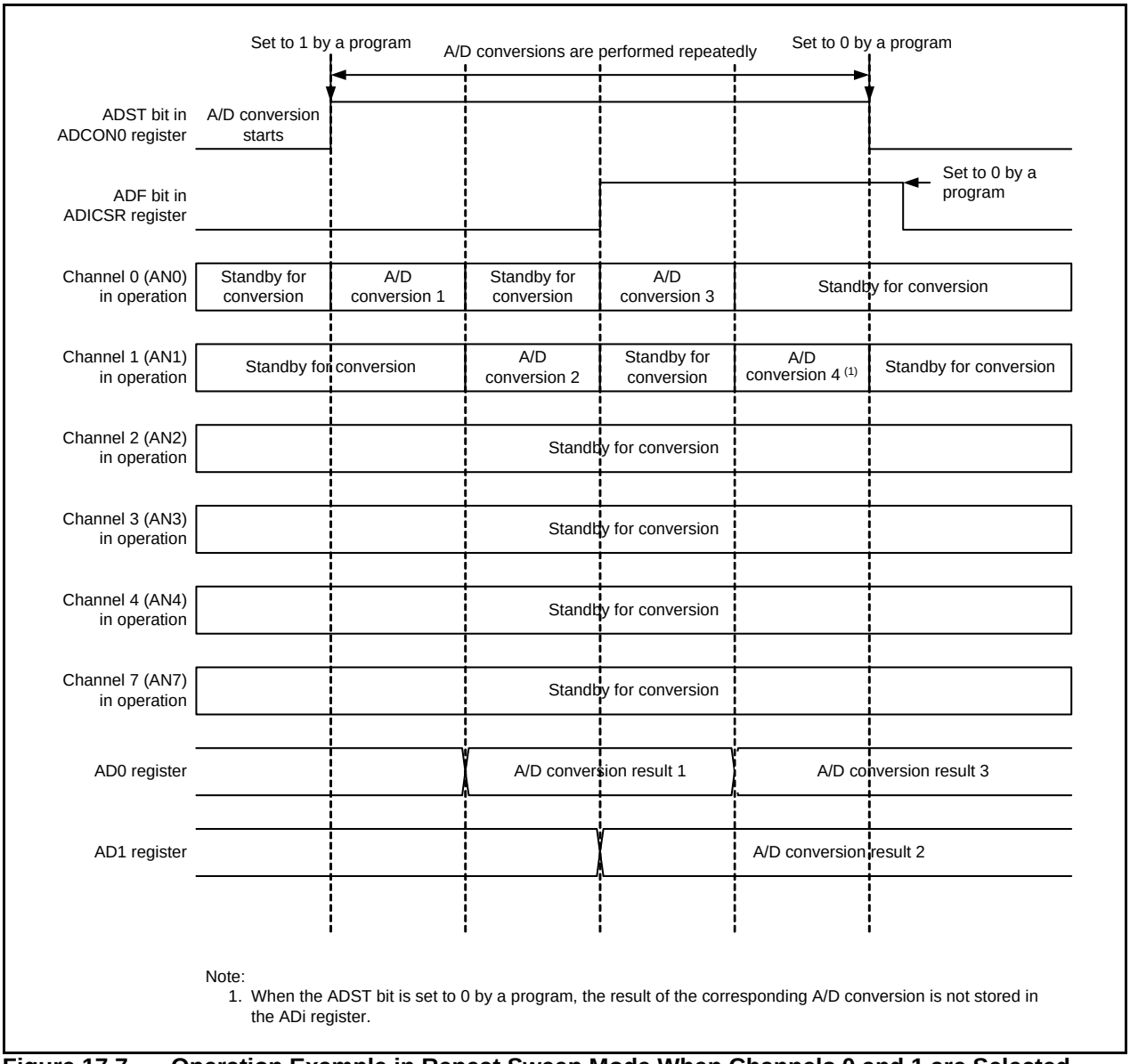
Figure 17.7 shows an Operation Example in Repeat Sweep Mode When Channels 0 and 1 are Selected.
In repeat sweep mode, A/D conversions of the analog inputs are performed for the specified two channels repeatedly as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started from AN0 when channel group 0 is selected, and AN2 when channel group 1 is selected. When channel group 2 is selected, A/D conversion is started from AN4.

(2) When A/D conversion has completed on each channel, the result is transferred to the corresponding ADi register (i = 0 or 1).

(3) When A/D conversion has completed on all the selected channels, the ADF bit in the ADICSR register is set to 1 (interrupt requested).
Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).

(4) While the ADST bit is 1 (A/D conversion starts), steps between (2) and (3) are repeated. When the ADST bit is set to 0 (A/D conversion stops), A/D conversion is stopped and the A/D converter enters the standby state. Then, when the ADST bit is set to 1, A/D conversion is restarted from AN0 when channel group 0 is selected, and AN2 when channel group 1 is selected. When channel group 2 is selected, A/D conversion is started from AN4.



Note:
1. When the ADST bit is set to 0 by a program, the result of the corresponding A/D conversion is not stored in the ADi register.

Figure 17.7 Operation Example in Repeat Sweep Mode When Channels 0 and 1 are Selected

19.6.3 Suspend Operation

The erase-suspend function temporarily halts the auto-erase during the operation.
The program suspend function temporarily halts the auto-programming during the operation.
When auto-erase or auto-programming is suspended, the following operation can be executed (see **Table 19.7 Executable Operation during Suspend**).

- When auto-erase of any block in the user ROM is suspended, auto-programming and reading of another block in the user ROM can be executed.
- When auto-programming of any block in the user ROM is suspended, reading of another block in the user ROM can be executed.

Table 19.7 Executable Operation during Suspend

		Operation during Suspend							
		Block where erase or program operation is executed before entering suspend				Block where erase or program operation is not yet executed before entering suspend			
		Erase	Program	Read lock bit status	Read	Erase	Program	Read lock bit status	Read
Command in execution	Erase	No	No	No	No	No	Yes	Yes	Yes
	Program	No	No	No	No	No	No	Yes	Yes

Notes:
1. “Yes” indicates operation is possible by using the suspend function and “No” indicates operation is disabled.
2. The block erase command can be executed for erasure. The program and lock bit program commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The block blank check operation is disabled during suspend.
3. The MCU enters read array mode immediately after entering suspend.

Figure 19.3 shows the Timing for Erase-Suspend Operation. Figure 19.4 shows the Timing for Program-Suspend Operation.

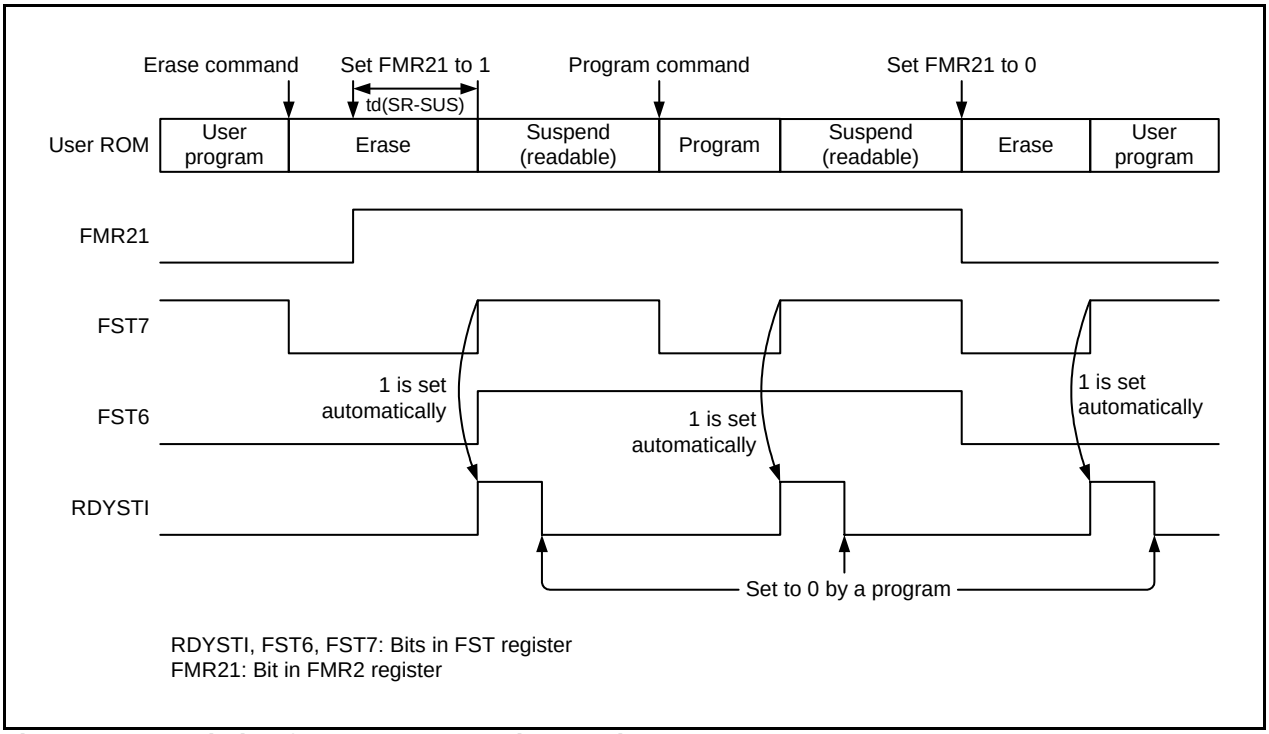
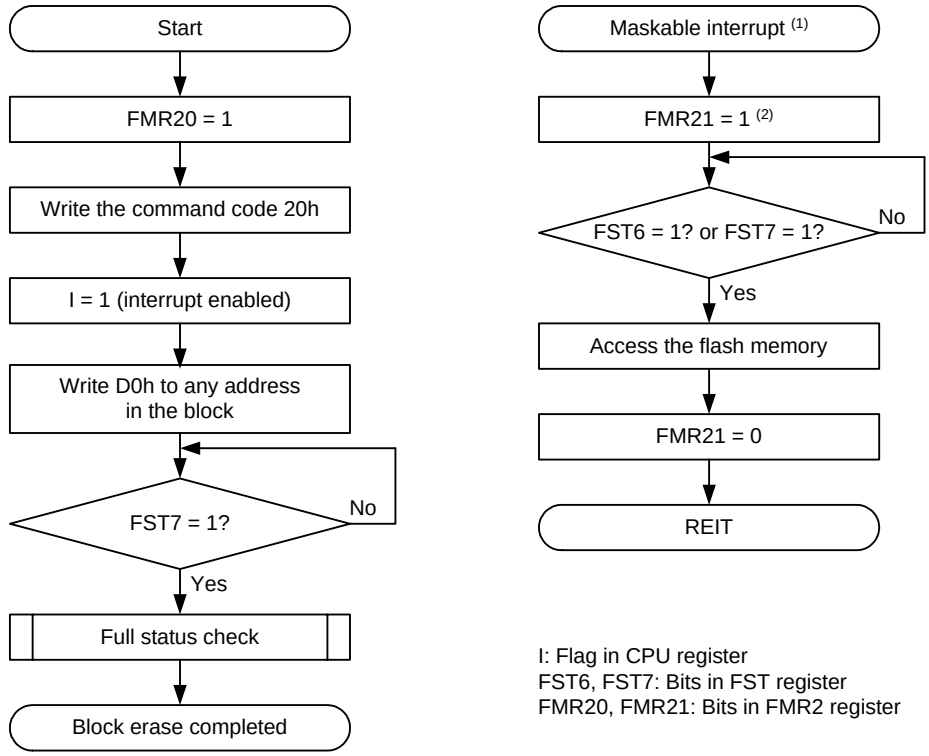


Figure 19.3 Timing for Erase-Suspend Operation



Notes:
1. The interrupt vector table and interrupt routine to be used must be allocated to an area other than the erase-target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.

Figure 19.13 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

20. Electrical Characteristics

Table 20.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Power supply voltage			-0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation circuit used) (1)	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) (1)	-0.3 to Vcc + 0.3	V
		Other pins		-0.3 to Vcc + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation circuit used) (1)	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) (1)	-0.3 to Vcc + 0.3	V
		Other pins		-0.3 to Vcc + 0.3	V
P_d	Power consumption		-40 °C ≤ Topr ≤ 85 °C	500	mW
T_{opr}	Operating ambient temperature			-20 to 85 (N version)/ -40 to 85 (D version)	°C
T_{stg}	Storage temperature			-60 to 150	°C

Note:
1. When the oscillation circuit is used: bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b
   When the oscillation circuit is not used: bits CKPT1 to CKPT0 in the EXCKCR register are set to any value other than 11b

Timing Requirements (Vcc = 3 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 20.21 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

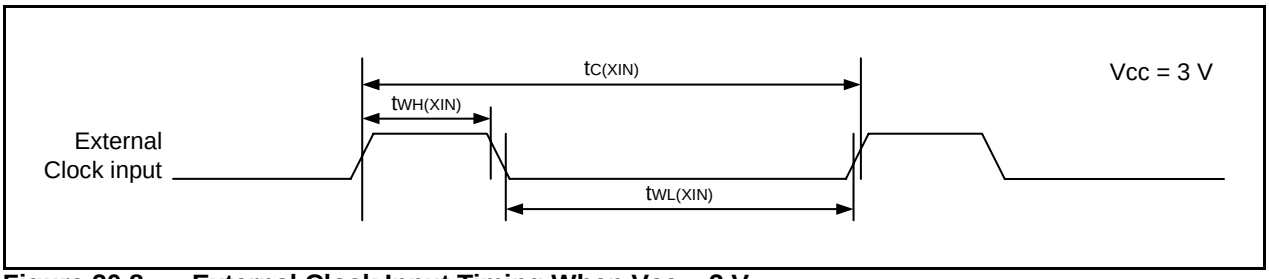


Figure 20.8 External Clock Input Timing When Vcc = 3 V

Table 20.22 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	300	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	120	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	120	—	ns

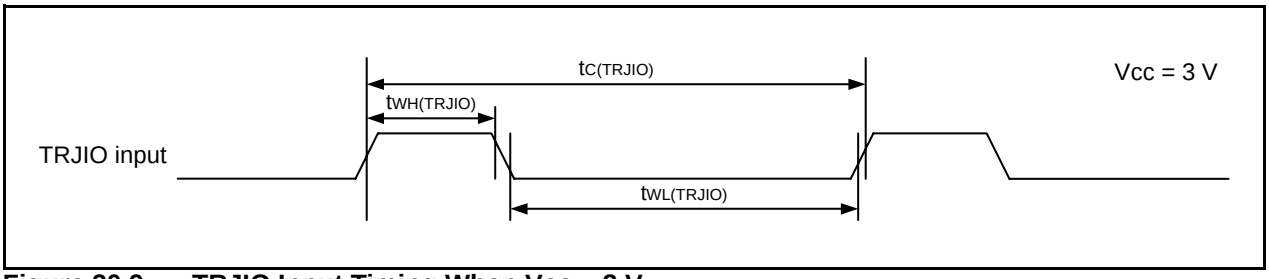


Figure 20.9 TRJIO Input Timing When Vcc = 3 V

Table 20.26 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition							Standard			Unit
			Oscillation Circuit	On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other				
			XIN (2)	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	125 kHz	No division	—		—	1.0	—	mA
			5 MHz	Off	125 kHz	Division by 8	—		—	0.6	—	mA
		High-speed on-chip oscillator mode	Off	5 MHz (4)	125 kHz	No division			—	1.6	6.5	mA
			Off	5 MHz (4)	125 kHz	Division by 8			—	1.1	—	mA
			Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	200	µA
		Wait mode	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	90	µA
			Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.0	80	µA
		Stop mode	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	µA
			Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.5	—	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 2.2 V
4. Set the system clock to 5 MHz or 4 MHz with the PHISEL register.