Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36079gfzv

Table 1.6 Pin Name Information by Pin Number

Pin Number		Control Pin	Port	I/O Pins for Peripheral Functions			
R8C/M11A Group	R8C/M12A Group			Interrupt	Timer	Serial Interface	A/D Converter, Comparator B
	1		P4_2	$\overline{KI3}$	TRBO	TXD0	
1	2		P3_7		TRJO/TRCIOD		$\overline{ADTRG}$
2	3	$\overline{RESET}$	PA_0				
3	4	XOUT	P4_7	$\overline{INT2}$			
4	5	VSS/AVSS					
5	6	XIN	P4_6	$\overline{INT1}$	TRJIO	RXD0/TXD0	VCOUT1
6	7	VCC/AVCC					
7	8	MODE					
	9		P3_5	$\overline{KI2}$	TRCIOD		VCOUT3
	10		P3_4	$\overline{INT2}$	TRCIOC		IVREF3
	11		P3_3	$\overline{INT3}$	TRCCLK		IVCMP3
	12		P4_5	$\overline{INT0}$			$\overline{ADTRG}$
8	13		P1_7	$\overline{INT1}$	TRJIO/TRCCLK		AN7/IVCMP1
9	14		P1_6		TRJO/TRCIOB	CLK0	IVREF1
10	15		P1_5	$\overline{INT1}$	TRJIO	RXD0	VCOUT1
11	16		P1_4	$\overline{INT0}$	TRCIOB	RXD0/TXD0	AN4
12	17		P1_3	$\overline{KI3}$	TRBO/TRCIOC		AN3
13	18		P1_2	$\overline{KI2}$	TRCIOB		AN2
14	19		P1_1	$\overline{KI1}$	TRCIOA/TRCTRG		AN1
	20		P1_0	$\overline{KI0}$	TRCIOD		AN0

7.2.4 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0005Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	VW0F1	VW0F0	—	—	VW0C1	VW0C0
After Reset	1	1	0	0	X	0	1	1
	The above applies when the LVDAS bit in the OFS register is 0.							
After Reset	1	1	0	0	X	0	1	0
	The above applies when the LVDAS bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Voltage monitor 0 reset disabled 1: Voltage monitor 0 reset enabled	R/W
b1	VW0C1	Voltage monitor 0 digital filter mode select bit (2, 3)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—	Reserved	The read value is undefined.	R
b4	VW0F0	Sampling clock select bits (3)	b5 b4 0 0: Division of fLOCO by 1 (no division) 0 1: Division of fLOCO by 2 1 0: Division of fLOCO by 4 1 1: Division of fLOCO by 8	R/W
b5	VW0F1			R/W
b6	—	Reserved	Set to 1.	R/W
b7	—			

Notes:

1. The VW0C0 bit is enabled when the VC0E bit in the VCA2 register is 1 (voltage detection 0 circuit enabled). When the VC0E bit is 0 (voltage detection 0 circuit disabled), set the VW0C0 bit to 0 (voltage monitor 0 reset disabled). To set the VW0C0 bit to 1 (voltage monitor 0 reset enabled), see **Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset**.
2. When the digital filter is used (while the VW0C1 bit is 0), set the LOCODIS bit in the OCOCR register to 0 (low-speed on-chip oscillator on).
   When the voltage monitor 0 reset is used to return from stop mode, set the VW0C1 bit to 1 (digital filter disabled mode).
3. When the VW0C0 bit is 1 (voltage monitor 0 reset enabled), do not set bits VW0C1 and VW0F0 to VW0F1 at the same time (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW0C register.

8.2 Registers

Table 8.2 lists the Watchdog Timer Register Configuration.

Table 8.2 Watchdog Timer Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Watchdog Timer Function Register	RISR	(Note 1)	00030h	8
Watchdog Timer Reset Register	WDTR	XXh	00031h	8
Watchdog Timer Start Register	WDTS	XXh	00032h	8
Watchdog Timer Control Register	WDTC	01XXXXXXb	00033h	8
Count Source Protection Mode Register	CSPR	(Note 1)	00034h	8
Periodic Timer Interrupt Control Register	WDTIR	00h	00035h	8

Note:
1. See the description of the individual registers.

8.2.1 Watchdog Timer Function Register (RISR)

Address 00030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RIS	UFIF	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 0.							
After Reset	0	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	UFIF	WDT underflow detection flag	0: No watchdog timer underflow 1: Watchdog timer underflow (1)	R/W
b7	RIS	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (2)	R/W

Notes:
1. After reading this bit as 1, wait at least one cycle of the count source before writing 0 to it.
2. The RIS bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.
   When the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), the RIS bit is automatically set to 1.

   Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the RISR register.

UFIF Bit (WDT underflow detection flag)

[Condition for setting to 0]
• When 0 is written to this bit.
[Conditions for setting to 1]
• When the watchdog timer underflows while the RIS bit is 0 (watchdog timer interrupt).
• When a refresh is executed during the period other than the acceptance period (illegal refresh) while the RIS bit is 0 (watchdog timer interrupt).

9.2 Registers

Table 9.3 lists the Clock Generation Circuit Register Configuration.

Table 9.3 Clock Generation Circuit Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
External Clock Control Register	EXCKCR	00h	00020h	8
High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h	00021h	8
System Clock f Control Register	SCKCR	00h	00022h	8
System Clock f Select Register	PHISEL	00h	00023h	8
Clock Stop Control Register	CKSTPR	00h	00024h	8
Clock Control Register When Returning from Modes	CKRSCR	00h	00025h	8
Oscillation Stop Detection Register	BAKCR	00h	00026h	8
High-Speed On-Chip Oscillator 18.432 MHz Control Register 0	FR18S0	Value when shipped	00064h	8
High-Speed On-Chip Oscillator 18.432 MHz Control Register 1	FR18S1	Value when shipped	00065h	8
High-Speed On-Chip Oscillator Control Register 1	FRV1	Value when shipped	00067h	8
High-Speed On-Chip Oscillator Control Register 2	FRV2	Value when shipped	00068h	8

9.3.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock and the peripheral function clock.

After the HOCOE bit in the OCOCR register is set to 1 (high-speed on-chip oscillator on) and the wait time for oscillation stabilization has elapsed, when the HSCKSEL bit in the SCKCR register is set to 1 (high-speed on-chip oscillator clock) and the SCKSEL bit in the CKSTPR register is set to 1 (fHSCK), the high-speed on-chip oscillator clock is the system base clock (fBASE).

Frequency adjustment data is stored in registers FRV1, FRV2, FR18S0, and FR18S1.

To adjust the frequency of the high-speed on-chip oscillator clock to 18.432 MHz, transfer the adjustment values in registers FR18S0 and FR18S1 to registers FRV1 and FRV2 respectively before use.

This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0 % when the serial interface is used in UART mode. (See **Table 16.8 Setting Example for Clock Asynchronous Serial I/O Mode (Internal Clock Selected)**).

9.3.3 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock and the peripheral function clock.

After the LOCODIS bit in the OCOCR register is set to 0 (low-speed on-chip oscillator on) and the wait time for oscillation stabilization has elapsed, when the LSCKSEL bit in the SCKCR register is set to 0 (low-speed on-chip oscillator clock) and the SCKSEL bit in the CKSTPR register is set to 0 (fLOCO), the low-speed on-chip oscillator clock is the system base clock (fBASE).

After a reset, the on-chip oscillator clock (with no division) is the CPU clock.

The frequency of the on-chip oscillator clock will vary greatly depending on the power supply voltage and operating ambient temperature. Application products must be designed with sufficient margin to allow for these variations in frequency.

11.3.2 Relocatable Vector Table

The relocatable vector table occupies 256 bytes beginning from the start address set in the INTB register. Table 11.6 lists the Relocatable Vector Table.

Table 11.6 Relocatable Vector Table

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Priority Level Setting (ILVL0 or ILVL2 to ILVLE)
BRK instruction (2)	+0 to +3 (+00000h to +00003h)	0	—
Flash ready	+4 to +7 (+00004h to +00007h)	1	ILVL05 to ILVL04
Reserved		2 to 3	—
Comparator B1	+16 to +19 (+00010h to +00013h)	4	ILVL21 to ILVL20
Comparator B3	+20 to +23 (+00014h to +00017h)	5	ILVL25 to ILVL24
Reserved	+24 to +27 (+00018h to +0001Bh)	6	—
Timer RC	+28 to +31 (+0001Ch to +0001Fh)	7	ILVL35 to ILVL34
Reserved	+32 to +35 (+00020h to +00023h)	8	—
Reserved	+36 to +39 (+00024h to +00027h)	9	—
Reserved	+40 to +43 (+00028h to +0002Bh)	10	—
Reserved	+44 to +47 (+0002Ch to +0002Fh)	11	—
Reserved	+48 to +51 (+00030h to +00033h)	12	—
Key input	+52 to +55 (+00034h to +00037h)	13	ILVL65 to ILVL64
A/D conversion	+56 to +59 (+00038h to +0003Bh)	14	ILVL71 to ILVL70
Reserved	+60 to +63 (+0003Ch to +0003Fh)	15	—
Reserved		16	—
UART0 transmission	+68 to +71 (+00044h to +00047h)	17	ILVL85 to ILVL84
UART0 reception	+72 to +75 (+00048h to +0004Bh)	18	ILVL91 to ILVL90
Reserved	+76 to +79 (+0004Ch to +0004Fh)	19	—
Reserved	+80 to +83 (+00050h to +00053h)	20	—
$\overline{\text{INT2}}$	+84 to +87 (+00054h to +00057h)	21	ILVLA5 to ILVLA4
Timer RJ2	+88 to +91 (+00058h to +0005Bh)	22	ILVLB1 to ILVLB0
Periodic timer	+92 to +95 (+0005Ch to +0005Fh)	23	ILVLB5 to ILVLB4
Timer RB2	+96 to +99 (+00060h to +00063h)	24	ILVLC1 to ILVLC0
$\overline{\text{INT1}}$	+100 to +103 (+00064h to +00067h)	25	ILVLC5 to ILVLC4
$\overline{\text{INT3}}$	+104 to +107 (+00068h to +0006Bh)	26	ILVLD1 to ILVLD0
Reserved		27 to 28	—
$\overline{\text{INT0}}$	+116 to +119 (+00074h to +00077h)	29	ILVLE5 to ILVLE4
Reserved		30	—
Reserved		31	—
Software (2)	+128 to +131 (+00080h to +00083h) to +252 to +255 (+000FCh to +000FFh)	32 to 63	—

Notes:
1. These addresses are relative to those indicated by the INTB register.
2. These interrupts are not disabled by the I flag.

11.6 Key Input Interrupt

A key input interrupt request is generated by one of the input edges on pins $\overline{KI0}$ to $\overline{KI3}$. The key input interrupt can be used as a key-on wakeup function to cancel wait mode or stop mode.

The KIiEN bit (i = 0 to 3) in the KIEN register is be used to select whether the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register is be used to select the input polarity.

When a low level is input to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), inputs to the other pins $\overline{KI0}$ to $\overline{KI3}$ are not detected as interrupts. Likewise, when a high level is input to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), inputs to the other pins $\overline{KI0}$ to $\overline{KI3}$ are not detected as interrupts.

Figure 11.11 shows the Block Diagram for Key Input Interrupts. Table 11.12 lists the Pin Configuration for Key Input Interrupts.

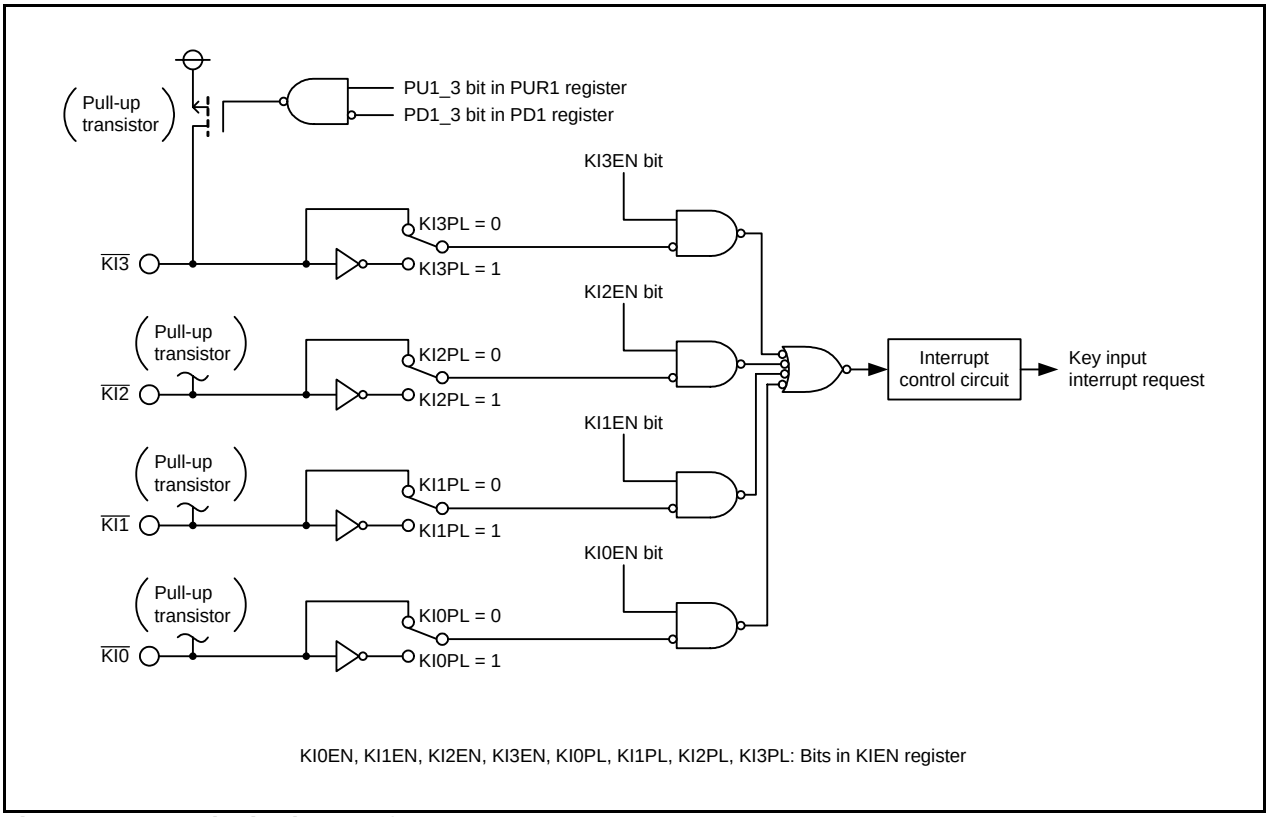


Figure 11.11 Block Diagram for Key Input Interrupts

Table 11.12 Pin Configuration for Key Input Interrupts

Pin Name	I/O	Function
$\overline{KI0}$	I	$\overline{KI0}$ interrupt input
$\overline{KI1}$	I	$\overline{KI1}$ interrupt input
$\overline{KI2}$	I	$\overline{KI2}$ interrupt input
$\overline{KI3}$	I	$\overline{KI3}$ interrupt input

12.5.5 Port 4 Function Mapping Register 0 (PML4)

Address 000CEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	P42SEL1	P42SEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	P42SEL0	Port P4_2 function select bits	b5 b4 0 0: I/O port 0 1: TRBO 1 0: $\overline{\text{TXD0}}$ 1 1: $\overline{\text{KI3}}$	R/W
b5	P42SEL1			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The PML4 register is used to select the P4_2 pin function.

12.5.6 Port 4 Function Mapping Register 1 (PMH4)

Address 000CFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P47SEL1	P47SEL0	P46SEL1	P46SEL0	P45SEL1	P45SEL0	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	P45SEL0	Port P4_5 function select bits	b3 b2 0 0: I/O port 0 1: $\overline{\text{INT0}}$ 1 0: $\overline{\text{ADTRG}}$ 1 1: Do not set.	R/W
b3	P45SEL1			R/W
b4	P46SEL0	Port P4_6 function select bits	bx b5 b4 0 0 0: I/O port or XIN input 0 0 1: RXD0 0 1 0: $\overline{\text{TXD0}}$ 0 1 1: $\overline{\text{INT1}}$ 1 0 0: VCOUT1 1 0 1: TRJIO Other than the above: Do not set. (bx: P46SEL2 bit in the PMH4E register)	R/W
b5	P46SEL1			R/W
b6	P47SEL0	Port P4_7 function select bits	b7 b6 0 0: I/O port or XOUT output 0 1: $\overline{\text{INT2}}$ Other than the above: Do not set.	R/W
b7	P47SEL1			R/W

The PMH4 register is used to select the functions of pins P4_5 to P4_7.

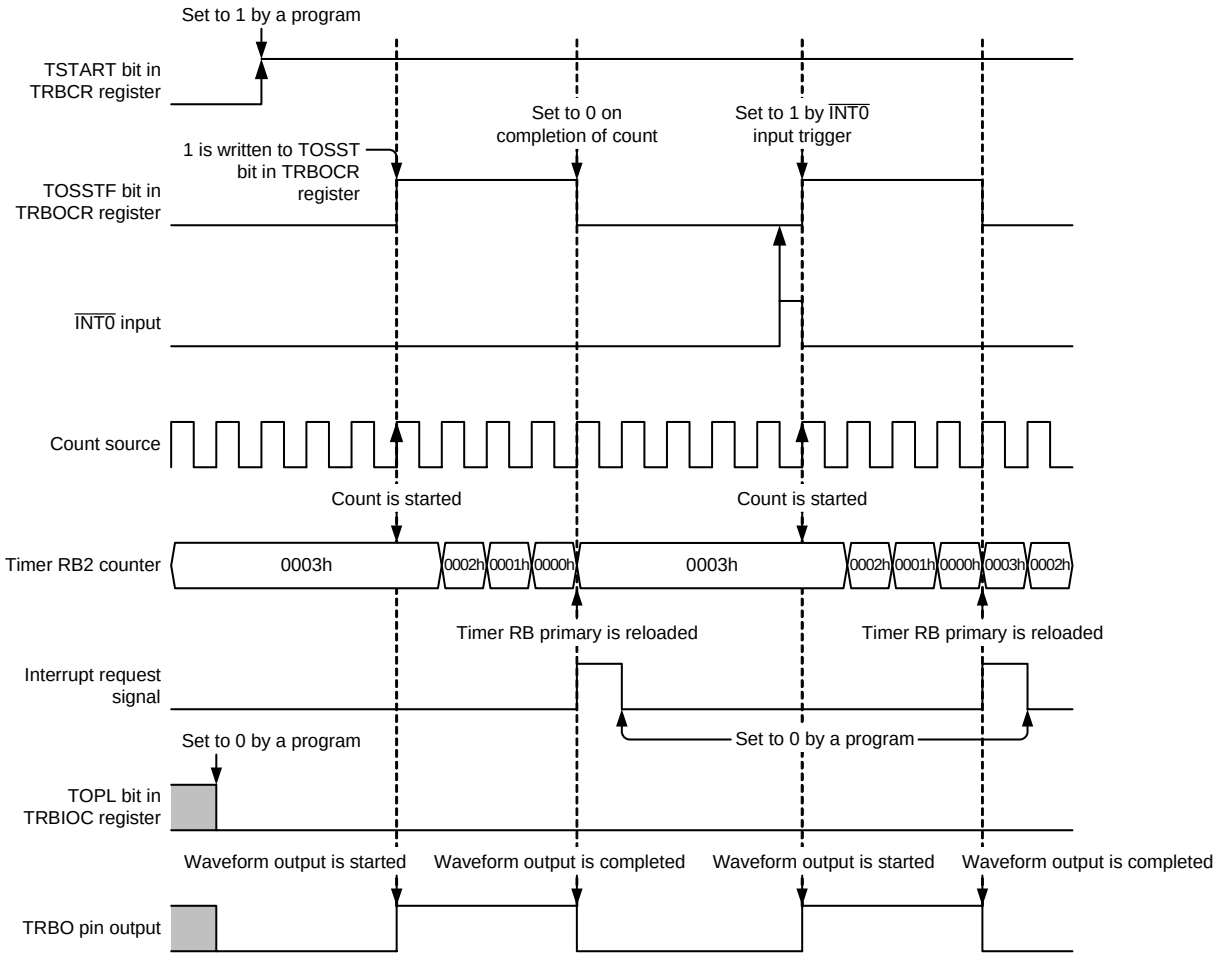
14.3.4 Timer RB Mode Register (TRBMR)

Address 000E3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TWRC	TCNT16	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bits (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	TCNT16	Timer RB counter select bit (1)	0: 8-bit timer with 8-bit prescaler 1: 16-bit timer	R/W
b3	TWRC	Timer RB write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RB count source select bits (1)	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: Timer RJ2 underflow 0 1 1: f2 1 0 0: f4 1 0 1: f32 1 1 0: f64 1 1 1: f128	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RB count source cutoff bit (1)	0: Count source is supplied 1: Count source is cut off	R/W

Notes:
1. Only change these bits when bits TSTART and TCSTF in the TRBCR register are 0 (count is stopped).
2. For details on writing to the register and counter using the TWRC bit, see **14.5.2 Prescaler and Counter Using TWRC Bit**.



The above diagram applies under the following conditions:
- TRBPRE register = 03h, TRBPR register = 00h
- TOPL bit = 0, TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

Figure 14.6 Example of 16-Bit Timer Operation in Programmable One-Shot Generation Mode

14.6 Interrupt Request

When the TRBIF bit in the TRBIR register is 1 (interrupt requested) and the TRBIE bit is 1 (interrupt enabled), an interrupt request is generated to the CPU. The conditions for setting the TRBIF bit to 1 differ depending on the mode. See the descriptions of the TRBIF bit and individual modes.

14.7 $\overline{\text{INT0}}$ Input Trigger Selection

In programmable one-shot and programmable wait one-shot generation modes, when 1 (one-shot count is started) is written to the TOSST bit in the TRBCR register or a trigger is input to the $\overline{\text{INT0}}$ pin with the TCSTF bit in the TRBCR register set to 1 (count is in progress), one-shot operation is started.

When using the trigger input from the $\overline{\text{INT0}}$ pin, make the following settings beforehand.

(1) Set the port mapping register to set port P1_4 or P4_5 as the $\overline{\text{INT0}}$ pin.
(2) Set bits INT0F0 to INT0F1 in the INTF0 register to select the digital filter sampling clock for the $\overline{\text{INT0}}$ pin.
(3) Set the INT0EN bit in the INTEN register to 1 (enabled) to enable an interrupt.
(4) Set the INOSEG bit in the TRBIOC register to select the falling or rising edge.
(5) Set the INOSTG bit in the TRBIOC register to 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled).

When an interrupt request is generated by the trigger input from the $\overline{\text{INT0}}$ pin, note the following:

- Set bits INT0SA to INT0SB in the ISCR0 register to select the falling edge, rising edge, or two-way edge for the interrupt.

Even if a one-shot trigger is generated while the TOSSTF bit in the TRBOCR is 1 (one-shot is operating (including wait period)), timer RB2 operation is not influenced, but the IRI0 bit in the IRR3 register is changed.
For details on interrupts, see **11. Interrupts**.

Figure 15.8 shows an Example of Buffer Operation during Input Capture. This example applies when the TRCGRA register is set as an input capture register and the TRCGRC register is set as a buffer register for the TRCGRA register. In this example, the TRCCNT register is used for the free-running count operation and both rising and falling edges are selected for the input capture input to the TRCIOA pin. Since buffer operation is set, the value in the TRCCNT register is stored in the TRCGRA register by input capture A and the value that has been stored in the TRCGRA register is transferred to the TRCGRC register at the same time.

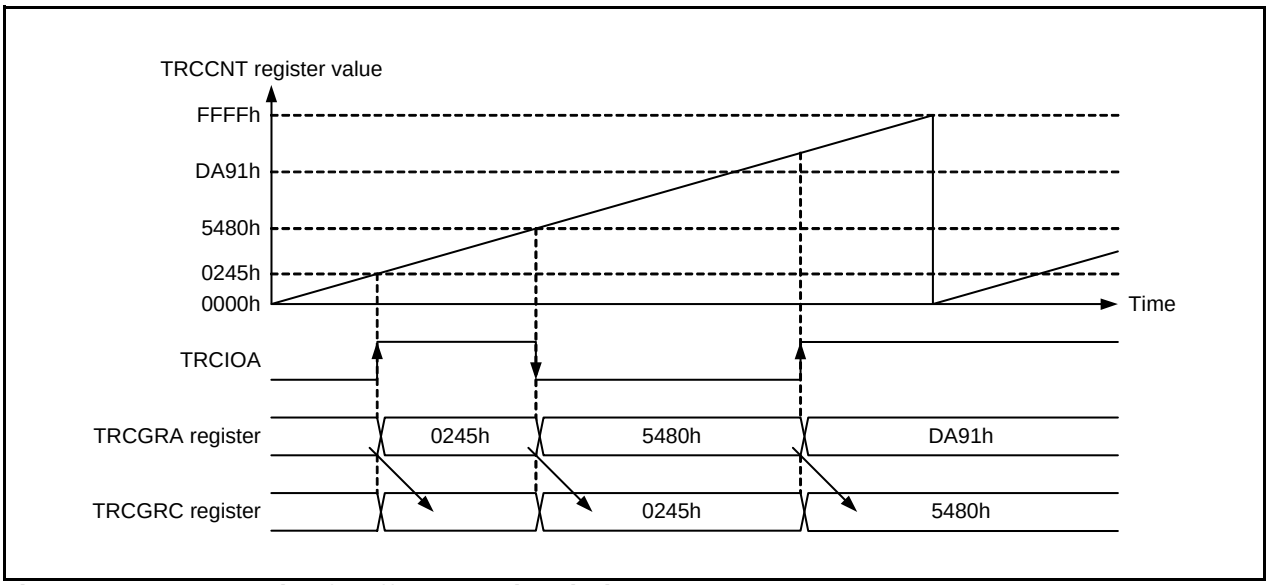


Figure 15.8 Example of Buffer Operation during Input Capture

15.7.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 15.1 Timer RC Specifications**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 15.19 Digital Filter Circuit Block Diagram**)

- The value of the TRCCNT register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

15.7.6 TRCMR Register in PWM2 Mode

When the CSTP bit in the TRCCR2 register is 1 (increment is stopped), do not set the TRCMR register when a compare match occurs between registers TRCCNT and TRCGRA.

15.7.7 MSTCR Register

After stopping the timer RC count, set the MSTTRC bit in the MSTCR register to 1 (standby).

15.7.8 Mode Switching

- When switching the modes during operation, set the CTS bit in the TRCMR register to 0 (count is stopped) before switching.
- After switching the modes, set each flag in the TRCSR register to 0 before operation is started.

15.7.9 Procedure for Setting Registers Associated with Timer RC

Set the registers associated with timer RC following the procedure below:

(1) Set timer RC operating mode (bits PWMB, PWMC, PWMD, and PWM2 in the TRCMR register).
(2) Set the registers other than that set in (1).
(3) Set the port output to be enabled (bits EA to ED in the TRCOER register).

19.5.4 Flash Memory Control Register 2 (FMR2)

Address 001ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Suspend enable bit (1)	0: Suspend disabled 1: Suspend enabled	R/W
b1	FMR21	Suspend request bit (2)	0: Restart 1: Suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Suspend request disabled by interrupt request 1: Suspend request enabled by interrupt request	R/W
b3	—	Reserved	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	FMR27	Low-current-consumption read mode enable bit (1, 3)	0: Low-current-consumption read mode disabled 1: Low-current-consumption read mode enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
2. The FMR21 bit can be set when the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMR20 bit is 1 (suspend enabled).
3. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU write mode disabled). Set this bit to 0 to perform A/D conversion.

FMR20 Bit (Suspend enable bit)

When the FMR20 bit is set to 1 (enabled), the suspend function is enabled.

FMR21 Bit (Suspend request bit)

When the FMR21 bit is set to 1 (suspend request), program/erase-suspend mode is entered. When the FMR22 bit is 1 (suspend request enabled by interrupt request), if an interrupt request for the enabled interrupt is generated, the FMR21 bit is automatically set to 1 (suspend request) and suspend mode is entered. To restart auto-erase or auto-programming, set the FMR21 bit to 0 (restart).

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Conditions for setting to 1]
- When the FMR22 bit is 1 (suspend request enabled by interrupt request) at the time an interrupt request is generated.
- When 1 is written to this bit by a program while the flash memory is busy.

FMR22 Bit (Interrupt request suspend request enable bit)

When the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) at the time an interrupt request is generated during auto-erase or auto-programming. Set the FMR22 bit to 1 when erase-suspend is used while the user ROM area is rewritten in EW1 mode.

Table 20.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Package	Condition	Standard			Unit
				Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset is cleared	14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	19.2	20.0	20.8	MHz
		14-pin DIP 20-pin DIP		19.0	20.0	21.0	MHz
		14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	19.0	20.0	21.0	MHz
	High-speed on-chip oscillator frequency when the FR18S0 register adjustment value is written into the FRV1 register and the FR18S1 register adjustment value into the FRV2 register (2)	14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	17.694	18.432	19.169	MHz
		14-pin DIP 20-pin DIP		17.510	18.432	19.353	MHz
		14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	17.510	18.432	19.353	MHz
—	Oscillation stabilization time	—		—	—	30	µs
—	Self power consumption at oscillation	—	Vcc = 5.0 V, Topr = 25 °C	—	530	—	µA

Notes:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0 % when the serial interface is used in UART mode.

Table 20.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fLOCO	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stabilization time		—	—	35	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25 °C	—	2	—	µA

Note:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.

Table 20.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = 25 °C.
2. Wait time until the internal power supply generation circuit stabilizes during power-on.

Table 20.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	—	ns
$t_{W(CKH)}$	CLK0 input high width	100	—	ns
$t_{W(CKL)}$	CLK0 input low width	100	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	50	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	50	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

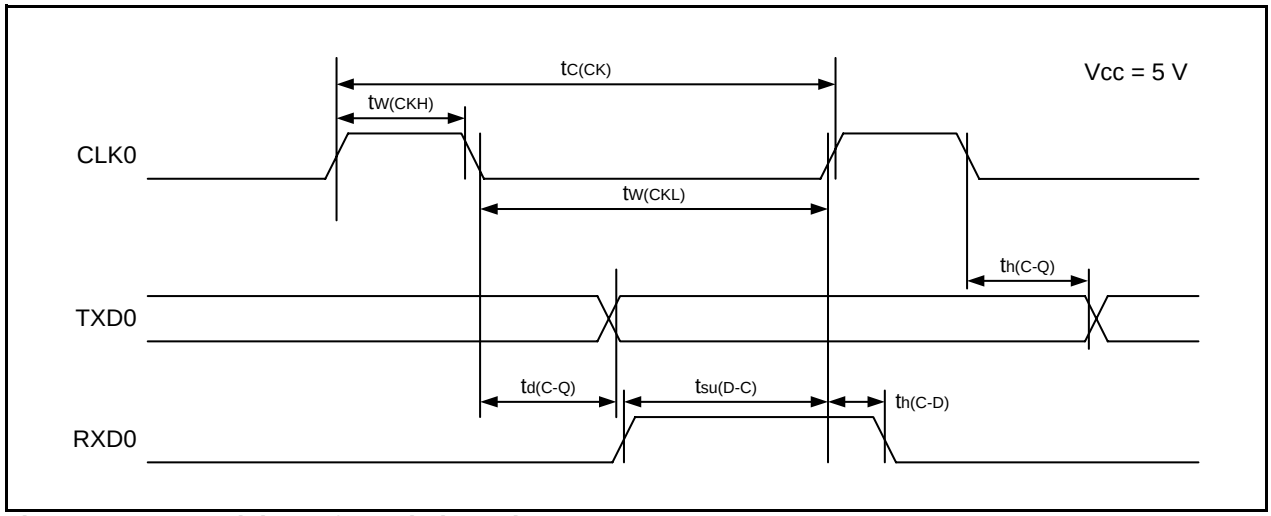


Figure 20.6 Serial Interface Timing When Vcc = 5 V

Table 20.18 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	250 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

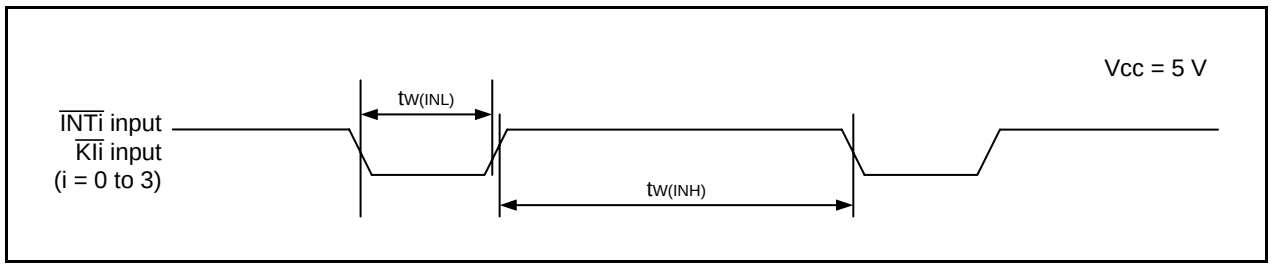


Figure 20.7 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 5 V

Appendix Tables 4.2 and 4.3 list the Register Comparison between R8C/M12A Group and R8C/M13B Group. For details on the R8C/M13B Group registers, refer to the R8C/M13B Group User's Manual: Hardware.

Appendix Table 4.2 Register Comparison between R8C/M12A Group and R8C/M13B Group (1)

Related Function	Register	Address	Bit	Remarks
System Control	MSTCR	00012h	MSTTRE	Functions added
	MSTCR1	00017h	MSTUART1, MSTTRK, MSTICSU, MSTIRDA	Register added
Clock	EXCKCR	00020h	CKPT1, CKPT0	Functions changed
			XCRCUT, XCINNC1, XCINNC0, CKPT3, CKPT2	Functions added
	SCKCR	00022h	LSCKSEL	Functions added
Interrupt	ILVL1	00041h	ILVL11, ILVL10	Register added
	ILVL5	00045h	ILVL51, ILVL50	Functions added
	ILVL7	00047h	ILVL75, ILVL74	Functions added
	ILVL9	00049h	ILVL95, ILVL94	Functions added
	ILVLA	0004Ah	ILVLA1, ILALA0	Functions added
	IRR0	00050h	IRS1R, IRS1T, IRTE	Functions added
	IRR1	00051h	IRTK, IRIS	Functions added
P0	PD0	000A8h		Register added
	P0	000AEh		Register added
	PUR0	000B4h		Register added
	POD0	000C0h		Register added
	PML0	000C6h		Register added
	PMH0	000C7h		Register added
P1_0, P1_2, P1_4, P1_5, P1_6	PML1	000C8h	P12SEL1, P12SEL0, P10SEL1, P10SEL0	Functions changed
	PMH1	000C9h	P16SEL1, P16SEL0, P15SEL1, P15SEL0, P14SEL1, P14SEL0	Functions changed
P2_0, P2_1, P2_2	PD2	000AAh	PD2_2, PD2_1, PD2_0	Register added
	P2	000B0h	P2_2, P2_1, P2_0	Register added
	PUR2	000B6h	PU2_2, PU2_1, PU2_0	Register added
	POD2	000C2h	POD2_2, POD2_1, POD2_0	Register added
	PML2	000CAh	P22SEL1, P22SEL0, P21SEL1, P21SEL0, P20SEL1, P20SEL0	Register added
P3_1, P3_3, P3_4	PD3	000ABh	PD3_1	Functions added
	P3	000B1h	P3_1	Functions added
	PUR3	000B7h	PU3_1	Functions added
	POD3	000C3h	POD3_1	Functions added
	PML3	000CCh	P33SEL1, P33SEL0	Functions changed
			P31SEL1, P31SEL0	Functions added
	PMH3	000CDh	P34SEL1, P34SEL0	Functions changed
P4_2, P4_5, P4_6, P4_7	PML4	000CEh	P42SEL1, P42SEL0	Functions changed
	PMH4	000CFh	P47SEL1, P47SEL0, P46SEL1, P46SEL0, P45SEL1, P45SEL0	Functions changed
AN5, AN6	ADINSEL	0009Dh	ADGSEL1, ADGSEL0	Functions changed

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.1