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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36079lhv

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6.2.3 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTINI	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period setting bits	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acceptance period setting bits	b3 b2 0 0: 25 % 0 1: 50 % 1 0: 75 % 1 1: 100 %	R/W
b3	WDTRCS1			R/W
b4	—	Reserved	Set to 1.	R/W
b5	MSTINI	MSTCR register initial value select bit	0: MSTCR register is set to 00h after reset 1: MSTCR register is set to 77h after reset	R/W
b6	—	Reserved	Set to 1.	R/W
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS2 register. Erasure of the block including the OFS2 register causes the OFS2 register to be set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For an example of the OFS2 register settings, see **5.6.1 Option Function Select Area Setting Example**.

Bits WDTUFS0 to WDTUFS1 (Watchdog timer underflow period setting bits)

These bits are used to select the underflow period for the watchdog timer.

Bits WDTRCS0 to WDTRCS1 (Watchdog timer refresh acceptance period setting bits)

These bits are used to select the refresh acceptance period as a percentage. Note that the period from the start of counting to underflow is 100 %.
For details, see **8.3.1.1 Refresh Acceptance Period**.

8.2.5 Count Source Protection Mode Register (CSPR)

Address 00034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 0.							
After Reset	0	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode enabled	R/W

Note:
1. To set the CSPRO bit to 1, first write 0 and then write 1 to it. This bit cannot be set to 0 by a program. Do not write to any register other than the CSPR register between writing 0 and then writing 1.

8.2.6 Periodic Timer Interrupt Control Register (WDTIR)

Address 00035h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTIE	WDTIF	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	WDTIF	Periodic timer interrupt request flag	0: No periodic timer interrupt requested 1: Periodic timer interrupt requested	R/W
b7	WDTIE	Periodic timer interrupt enable bit (1)	0: Periodic timer interrupt disabled 1: Periodic timer interrupt enabled	R/W

Note:
1. When bits WDTRCS1 to WDTRCS0 in the OFS2 register is 11b (100 %), set the WDTIE bit to 0 (periodic timer interrupt disabled).

WDTIF Bit (Periodic timer interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• When the watchdog timer completes counting an illegal write range.

9. Clock Generation Circuit

9.1 Overview

The following three circuits are included in the clock generation circuit:
• XIN clock oscillation circuit
• High-speed on-chip oscillator
• Low-speed on-chip oscillator
Table 9.1 lists the Clock Generation Circuit Specifications. Figure 9.1 shows the Clock Generation Circuit Block Diagram. Figure 9.2 shows the Supply of Peripheral Function Clocks. Table 9.2 lists the Clock Generation Circuit Pin Configuration.

Table 9.1 Clock Generation Circuit Specifications

Item	XIN Clock Oscillation Circuit	High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator
Clock frequency	0 MHz to 20 MHz (2 MHz to 20 MHz when an oscillator is used)	Approx. 20 MHz	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	—	—
Oscillator connect pins	XIN, XOUT (1)	—	—
Oscillation start and stop	Usable	Usable	Usable
State after reset	Stopped	Stopped	Oscillates
Others	• An externally generated clock can be input. • A feed-back resistor is included (connected or not connected can be selected).	The system clock can be output from P4_7.	The system clock can be output from P4_7.

Note:
1. When the on-chip oscillator clock instead of the XIN clock oscillation circuit is used as the CPU clock, these pins can be used as P4_6 and P4_7.

9.2.4 System Clock f Select Register (PHISEL)

Address 00023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PHISEL7	PHISEL6	PHISEL5	PHISEL4	PHISEL3	PHISEL2	PHISEL1	PHISEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b7 to b0	PHISEL7 to PHISEL0	System clock division ratio select bits	These bits used to set the division ratio of the system base clock (fBASE) to generate the system clock (f) and the A/D converter clock (fAD). • System clock (f) f = fBASE/(n + 1) • Clock for A/D converter (fAD) fAD = fBASE/(n + 1).....when (n + 1) is not a multiple of 4 fAD = 4 × fBASE/(n + 1)...when (n + 1) is a multiple of 4 n: Binary value set by the PHISEL register	00h to FFh	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the PHISEL register.
Table 9.6 lists the PHISEL Register Setting Example.

Table 9.6 PHISEL Register Setting Example

Value Set in PHISEL Register (n)	System Clock (f)	A/D Converter Clock (fAD)
00h	fBASE	fBASE
01h	Division of fBASE by 2	Division of fBASE by 2
02h	Division of fBASE by 3	Division of fBASE by 3
03h	Division of fBASE by 4	fBASE
04h	Division of fBASE by 5	Division of fBASE by 5
05h	Division of fBASE by 6	Division of fBASE by 6
06h	Division of fBASE by 7	Division of fBASE by 7
07h	Division of fBASE by 8	Division of fBASE by 2

10.3 Wait Mode

The watchdog timer is stopped when count source protection mode is disabled and the CPU clock is used. The XIN clock and the high-speed/low-speed on-chip oscillator clock are not stopped, so the peripheral functions that use these clocks continue operating. The system clock can be stopped with WCKSTP bit in the CKSTPR register. At this time, the peripheral functions that use the system clock and a divided system clock generated by the prescaler are stopped.

10.3.1 Peripheral Function Clock Stop Function

When the WCKSTP bit in the CKSTPR register is 1 (peripheral function clock stopped in wait mode), the system clock and the prescaler are stopped in wait mode to reduce power consumption. At this time, the peripheral functions that use the system clock and a divided system clock generated by the prescaler are stopped.

10.3.2 Entering Wait Mode

Wait mode is entered when the WAIT instruction is executed or the WAITM bit in the SCKCR register is set to 1 (wait mode is entered).

10.3.3 Pin States in Wait Mode

The I/O ports retain the states immediately before wait mode is entered.

11.2.5 Interrupt Priority Level Register i (ILVLi) (i = 0, or 2 to E)

Address 00040h (ILVL0), 00042h to 0004Eh (ILVL2 to ILVLE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	ILVLi5	ILVLi4	—	—	ILVLi1	ILVLi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVLi0	Interrupt priority level setting bits	b1 b0 0 0: Level 0 (interrupt disabled) 0 1: Level 1 1 0: Level 2 1 1: Level 2	R/W
b1	ILVLi1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	ILVLi4	Interrupt priority level setting bits	b5 b4 0 0: Level 0 (interrupt disabled) 0 1: Level 1 1 0: Level 2 1 1: Level 2	R/W
b5	ILVLi5			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The ILVLi register (i = 0, or 2 to E) is used to set the priority levels (levels 0 to 2) of the maskable interrupts. The settings in bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5 in each register are used to decide the priority of the corresponding interrupt request.

See **Table 11.4 Correspondence between Interrupt Requests and ILVLi (i = 0, or 2 to E)** for the interrupt setting bits.

The interrupt priority level register must be rewritten only while no interrupt requests corresponding to that register are generated. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers**.

Table 11.4 Correspondence between Interrupt Requests and ILVLi (i = 0, or 2 to E)

ILVLi Register	Bit							
	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	ILVLi5	ILVLi4	—	—	ILVLi1	ILVLi0
ILVL0	—	—	Flash ready		—	—	—	
ILVL2	—	—	Comparator B3		—	—	Comparator B1	
ILVL3	—	—	Timer RC		—	—	—	
ILVL4	—	—	—		—	—	—	
ILVL5	—	—	—		—	—	—	
ILVL6	—	—	Key input		—	—	—	
ILVL7	—	—	—		—	—	A/D conversion	
ILVL8	—	—	UART0 transmission		—	—	—	
ILVL9	—	—	—		—	—	UART0 reception	
ILVLA	—	—	$\overline{\text{INT2}}$		—	—	—	
ILVLB	—	—	Periodic timer		—	—	Timer RJ2	
ILVLC	—	—	$\overline{\text{INT1}}$		—	—	Timer RB2	
ILVLD	—	—	—		—	—	$\overline{\text{INT3}}$	
ILVLE	—	—	$\overline{\text{INT0}}$		—	—	—	

—: Not used. The write value must be 0.
i = 0, or 2 to E

12. I/O Ports

There are 17 I/O ports. P4_6 and P4_7 can be used as I/O ports when the XIN clock oscillation circuit is not used. PA_0 can be used as an I/O port when a hardware reset is not used. In addition, all the ports are multiplexed with multiple peripheral functions.

12.1 Overview

The functions of the ports are selected by the peripheral function mapping registers (PMLi/PMHi, i = 1, 3, or 4) and the peripheral function mapping expansion registers (PMH1E and PMH4E). The functions of the I/O ports are selected by the port direction registers (PDi, i = 1, 3, 4, or A). In addition, the drive capacity of some ports can be switched. Table 12.1 shows the I/O Port Overview. Table 12.2 lists the Port Functions by Pin (R8C/M12A Group). Table 12.3 lists the I/O Port Register Configuration.

Table 12.1 I/O Port Overview

Ports	I/O	Output Type	I/O Setting	Internal Pull-Up Resistor	Drive Capacity Switching
P1_0 to P1_7	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (3)	Set in 1-bit units. (4)
P3_3, P3_4, P3_5, P3_7	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (3)	Set in 1-bit units. (4)
PA_0 (1)	I/O	3-state CMOS	Set in 1-bit units.	None	None
P4_2, P4_5, P4_6, P4_7 (2)	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (3)	None

Notes:
1. When the hardware reset is not used, this port can be used as an I/O port.
2. When the XIN clock oscillation circuit or direct input of the XIN clock is not used, these can be used as I/O ports.
3. In input mode, whether an internal pull-up resistor is connected or not can be selected by the PURi register (i = 1, 3, or 4).
4. The drive capacity of the output transistors (low or high) can be selected by the DRRi register (i = 1 or 3).

Table 12.2 Port Functions by Pin (R8C/M12A Group)

Pin Number	R8C/M12A Group	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function Select Bit		
		PM2 to PM0 = 000b	PM2 to PM0 = 001b	PM2 to PM0 = 010b	PM2 to PM0 = 011b	PM2 to PM0 = 100b	PM2 to PM0 = 101b	PM2	PM1	PM0
1	P4_2	P4_2	TRBO	TXD0	$\overline{KI3}$	—	—	—	P42SEL1	P42SEL0
2	P3_7	P3_7	$\overline{ADTRG}$	TRJO	TRCIOD	—	—	—	P37SEL1	P37SEL0
3	$\overline{RESET}$	PA_0	—	—	—	—	—	—	—	—
4	P4_7/XOUT	P4_7/XOUT	$\overline{INT2}$	—	—	—	—	—	P47SEL1	P47SEL0
5	VSS/AVSS	—	—	—	—	—	—	—	—	—
6	P4_6/XIN	P4_6/XIN	RXD0	TXD0	$\overline{INT1}$	VCOUT1	TRJIO	P46SEL2	P46SEL1	P46SEL0
7	VCC/AVCC	—	—	—	—	—	—	—	—	—
8	MODE	—	—	—	—	—	—	—	—	—
9	P3_5	P3_5	TRCIOD	$\overline{KI2}$	VCOUT3	—	—	—	P35SEL1	P35SEL0
10	P3_4	P3_4/IVREF3	TRCIOC	$\overline{INT2}$	—	—	—	—	P34SEL1	P34SEL0
11	P3_3	P3_3/IVCMP3	TRCCLK	$\overline{INT3}$	—	—	—	—	P33SEL1	P33SEL0
12	P4_5	P4_5	$\overline{INT0}$	$\overline{ADTRG}$	—	—	—	—	P45SEL1	P45SEL0
13	P1_7	P1_7/AN7/ IVCMP1	$\overline{INT1}$	TRJIO	TRCCLK	—	—	—	P17SEL1	P17SEL0
14	P1_6	P1_6/IVREF1	CLK0	TRJO	TRCIOB	—	—	—	P16SEL1	P16SEL0
15	P1_5	P1_5	RXD0	TRJIO	$\overline{INT1}$	VCOUT1	—	P15SEL2	P15SEL1	P15SEL0
16	P1_4	P1_4/AN4	TXD0	RXD0	$\overline{INT0}$	TRCIOB	—	P14SEL2	P14SEL1	P14SEL0
17	P1_3	P1_3/AN3	TRCIOC	$\overline{KI3}$	TRBO	—	—	—	P13SEL1	P13SEL0
18	P1_2	P1_2/AN2	TRCIOB	$\overline{KI2}$	—	—	—	—	P12SEL1	P12SEL0
19	P1_1	P1_1/AN1	TRCIOA/ TRCTRG	$\overline{KI1}$	—	—	—	—	P11SEL1	P11SEL0
20	P1_0	P1_0/AN0	TRCIOD	$\overline{KI0}$	—	—	—	—	P10SEL1	P10SEL0

12.9 Handling of Unused Pins

Table 12.25 lists the Handling of Unused Pins. Figure 12.5 shows the Handling of Unused Pins.

Table 12.25 Handling of Unused Pins

Pin Name	Connection
Ports P1, P3_3 to P3_5, P3_7, P4_2, P4_5 to 4_7	• Set each of these pins to input mode, and either connect the pin to VSS through a resistor (pull-down) or connect it to VCC through a resistor (pull-up). (2) • Set each of these pins to output mode and leave it open. (2, 3)
$\overline{\text{RESET}}$/PA_0 (1)	Connect to VCC through a pull-up resistor. (2)

Notes:
1. When the power-on reset is used.
2. Use lines that are as short as possible (2 cm or shorter) to handle unused pins in the vicinity of the MCU.
3. When these ports are set to output mode and left open, keep the following in mind. They remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be unstable and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. The program should periodically reconfigure the content for enhanced reliability.

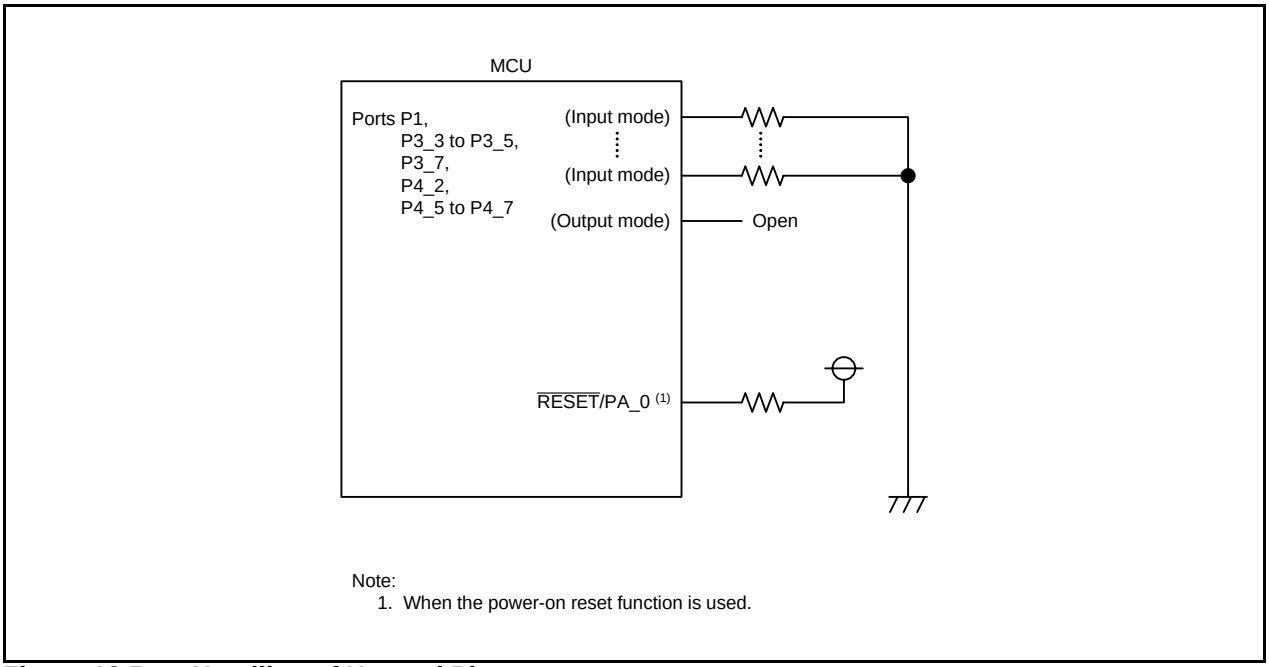
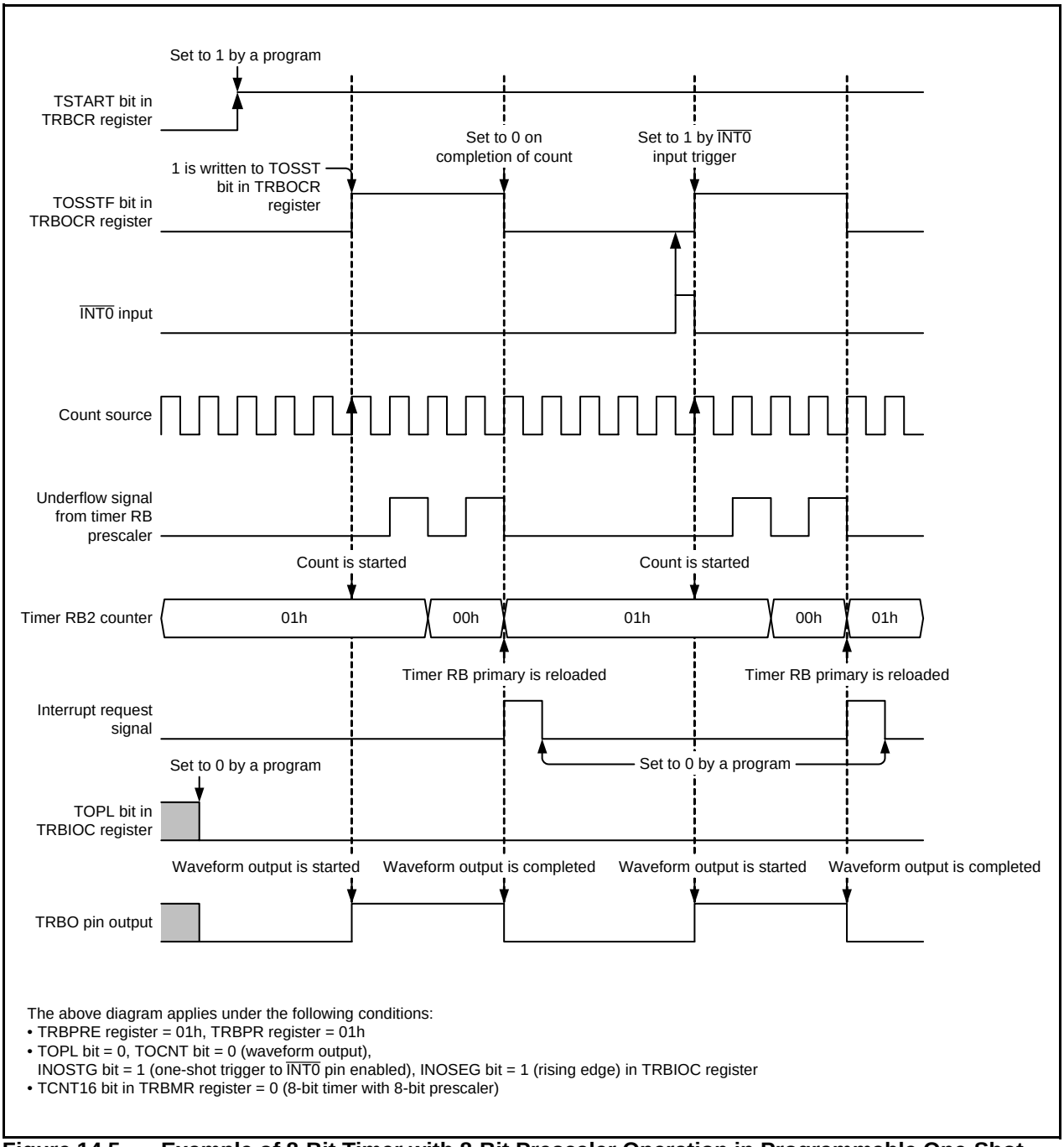


Figure 12.5 Handling of Unused Pins



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h
- TOPL bit = 0, TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

Figure 14.5 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable One-Shot Generation Mode

14.6 Interrupt Request

When the TRBIF bit in the TRBIR register is 1 (interrupt requested) and the TRBIE bit is 1 (interrupt enabled), an interrupt request is generated to the CPU. The conditions for setting the TRBIF bit to 1 differ depending on the mode. See the descriptions of the TRBIF bit and individual modes.

14.7 $\overline{\text{INT0}}$ Input Trigger Selection

In programmable one-shot and programmable wait one-shot generation modes, when 1 (one-shot count is started) is written to the TOSST bit in the TRBCR register or a trigger is input to the $\overline{\text{INT0}}$ pin with the TCSTF bit in the TRBCR register set to 1 (count is in progress), one-shot operation is started.

When using the trigger input from the $\overline{\text{INT0}}$ pin, make the following settings beforehand.

(1) Set the port mapping register to set port P1_4 or P4_5 as the $\overline{\text{INT0}}$ pin.
(2) Set bits INT0F0 to INT0F1 in the INTF0 register to select the digital filter sampling clock for the $\overline{\text{INT0}}$ pin.
(3) Set the INT0EN bit in the INTEN register to 1 (enabled) to enable an interrupt.
(4) Set the INOSEG bit in the TRBIOC register to select the falling or rising edge.
(5) Set the INOSTG bit in the TRBIOC register to 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled).

When an interrupt request is generated by the trigger input from the $\overline{\text{INT0}}$ pin, note the following:

- Set bits INT0SA to INT0SB in the ISCR0 register to select the falling edge, rising edge, or two-way edge for the interrupt.

Even if a one-shot trigger is generated while the TOSSTF bit in the TRBOCR is 1 (one-shot is operating (including wait period)), timer RB2 operation is not influenced, but the IRI0 bit in the IRR3 register is changed.
For details on interrupts, see **11. Interrupts**.

15.2.10 Timer RC Digital Filter Function Select Register (TRCDF)

Address 000F9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA digital filter function bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB digital filter function bit (1)		R/W
b2	DFC	TRCIOC digital filter function bit (1)		R/W
b3	DFD	TRCIOD digital filter function bit (1)		R/W
b4	DFTRG	TRCTRG digital filter function bit (2)		R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	DFCK0	Digital filter clock select bits (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits CKS2 to CKS0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. Enabled in the input capture function.
2. Enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

Figure 15.18 shows an Example of One-Shot Waveform Output Operation in PWM2 Mode (Count is Started by TRCTRG Input).
After the CTS bit in the TRCMR register is set to 1 (count is started), the increment is started on the rising edge of TRCIOA/TRCTRG, and the counter is changed to 0000h by a compare match with the TRCGRA register, the count operation is stopped, and a one-shot waveform is output under the following conditions.

- Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 10b (falling edge) to set the falling edge of the TRCTRG input.
- The CSTP bit in the TRCCR2 register is set to 1 (increment is stopped) to stop the increment when a compare match with the TRCGRA register occurs.
- The CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by a compare match.
- The TOB bit in the TRCCR1 register is set to 0 (output value 0) to set the initial value of the output level to 0.

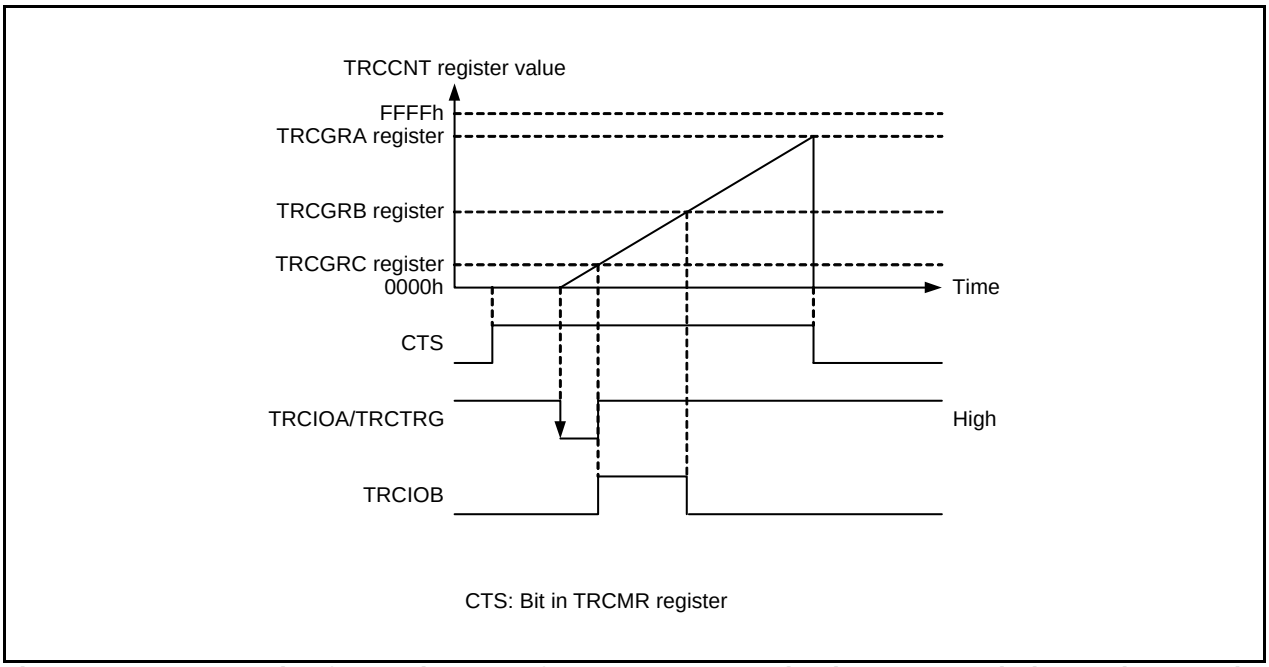


Figure 15.18 Example of One-Shot Waveform Output Operation in PWM2 Mode (Count is Started by TRCTRG Input)

16.2 Registers

Table 16.3 lists the UART0 Register Configuration.

Table 16.3 UART0 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
UART0 Transmit/Receive Mode Register	U0MR	00h	00080h	8
UART0 Bit Rate Register	U0BRG	XXh	00081h	8
UART0 Transmit Buffer Register	U0TBL	XXh	00082h	8 (1)
	U0TBH	XXh	00083h	8 (1)
UART0 Transmit/Receive Control Register 0	U0C0	00001000b	00084h	8
UART0 Transmit/Receive Control Register 1	U0C1	00000010b	00085h	8
UART0 Receive Buffer Register	U0RBL	XXh	00086h	8 (1)
	U0RBH	XXh	00087h	8 (1)
UART0 Interrupt Flag and Enable Register	U0IR	00h	00088h	8

X: Undefined

Note:

1. For details on access, see the description of the individual registers.

16.2.1 UART0 Transmit/Receive Mode Register (U0MR)

Address 00080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bits (1, 2)	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than the above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit (3)	0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved	Set to 0.	R/W

Notes:

1. When setting bits SMD2 to SMD0 to 000b (serial interface disabled), set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. When bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode), the error flags (bits FER, PER, and SUM) in the U0RB register are disabled. When these bits are read, the values are undefined.
3. The PRY bit is enabled when the PRTYE bit is 1 (parity enabled).

16.3 Operation

UART0 supports two modes: Clock synchronous serial I/O mode and clock asynchronous serial I/O (UART) mode.

16.3.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, transmission or reception is performed using a transfer clock.
Table 16.4 lists the Clock Synchronous Serial I/O Mode Specifications. Table 16.5 lists the Registers and Settings Used in Clock Synchronous Serial I/O Mode.

Table 16.4 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fi/(2 (n + 1)) fi = f1, f8, or f32 n = Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT (input from the CLK0 pin)
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U0C1 register must be 1 (transmission enabled). • The TI bit in the U0C1 register must be 0 (data present in the U0TB register).
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U0C1 register must be 1 (reception enabled). • The TE bit in the U0C1 register must be 1 (transmission enabled). • The TI bit in the U0C1 register must be 0 (data present in the U0TB register).
Interrupt request generation timing	• For transmission: One of the following can be selected. - The U0IRS bit in the U0C1 register is 0 (transmit buffer is empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit in the U0C1 register is 1 (transmission is completed): When data transmission from the UART0 transmit register is completed. • For reception: When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (2) This error occurs if the next data reception is started and the 7th bit is received before the U0RB register is read.
Selectable functions	• CLK polarity selection The output and input timing of transfer data can be selected to be either the rising or the falling edge of the transfer clock. • LSB first or MSB first selection The start bit can be selected to be bit 0 or bit 7 when transmission and reception are started. • Continuous receive mode selection Reading the U0RB register enables reception at the same time.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   • The external clock is set to high when the CKPOL bit in the U0C0 register is 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock).
   • The external clock is set to low when the CKPOL bit is 1 (transmit data is output on the rising edge and receive data is input on the falling edge of the transfer clock).
2. If an overrun error occurs, the receive data (b0 to b7) in the U0RB register is undefined. The U0RIF bit in the U0IR register remains unchanged.

16.3.2.3 RXD0 Digital Filter

When the DFE bit in the U0C0 register is 1 (digital filter enabled), the RXD0 input is latched internally through the digital filter circuit for noise cancellation. The noise canceller consists of three cascaded latch circuits and a match detection circuit. When the RXD0 input is sampled on the base clock with frequency of 16 times the transfer rate and three latch outputs match, the level is passed forward to the next circuit. When they do not match, the previous level is retained.

That is, if the RXD0 input retains the same level for three clocks or more, it is recognized as a signal. If not, it is recognized as noise.

Figure 16.8 shows the RXD0 Digital Filter Block Diagram.

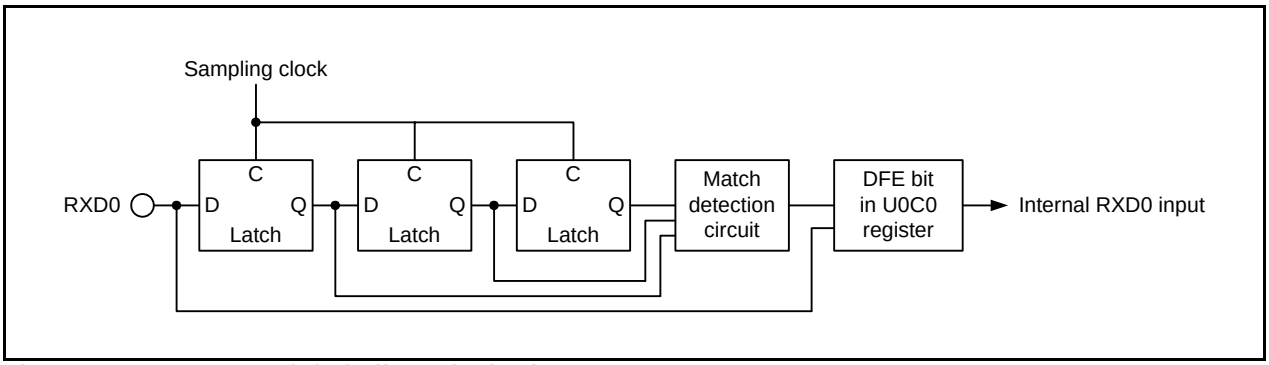


Figure 16.8 RXD0 Digital Filter Block Diagram

16.3.2.4 Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedure below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

17.3 Operation

This A/D converter provides operating four modes: One-shot, repeat, single sweep, and repeat sweep modes. This converter is a successive approximation type with 10-bit resolution.
The operating mode, analog input channel, and A/D conversion clock should be switched while the ADST bit in the ADCON0 register is 0 (A/D conversion stops).

17.3.1 Items Common to Multiple Modes

17.3.1.1 Input Sampling and A/D Conversion Time

The A/D converter includes a sample and hold circuit. When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts), the A/D converter samples the input and starts conversion after the A/D conversion start delay time (tD) has elapsed.
Figure 17.2 shows the A/D Conversion Timing. Table 17.6 lists the A/D Conversion Time.
As shown in Figure 17.2, the A/D conversion time (tCONV) includes tD and the input sampling time (tSPL). Here, tD is determined by the timing for writing to the ADCON0 register and is not a fixed value. The conversion time, therefore, varies within the range shown in Table 17.6.
In one-shot mode and single sweep mode, the ADF bit in the ADICSR register is set to 1 during end processing time, and the last A/D conversion result is stored in the ADi register.

- In one-shot mode
  A/D conversion time (tCONV) + end processing time (tEND)
- When two channels are selected in single sweep mode
  A/D conversion time (tCONV) + A/D conversion time (tCONV with no start delay time (tD) included) + end processing time (tEND)

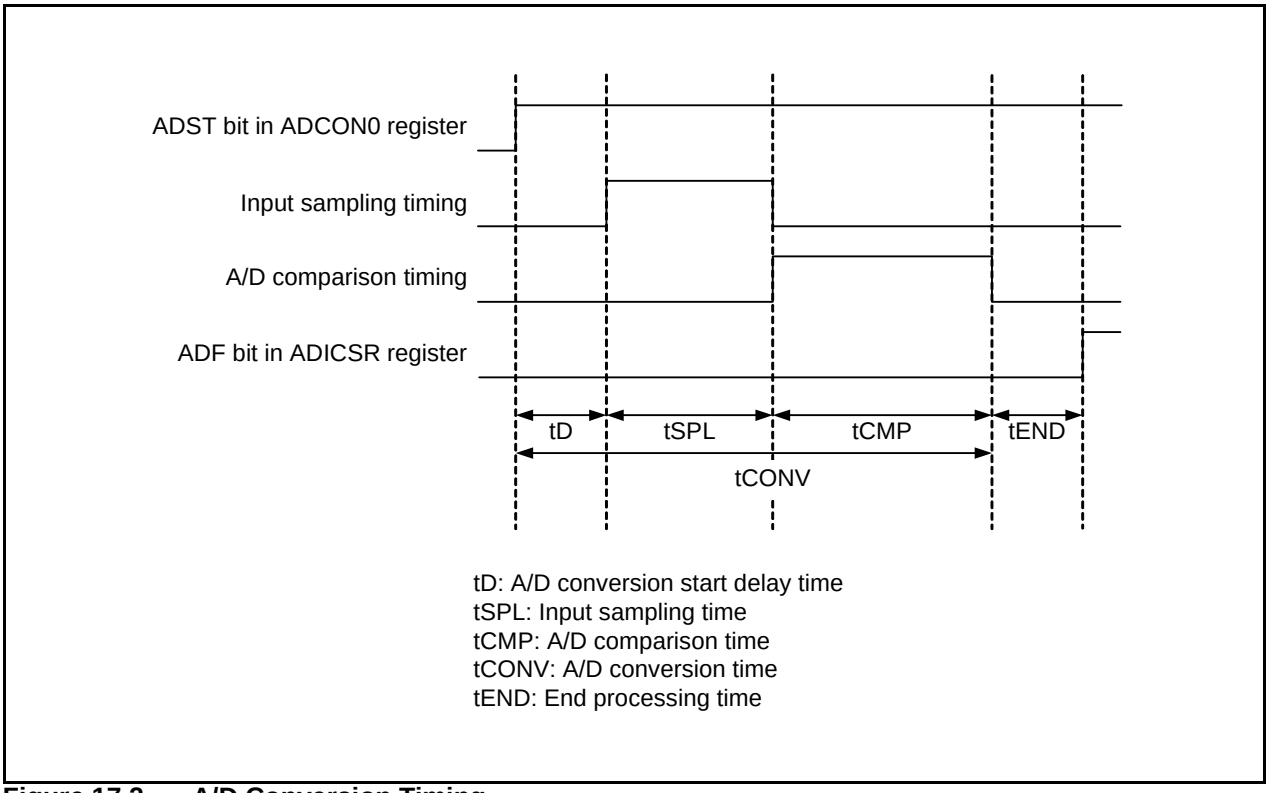


Figure 17.2 A/D Conversion Timing

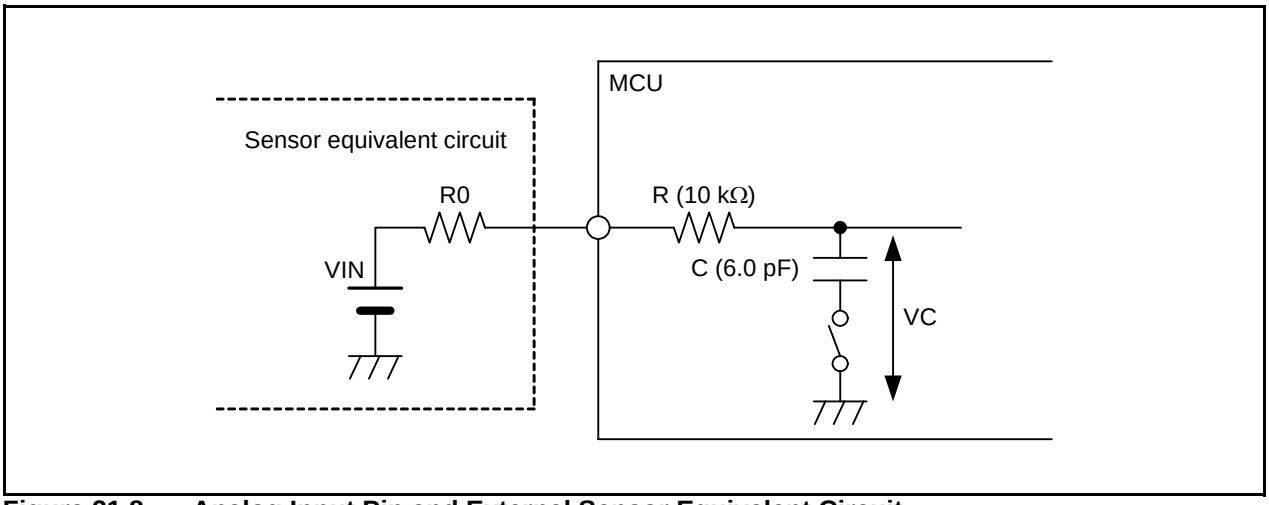


Figure 21.8 Analog Input Pin and External Sensor Equivalent Circuit

21.11.3 Register Setting

- Registers ADMOD and ADINSEL must be written only when A/D conversion is stopped.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion while the WCKSTP bit in the CKSTPR register is 1 (system clock is stopped in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory is stopped) or the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled) during A/D conversion.
- During A/D conversion, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate the conversion, the conversion result from the A/D converter will be undefined and no interrupt will be generated. The value of the ADi register (i = 0 or 1) which is not engaged in A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use any of the values of the ADi register.
- When using the A/D converter, it is recommended that the average of the conversion results be taken.

21.12.3 Notes on Flash Memory Stop and Operation Transition

(1) Do not enter stop mode while the FMSTP bit is 1 (the flash memory is stopped).
(2) Do not enter wait mode while the FMSTP bit is 1 (the flash memory is stopped) and the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
(3) Do not enter flash memory stop state for 42 μs after entering from flash memory stop state to flash memory operation state. And do not rewrite the LOCODIS bit in the OCOCR register for 42 μs.

Conditions when entering flash memory operation state from flash memory stop state.
• Set the FMSTP bit to 0 (the flash memory operates).
• Return from wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Return from stop mode.

Conditions when entering flash memory stop state from flash memory operation state.
• Set the FMSTP bit to 1 (the flash memory is stopped).
• Enter wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Enter stop mode.

REVISION HISTORY	R8C/M11A Group, R8C/M12A Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Nov 30, 2010	68	Table 8.3 revised, Notes 2 and 3 deleted
		69	Table 8.4 Notes 1 to 3 deleted
		70	Table 8.5 revised, Note 1 added, and Figure 8.3 revised
		71	8.4 revised
		72 to 90	"9. Clock Generation Circuit" revised
		91, 379	9.6, 21.3 revised
		92 to 106	"10. Power Control" revised
		107, 380	10.6, 21.4 revised
		108	Table 11.1 revised
		111	11.2.1 Note 1 added
		113	11.2.4 Note 1 revised
		115	11.2.6 and 11.2.7 revised
		116	11.2.8 revised
		118	11.2.10 and 11.2.11 "The resister remains ... or software reset." added
		119	Table 11.5 "0FFE7h" → "0FFE6h"
		121	11.4.2 revised, Table 11.7 added
		122	11.4.3 revised
		123	11.4.4 (1) revised
		125	11.4.7 revised
		128	Figure 11.8 Note 1 deleted
		129	11.5.1 revised
		130	11.5.2 and Figure 11.9 revised
		131	Figure 11.11 revised
		132	11.7 revised
		133	Figure 11.12 revised
		135, 382	11.9.4,21.5.4, Figure 11.13, and Figure 21.1 revised
		136, 383	11.9.5, 21.5.5 revised, Figure 11.14, Figure 21.2 added
		137, 384	11.9.6, 21.5.6, Figure 11.15, Figure 21.3 added
		140	12.2 and 12.2.1 revised
		142	12.3.2 revised
		143	12.3.4 Note 1 added
		148	Tables 12.9 and 12.10 revised
		150	12.4.2 revised
		151	12.4.4 Note 1 added
		154	Table 12.15 revised
		156	12.5.2 revised
		160	Table 12.16, Table 12.18, and Table 12.19 revised
		162	12.6.2 revised
		163	12.7 added
		166	Figure 12.6 revised, Figure 12.7 added
		167	Figure 12.9 revised
		168	Figure 12.10 revised