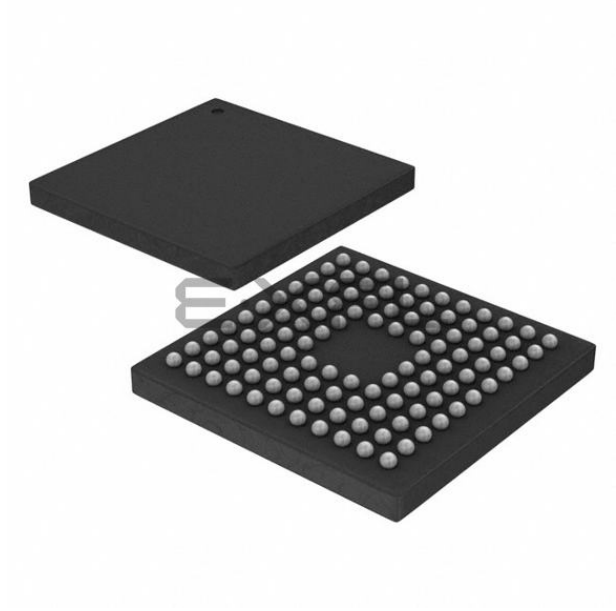
# Silicon Labs - EFM32GG390F1024G-E-BGA112 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 87 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 112-LFBGA |
| Supplier Device Package | 112-BGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32gg390f1024g-e-bga112 |

s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

## 2.1.18 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

## 2.1.19 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

## 2.1.20 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

## 2.1.21 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

## 2.1.22 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

## 2.1.23 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

## 2.1.24 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

## 2.1.25 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

### 2.1.26 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

### 2.1.27 Operational Amplifier (OPAMP)

The EFM32GG390 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

### 2.1.28 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE™), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

### 2.1.29 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32GG390 to keep track of time and retain data, even if the main power source should drain out.

### 2.1.30 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

### 2.1.31 General Purpose Input/Output (GPIO)

In the EFM32GG390, there are 86 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

## 2.2 Configuration Summary

The features of the EFM32GG390 is a subset of the feature set described in the EFM32GG Reference Manual. Table 2.1 (p. 8) describes device specific implementation of the features.

| Module | Configuration | Pin Connections |
|---|---|---|
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 86 pins | Available pins are shown in Table 4.3 (p. 63) |

## 2.3 Memory Map

The *EFM32GG390* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

***Figure 2.2. EFM32GG390 Memory Map with largest RAM and Flash sizes***

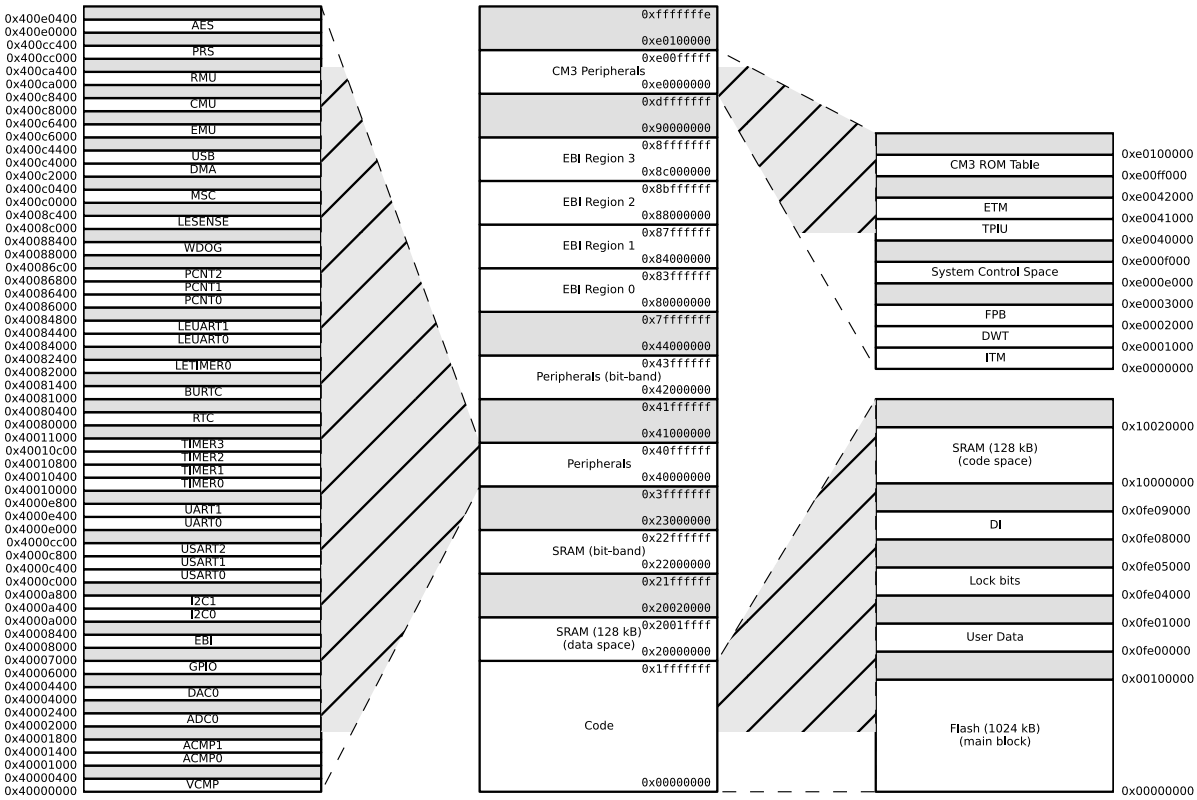
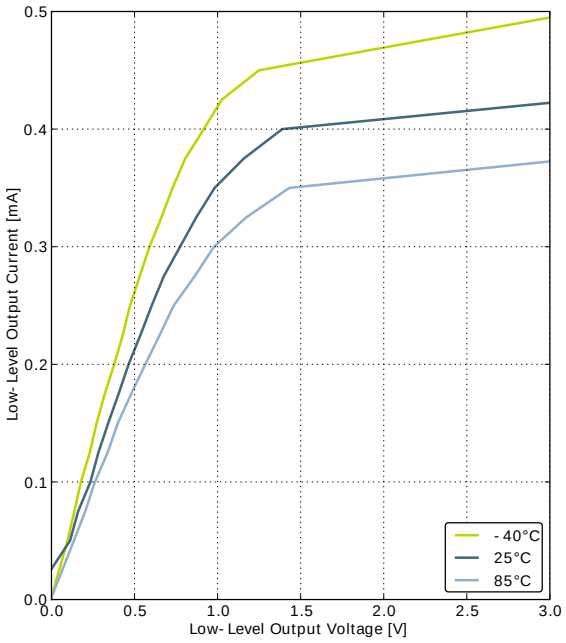
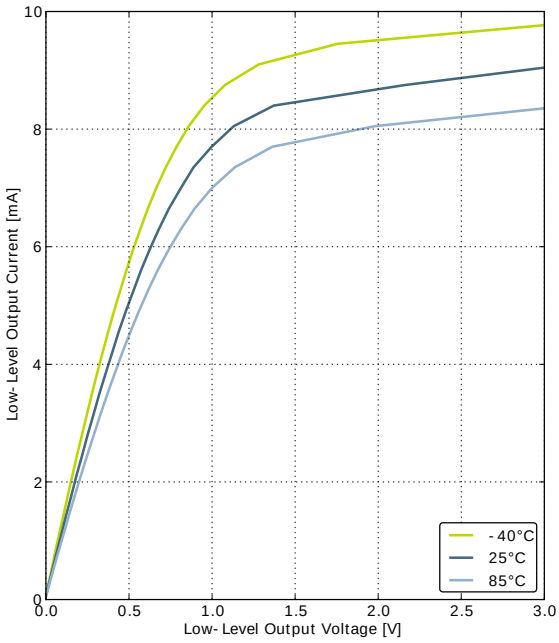


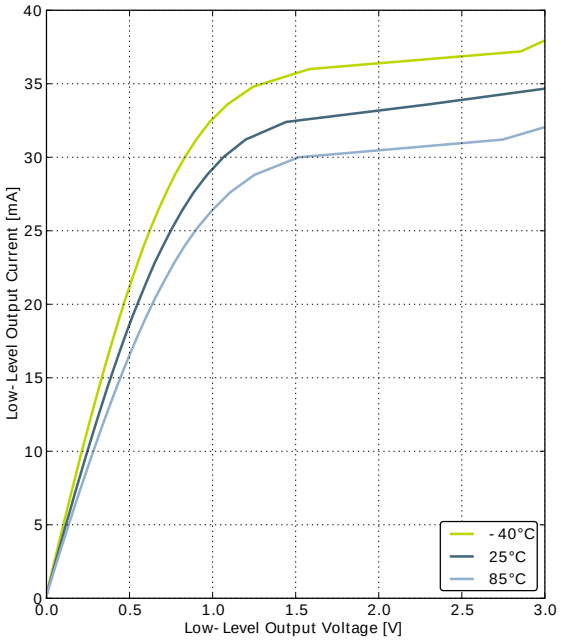
***Figure 3.6. Typical Low-Level Output Current, 3V Supply Voltage***



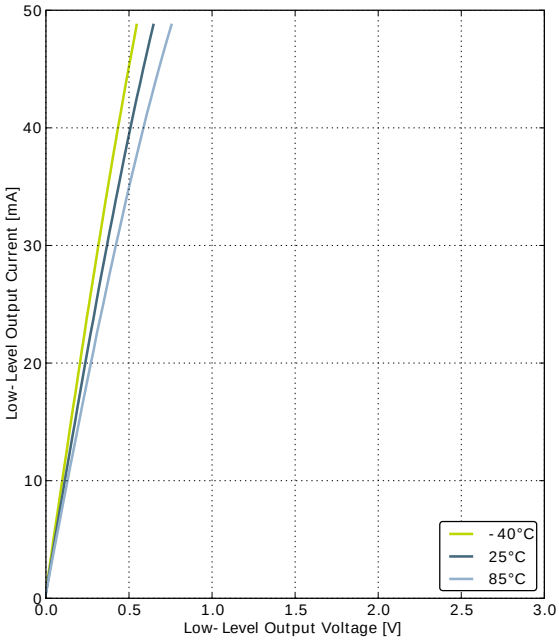

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

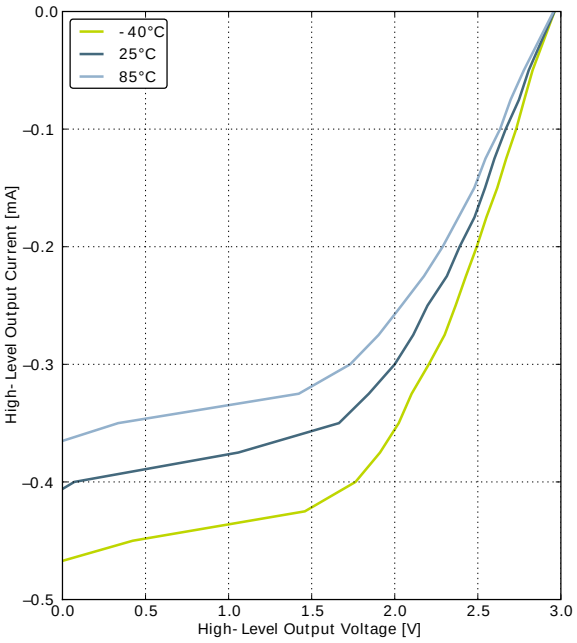



GPIO_Px_CTRL DRIVEMODE = STANDARD

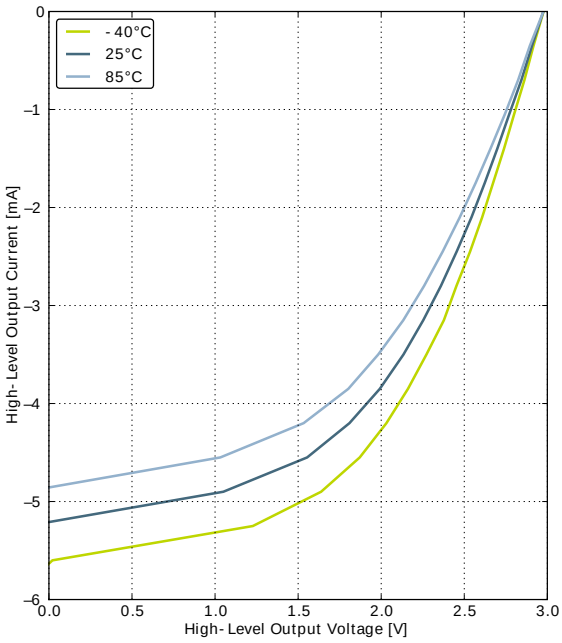



GPIO_Px_CTRL DRIVEMODE = HIGH

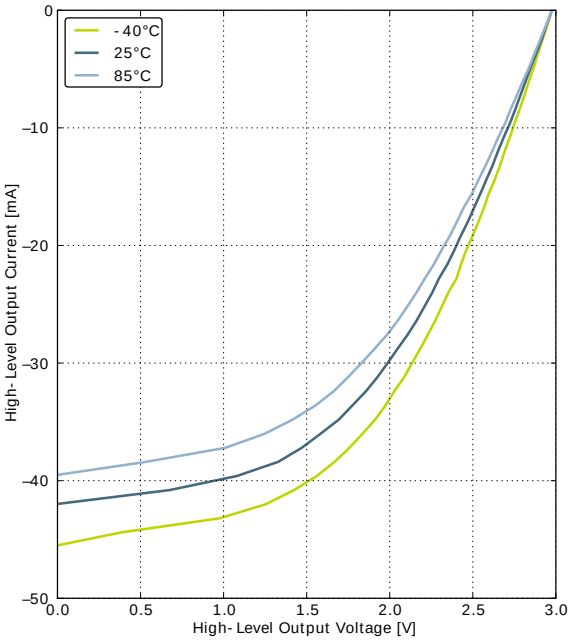
***Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage***



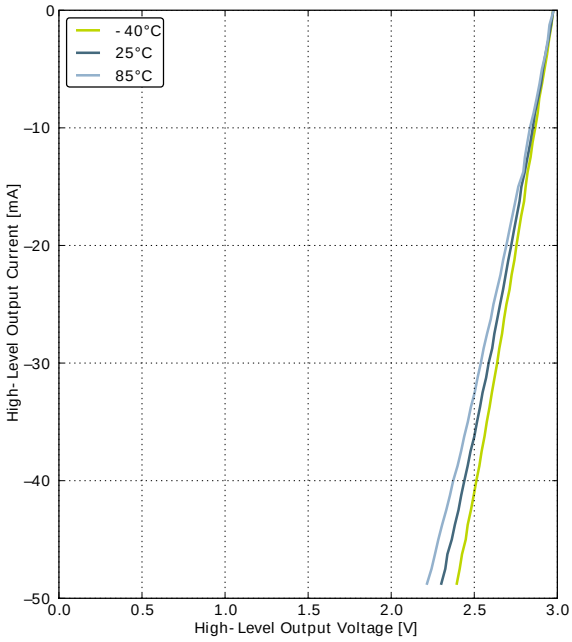

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

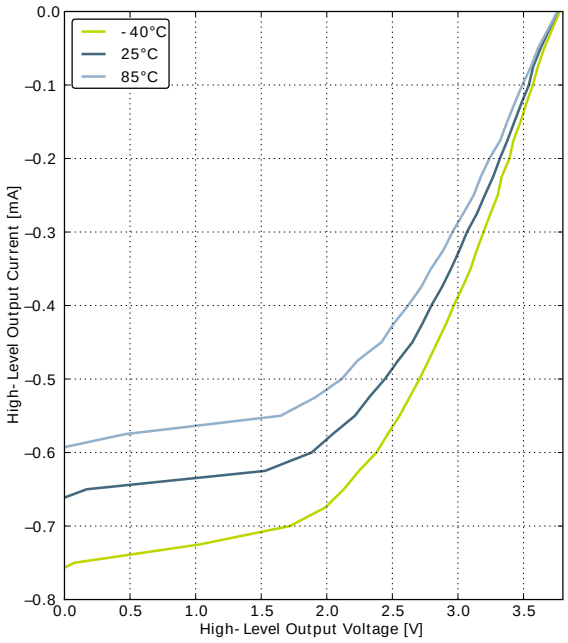



GPIO_Px_CTRL DRIVEMODE = STANDARD

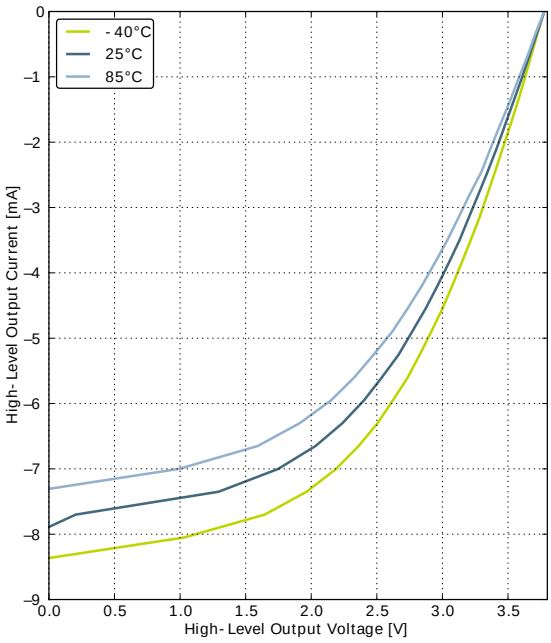



GPIO_Px_CTRL DRIVEMODE = HIGH

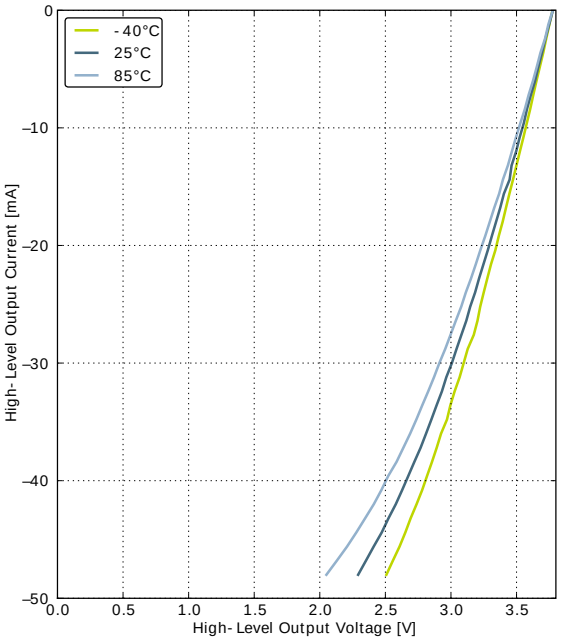
***Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage***



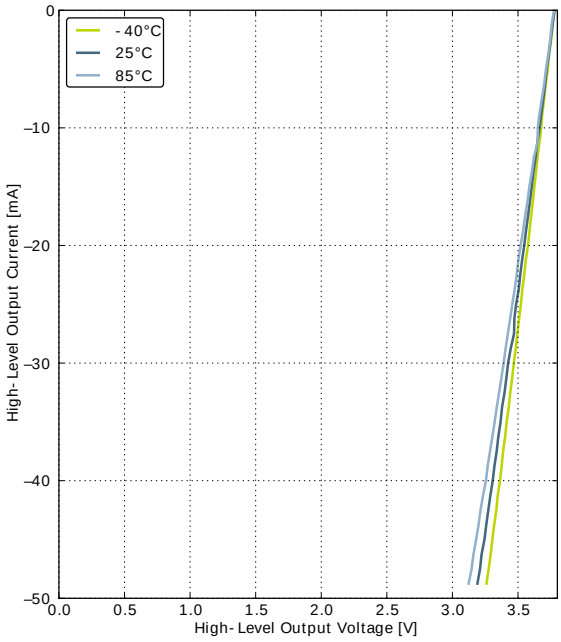

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW




GPIO_Px_CTRL DRIVEMODE = STANDARD




GPIO_Px_CTRL DRIVEMODE = HIGH

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |
| $f_{ADCCLK}$ | ADC Clock Frequency | | | | 13 | MHz |
| $t_{ADCCONV}$ | Conversion time | 6 bit | 7 | | | ADCCLK Cycles |
| | | 8 bit | 11 | | | ADCCLK Cycles |
| | | 12 bit | 13 | | | ADCCLK Cycles |
| $t_{ADCACQ}$ | Acquisition time | Programmable | 1 | | 256 | ADCCLK Cycles |
| $t_{ADCACQVDD3}$ | Required acquisition time for VDD/3 reference | | 2 | | | µs |
| $t_{ADCSTART}$ | Startup time of reference generator and ADC core in NORMAL mode | | | 5 | | µs |
| | Startup time of reference generator and ADC core in KEEPADCWARM mode | | | 1 | | µs |
| $SNR_{ADC}$ | Signal to Noise Ratio (SNR) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 59 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 63 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 65 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 60 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 65 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 54 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 67 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 69 | | dB |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $GAIN_{ED}$ | Gain error drift | 1.25V reference | | 0.01[2] | 0.033[3] | %/°C |
| | | 2.5V reference | | 0.01[2] | 0.03[3] | %/°C |
| $OFFSET_{ED}$ | Offset error drift | 1.25V reference | | 0.2[2] | 0.7[3] | LSB/°C |
| | | 2.5V reference | | 0.2[2] | 0.62[3] | LSB/°C |

[1]On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

[2]Typical numbers given by abs(Mean) / (85 - 25).

[3]Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 32) and Figure 3.18 (p. 33) , respectively.

***Figure 3.17. Integral Non-Linearity (INL)***

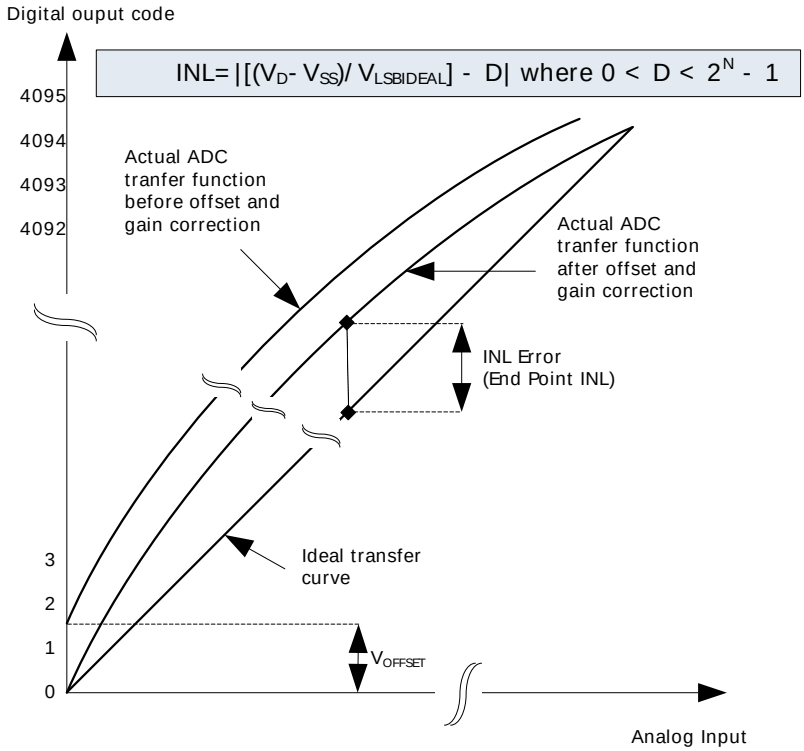
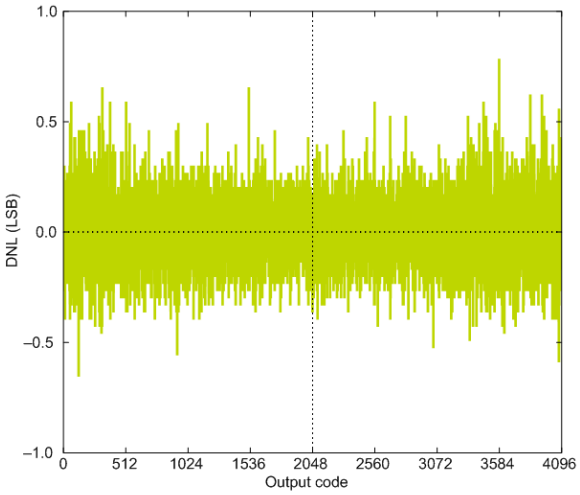
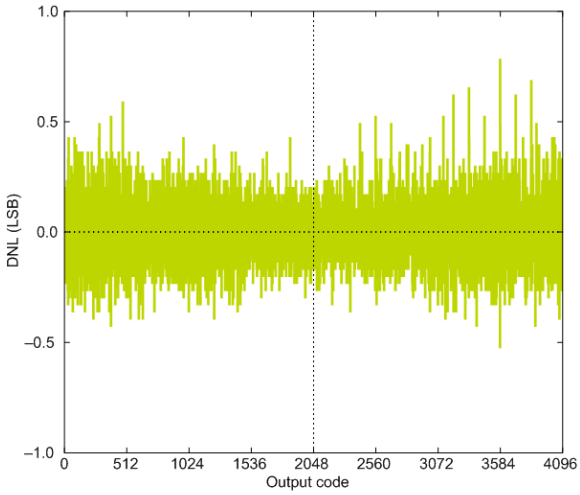


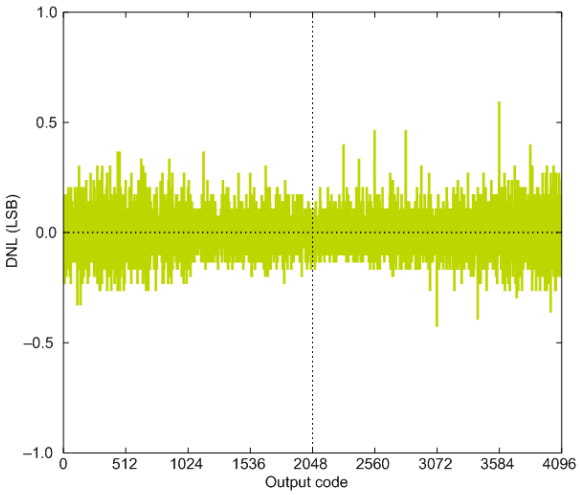
***Figure 3.21. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C***



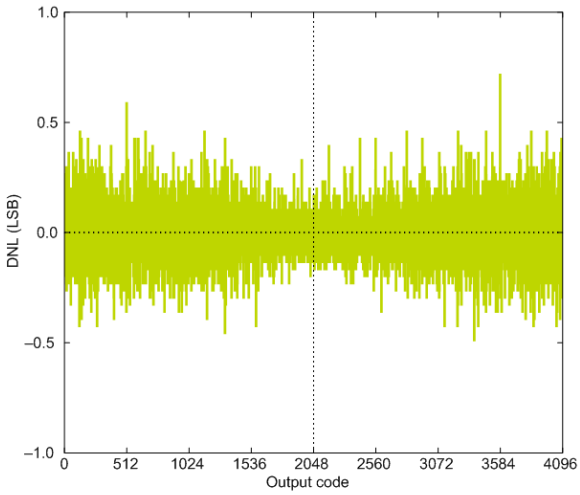

1.25V Reference



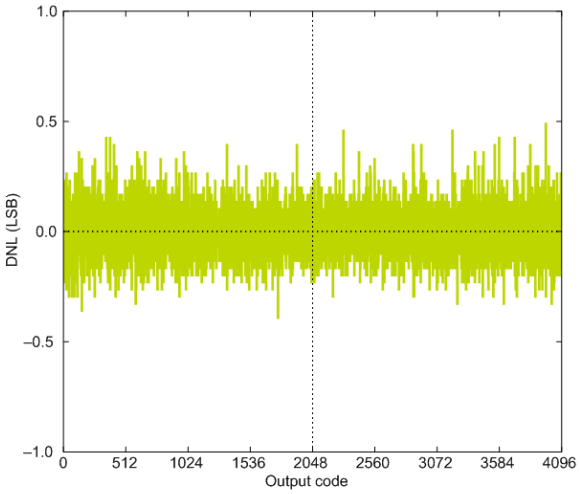

2.5V Reference




2XVDDVSS Reference




5VDIFF Reference




VDD Reference

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 58 | | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 59 | | dB |
| $SNDR_{DAC}$ | Signal to Noise-pulse Distortion Ratio (SNDR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 57 | | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 54 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 56 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 53 | | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 55 | | dB |
| $SFDR_{DAC}$ | Spurious-Free Dynamic Range(SFDR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 62 | | dBc |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 56 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 61 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 55 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 60 | | dBc |
| $V_{DACOFFSET}$ | Offset voltage | After calibration, single ended | | 2 | 12 | mV |
| | | After calibration, differential | | 2 | | mV |
| $DNL_{DAC}$ | Differential non-linearity | | | ±1 | | LSB |
| $INL_{DAC}$ | Integral non-linearity | | | ±5 | | LSB |
| $MC_{DAC}$ | No missing codes | | | 12 | | bits |

[1]Measured with a static input code and no loading on the output.

## 3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

***Table 3.16. OPAMP***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OPAMP}$ | Active Current | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain | | 350 | 405 | µA |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain | | 95 | 115 | µA |

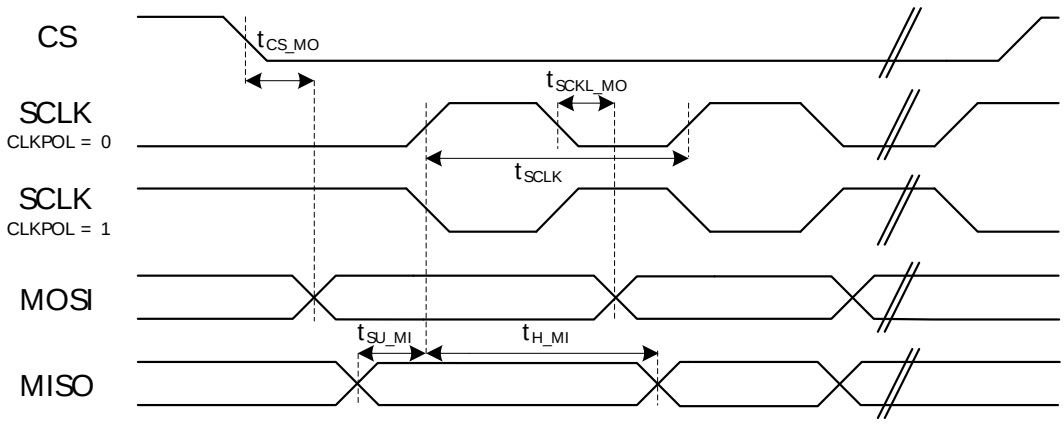
### Table 3.26. I2C Fast-mode Plus (Fm+)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 1000[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 0.5 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.26 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 50 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.26 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.26 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.26 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 0.5 | | | µs |

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32GG Reference Manual.

## 3.17 USART SPI

### Figure 3.36. SPI Master Timing




### Table 3.27. SPI Master Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SCLK}$ [1] [2] | SCLK period | | 2 * $t_{HFPER-CLK}$ | | | ns |
| $t_{CS\_MO}$ [1] [2] | CS to MOSI | | -2.00 | | 1.00 | ns |
| $t_{SCLK\_MO}$ [1] [2] | SCLK to MOSI | | -4.00 | | 3.00 | ns |
| $t_{SU\_MI}$ [1] [2] | MISO setup time | IOVDD = 1.98 V | 36.00 | | | ns |
| | | IOVDD = 3.0 V | 29.00 | | | ns |
| $t_{H\_MI}$ [1] [2] | MISO hold time | | -4.00 | | | ns |

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

*Figure 3.37. SPI Slave Timing*

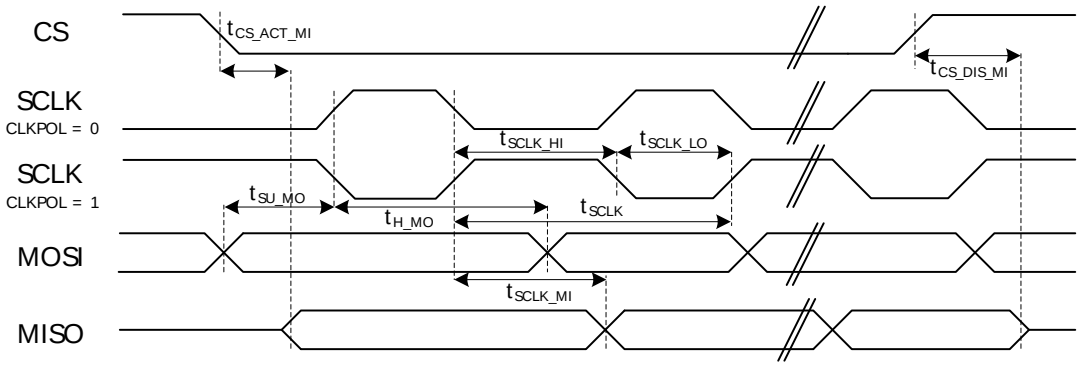



*Table 3.28. SPI Slave Timing*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SCLK\_sl}$ [1] [2] | SCKL period | 2 * $t_{HFPER-CLK}$ | | | ns |
| $t_{SCLK\_hi}$ [1] [2] | SCLK high period | 3 * $t_{HFPER-CLK}$ | | | ns |
| $t_{SCLK\_lo}$ [1] [2] | SCLK low period | 3 * $t_{HFPER-CLK}$ | | | ns |
| $t_{CS\_ACT\_MI}$ [1] [2] | CS active to MISO | 4.00 | | 30.00 | ns |
| $t_{CS\_DIS\_MI}$ [1] [2] | CS disable to MISO | 4.00 | | 30.00 | ns |
| $t_{SU\_MO}$ [1] [2] | MOSI setup time | 4.00 | | | ns |
| $t_{H\_MO}$ [1] [2] | MOSI hold time | 2 + 2* $t_{HF-PERCLK}$ | | | ns |
| $t_{SCLK\_MI}$ [1] [2] | SCLK to MISO | 9 + $t_{HFPER-CLK}$ | | 36 + 2*$t_{HF-PERCLK}$ | ns |

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

# 3.18 USB

The USB hardware in the EFM32GG390 passes all tests for USB 2.0 Full Speed certification. See the test-report distributed with application note "AN0046 - USB Hardware Design Guide".

# 3.19 Digital Peripherals

*Table 3.29. Digital Peripherals*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{USART}$ | USART current | USART idle current, clock enabled | | 4.9 | | µA/MHz |
| $I_{UART}$ | UART current | UART idle current, clock enabled | | 3.4 | | µA/MHz |
| $I_{LEUART}$ | LEUART current | LEUART idle current, clock enabled | | 140 | | nA |
| $I_{I2C}$ | I2C current | I2C idle current, clock enabled | | 6.1 | | µA/MHz |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{TIMER}$ | TIMER current | TIMER_0 idle current, clock enabled | | 6.9 | | µA/MHz |
| $I_{LETIMER}$ | LETIMER current | LETIMER idle current, clock enabled | | 119 | | nA |
| $I_{PCNT}$ | PCNT current | PCNT idle current, clock enabled | | 54 | | nA |
| $I_{RTC}$ | RTC current | RTC idle current, clock enabled | | 54 | | nA |
| $I_{AES}$ | AES current | AES idle current, clock enabled | | 3.2 | | µA/MHz |
| $I_{GPIO}$ | GPIO current | GPIO idle current, clock enabled | | 3.7 | | µA/MHz |
| $I_{EBI}$ | EBI current | EBI idle current, clock enabled | | 11.8 | | µA/MHz |
| $I_{PRS}$ | PRS current | PRS idle current | | 3.5 | | µA/MHz |
| $I_{DMA}$ | DMA current | Clock enable | | 11.0 | | µA/MHz |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| | | OPAMP_OUT0ALT | | | I2C0_SDA #4 | |
| H2 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | | EBI_CSTFT #0/1/2 | | | |
| H5 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| H9 | PD5 | ADC0_CH5<br>OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| H10 | PD6 | ADC0_CH6<br>OPAMP_P1 | | LETIM0_OUT0 #0<br>TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2<br>I2C0_SDA #1 | LES_ALTEX0 #0<br>ACMP0_O #2<br>ETM_TD0 #0 |
| H11 | PD7 | ADC0_CH7<br>OPAMP_N1 | | LETIM0_OUT1 #0<br>TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2<br>I2C0_SCL #1 | CMU_CLK0 #2<br>LES_ALTEX1 #0<br>ACMP1_O #2<br>ETM_TCLK #0 |
| J1 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| J2 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| J3 | PD15 | | | | I2C0_SCL #3 | |
| J4 | PA12 | | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| J5 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| J6 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| J7 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| J8 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| J9 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | USB_DMPU #0<br>US1_CLK #1 | DBG_SWO #3 |
| J10 | PD3 | ADC0_CH3<br>OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| J11 | PD4 | ADC0_CH4<br>OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| K1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| K2 | PC4 | ACMP0_CH4<br>OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4<br>LETIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0<br>I2C1_SDA #0 | LES_CH4 #0 |
| K3 | PA13 | | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| K4 | VSS | Ground. | | | | |
| K5 | PA11 | | EBI_HSNC #0/1/2 | | | |
| K6 | RESETn | Reset input, active low.<br>To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| K7 | AVSS_1 | Analog ground 1. | | | | |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| K8 | AVDD_2 | Analog power supply 2. | | | | |
| K9 | AVDD_1 | Analog power supply 1. | | | | |
| K10 | AVSS_0 | Analog ground 0. | | | | |
| K11 | PD1 | ADC0_CH1<br>DAC0_OUT1ALT #4/<br>OPAMP_OUT1ALT | | TIM0_CC0 #3<br>PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| L2 | PC5 | ACMP0_CH5<br>OPAMP_N0 | EBI_NANDWEn<br>#0/1/2 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0<br>I2C1_SCL #0 | LES_CH5 #0 |
| L3 | PA14 | | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| L4 | IOVDD_1 | Digital IO power supply 1. | | | | |
| L5 | PB11 | DAC0_OUT0 /<br>OPAMP_OUT0 | | LETIM0_OUT0 #1<br>TIM1_CC2 #3 | I2C1_SDA #1 | |
| L6 | PB12 | DAC0_OUT1 /<br>OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| L7 | AVSS_2 | Analog ground 2. | | | | |
| L8 | PB13 | HFXTAL_P | | | US0_CLK #4/5<br>LEU0_TX #1 | |
| L9 | PB14 | HFXTAL_N | | | US0_CS #4/5<br>LEU0_RX #1 | |
| L10 | AVDD_0 | Analog power supply 0. | | | | |
| L11 | PD0 | ADC0_CH0<br>DAC0_OUT0ALT #4/<br>OPAMP_OUT0ALT<br>OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |

## 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 57). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

***Note***

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

***Table 4.2. Alternate functionality overview***

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | | PF8 | | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

## 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32GG390* is shown in Table 4.3 (p. 63). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

***Table 4.3. GPIO Pinout***

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | - | - | - | - | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | - | - | - | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | - | - | PF2 | PF1 | PF0 |

## 4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32GG390* is shown in Figure 4.2 (p. 64) .

*Figure 5.3. BGA112 PCB Stencil Design*

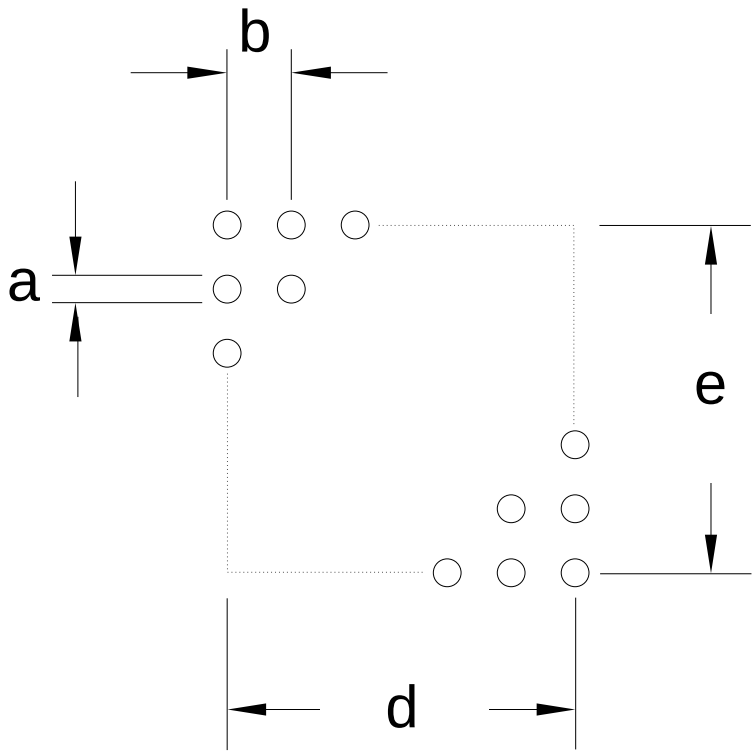



*Table 5.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| a | 0.33 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 64) .

## 5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

# 7 Revision History

## 7.1 Revision 1.40

March 21st, 2016

Added clarification on conditions for $INL_{ADC}$ and $DNL_{ADC}$ parameters.

Reduced maximum and typical current consumption for all EM0 entries except 48 MHz in the Current Consumption table in the Electrical Characteristics section.

Increased maximum specifications for EM2 current, EM3 current, and EM4 current in the Current Consumption table in the Electrical Characteristics section.

Increased typical specification for EM2 and EM3 current at 85 C in the Current Consumption table in the Electrical Characteristics section.

Added EM2, EM3, and EM4 current consumption vs. temperature graphs.

Added a new EM2 entry and specified the existing specification is for EM0 for the BOD threshold on falling external supply voltage in the Power Management table in the Electrical Characteristics section.

Reduced maximum input leakage current in the GPIO table in the Electrical Characteristics section.

Added a maximum current consumption specification to the LFRCO table in the Electrical Characteristics section.

Added maximum specifications for the active current including references for two channels to the DAC table in the Electrical Characteristics section.

Increased the maximum specification for DAC offset voltage in the DAC table in the Electrical Characteristics section.

Increased the typical specifications for active current with FULLBIAS=1 and capacitive sense internal resistance in the ACMP table in the Electrical Characteristics section.

Added minimum and maximum specifications and updated the typical value for the VCMP offset voltage in the VCMP table in the Electrical Characteristics section.

Removed the maximum specification and reduced the typical value for hysteresis in the VCMP table in the Electrical Characteristics section.

Updated all graphs in the Electrical Characteristics section to display data for 2.0 V as the minimum voltage.

## 7.2 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.