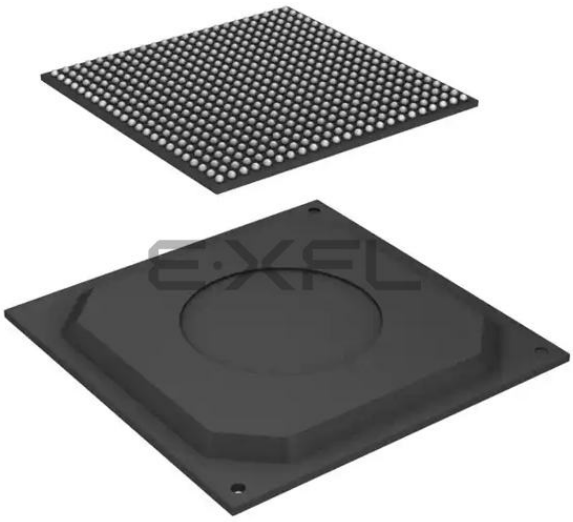

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx535dvv1cr2

- SAHARAv4 Lite—Cryptographic accelerator that includes true random number generator (TRNG)
- Security controller, version 2 (SCCv2)—Improved SCC with AES engine, secure/non-secure RAM and support for multiple keys as well as TZ/non-TZ separation
- Central security unit (CSU)—Enhancement for the IIM (IC Identification Module). CSU is configured during boot by eFUSEs, and determines the security level operation mode as well as the TrustZone (TZ) policy
- Advanced High Assurance Boot (A-HAB)—HAB with the following embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization

Table 3. i.MX53xD Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SPDIF	Sony Philips Digital Interface	Multimedia Peripherals	A standard digital audio transmission protocol developed jointly by the Sony and Philips corporations. Both transmitter and receiver functionalists are supported.
SRTC	Secure Real Time Clock	Security	The SRTC incorporates a special system state retention register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC_POW. The NVCC_SRTC_POW can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR mark the event (security violation indication).
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX53xDA processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously.
Temperature Monitor	(Part of SATA Block)	System Control Peripherals	The temperature sensor is an internal module to the i.MX53xD that monitors the die temperature. The monitor is capable in generating SW interrupt, or trigger the CCM, to reduce the core operating frequency.
TVE	TV Encoder	Multimedia	The TV encoder, version 2.1 is implemented in conjunction with the image processing unit (IPU) allowing handheld devices to display captured still images and video directly on a TV or LCD projector. It supports composite PAL/NTSC, VGA, S-video, and component up to HD1080p analog video outputs.
TZIC	TrustZone Aware Interrupt Controller	ARM/Control	The TrustZone interrupt controller (TZIC) collects interrupt requests from all i.MX53xD sources and routes them to the ARM core. Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UART blocks supports the following serial data transmit/receive protocols and configurations: • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE

4.1.3 Operating Ranges

Table 8 provides the operating ranges of i.MX53xD processor.

Table 8. i.MX53xD Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP[3]	ARM core supply voltage $f_{ARM} \leq 167$ MHz	0.85	0.9	1.4	V
	ARM core supply voltage $f_{ARM} \leq 400$ MHz	0.9	0.95	1.4	V
	ARM core supply voltage $f_{ARM} \leq 800$ MHz	1.05	1.1	1.4	V
	ARM core supply voltage $f_{ARM} \leq 1000$ MHz	1.2	1.25	1.4	V
	ARM core supply voltage $f_{ARM} \leq 1200$ MHz[4]	1.30	1.35	1.4	V
	ARM core supply voltage Stop mode	0.8	0.85	1.4	V
VCC	Peripheral supply voltage[5]	1.25	1.3	1.35	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.35	V
VDDA[6]	Memory arrays voltage	1.25	1.30	1.35	V
	Memory arrays voltage—Stop mode	0.9	0.95	1.35	V
VDDAL1[6]	L1 Cache Memory arrays voltage	1.25	1.30	1.35	V
	L1 Cache Memory arrays voltage—Stop mode	0.9	0.95	1.35	V
VDD_DIG_PLL[7]	PLL Digital supplies—external regulator option	1.25	1.3	1.35	V
VDD_ANA_PLL[8]	PLL Analog supplies—external regulator option	1.75	1.8	1.95	V
NVCC_CKIH	ESD protection of the CKIH pins, FUSE read Supply and 1.8V bias for the UHVIO pads	1.65	1.8	1.95	V
NVCC_LCD NVCC_JTAG	GPIO digital power supplies	1.65	1.8 or 2.775	3.1	V
NVCC_LVDS	LVDS interface Supply	2.375	2.5	2.75	V
NVCC_LVDS_BG	LVDS Band Gap Supply	2.375	2.5	2.75	V
NVCC_EMI_DRAM	DDR Supply DDR2 range	1.7	1.8	1.9	V
	DDR Supply LPDDR2 range	1.14	1.2	1.3	
	DDR Supply LV-DDR2 range	1.47	1.55	1.63	
		1.42	1.5	1.58	
	DDR Supply DDR3 range	1.42	1.5	1.58	
VDD_FUSE[9]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V

Table 20 shows DDR output driver average impedance of the i.MX53 processor.

Table 20. DDR Output Driver Average Impedance[1]

Parameter	Symbol	Test Conditions	Drive strength (DSE)								Unit
			000	001	010	011	100	101	110	111	
Output Driver Impedance	Rdrv[2]	LPDDR1/DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 00 Calibration resistance = 300 Ω[3]	Hi-Z	300	150	100	75	60	50	43	Ω
		DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 01 Calibration resistance = 180 Ω[3]	Hi-Z	180	90	60	45	36	30	26	
		DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 10 Calibration resistance = 200 Ω[3]	Hi-Z	200	100	66	50	40	33	28	
		DDR2 mode NVCC_DRAM= 1.8 V DDR_SEL = 11 Calibration resistance = 140 Ω[3]	Hi-Z	140	70	46	35	28	23	20	
		LPDDR2 mode NVCC_DRAM= 1.2 V DDR_SEL = 01[4] Calibration resistance = 160 Ω[3]	Hi-Z	160	80	53	40	32	27	23	
		LPDDR2 mode NVCC_DRAM = 1.2 V DDR_SEL = 10 Calibration resistance = 240 Ω[3]	Hi-Z	240	120	80	60	48	40	34	
		LPDDR2 mode NVCC_DRAM = 1.2 V DDR_SEL = 11[4] Calibration resistance = 160 Ω[3]	Hi-Z	160	80	53	40	32	27	23	
		DDR3 mode NVCC_DRAM = 1.5 V DDR_SEL = 00 Calibration resistance = 200 Ω[3]	Hi-Z	240	120	80	60	48	48	34	

1 Output driver impedance is controlled across PVTs (process, voltages, and temperatures) using calibration procedure and pu_*cal, pd_*cal input pins.

2 Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

3 Calibration is done against external reference resistor. Value of the resistor should be varied depending on DDR mode and DDR_SEL setting.

4 If DDR_SEL = ‘01’ or DDR_SEL = ‘11’ are selected with NVCC_DRAM = 1.2 V for LPDDR2 operation, the external reference resistor value must be 160 Ω for a correct ZQ calibration. In any case, reference resistors attached to the DDR memory devices should be kept to 240 Ω per the JEDEC standard.

Table 37. NFC—Timing Characteristics

ID	Parameter	Symbol	Asymmetric Mode Min	Symmetric Mode Min	Max
NF1	NFCLE setup Time	t_{CLS}	2T + 0.1	2T + 0.1	—
NF2	NFCLE Hold Time	t_{CLH}	T - 4.45	T - 4.45	—
NF3[1]	NFCE_B Setup Time	t_{CS}	3T + 0.95	3T+0.95	—
NF4	NFCE_B Hold Time	t_{CH}	2T-5.55	1.5T-5.55	—
NF5	NFWE_B Pulse Width	t_{WP}	T - 1.4	0.5T - 1.4	—
NF6	NFALE Setup Time	t_{ALS}	2T + 0.1	2T + 0.1	—
NF7	NFALE Hold Time	t_{ALH}	T - 4.45	T - 4.45	—
NF8	Data Setup Time	t_{DS}	T - 0.9	0.5T - 0.9	—
NF9	Data Hold Time	t_{DH}	T - 5.55	0.5T - 5.55	—
NF10	Write Cycle Time	t_{WC}	2T	T-0.5	—
NF11	NFWE_B Hold Time	t_{WH}	T - 1.15	0.5T - 1.15	—
NF12	Ready to NFRE_B Low	t_{RR}	9T + 8.9	9T + 8.9	—
NF13	NFRE_B Pulse Width	t_{RP}	1.5T	0.5T-1	—
NF14	READ Cycle Time	t_{RC}	2T	T	—
NF15	NFRE_B High Hold Time	t_{REH}	0.5T - 1.15	0.5T - 1.15	—
NF16[2]	Data Setup on READ	t_{DSR}	11.2 + 0.5T - Tdl[3]	11.2 - Tdl[3]	—
NF17[4]	Data Hold on READ	t_{DHR}	0	—	$2T_{aclk}$ + T
NF18[5]	Data Hold on READ	t_{DHR}	—	Tdl[3] - 11.2	$2T_{aclk}$ + T
NF19	CLE to RE delay	t_{CLR}	9T	9T	—
NF20	CE to RE delay	t_{CRE}	T - 3.45	T - 3.45	T + 0.3
NF21	WE high to RE low	t_{WHR}	10.5T	10.5T	—
NF22	WE high to busy	t_{WB}	—	—	6T

1 In case of NUM_OF_DEVICES is greater than 0 (for example, interleaved mode), then only during the data phase of symmetric mode the setup time will equal 1.5T + 0.95.

2 t_{DSR} is calculated by the following formula:

Asymmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} + {}^1/_2T - Tdl$[3]

Symmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} - Tdl$[3]

$t_{REpd} + t_{Dpd}$ = 11.2 ns (including clock skew)

where t_{REpd} is RE propogation delay in the chip including I/O pad delay, and t_{Dpd} is Data propogation delay from I/O pad to EXTMC including I/O pad delay.

t_{DSR} can be used to determine t_{REA} max parameter with the following formula: $t_{REA} = 1.5T - t_{DSR}$.

3 Tdl is composed of 4 delay-line units each generates an equal delay with min 1.25 ns and max 1 aclk period (T_{aclk}). Default is 1/4 aclk period for each delay-line unit, so all 4 delay lines together generates a total of 1 aclk period. T_{aclk} is “emi_slow_clk” of the system, which default value is 7.5 ns (133 MHz).

[4] NF17 is defined only in asymmetric operation mode.
NF17 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

[5] NF18 is defined only in Symmetric operation mode.
t_{DHR} (MIN) is calculated by the following formula: $Tdl^{3} - (t_{REpd} + t_{Dpd})$
where t_{REpd} is RE propogation delay in the chip including I/O pad delay, and t_{Dpd} is Data propogation delay from I/O pad to EXTMC including I/O pad delay.
NF18 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4.6.6 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.6.6.1 EIM Signal Cross Reference

Table 38 is a guide intended to help the user identify signals in the External Interface Module Chapter of the Reference Manual which are identical to those mentioned in this data sheet.

Table 38. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA
ADDR	EIM_A[25:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.6.6.2 EIM Interface Pads Allocation

EIM supports16-bit and 8-bit devices operating in address/data separate or multiplexed modes. In some of the modes the EIM and the NAND FLASH have shared data bus. Table 39 provides EIM interface pads allocation in different modes.

Table 41. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 MHz is supported by SOC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization		—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 Parameters WE4... WE21 value see column BCD = 0 in Table 40.

2 All config. parameters (CSA,CSN,WBEA,WBEN,ADVA,ADVN,OEN,OEA,RBEA & RBEN) are in cycle units.

3 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

4 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

5 t is axi_clk cycle time.

6 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

7 BE Negation. This bit field determines when BE signal is negated during read cycles.

4.6.7 DDR SDRAM Specific Parameters (DDR2/LVDDR2, LPDDR2, and DDR3)

The DDR2/LVDDR2 interface fully complies with JESD79-2E – DDR2 JEDEC release April, 2008, supporting DDR2-800 and LVDDR2-800.

The DDR3 interface fully complies with JESD79-3D – DDR3 JEDEC release April 2008 supporting DDR3-800.

The LPDDR2 interface fully complies with JESD209-2B, supporting LPDDR2-800.

Table 47. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns
CS5	SSx Lead Time (Slave Select setup time)	t_{SCS}	26	—	ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}	26	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	21	ns
CS8	MISO Setup Time	t_{Smiso}	5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	5	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.5, "I/O AC Parameters"

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.2.2 CSPI Slave Mode Timing

Figure 33 depicts the timing of CSPI in slave mode. Timing characteristics were not available at the time of publication.

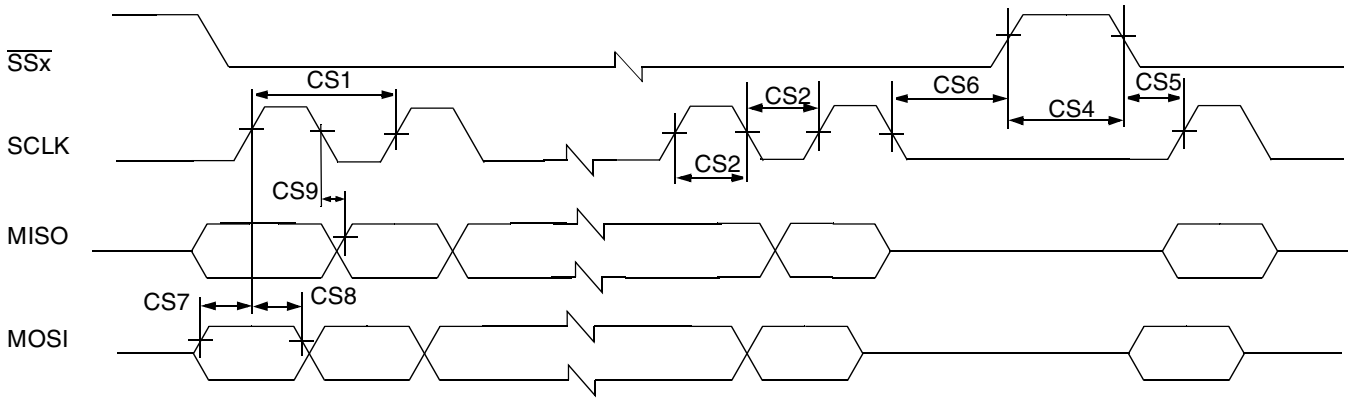

Figure 33. CSPI/ECSPI Slave Mode Timing Diagram

4.7.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 50 shows the interface timing values. The number field in the table refers to timing signals found in Figure 34 and Figure 35.

Table 50. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics[1,2,3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
62	Clock cycle[5]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
64	Clock low period • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[6]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[6]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[6]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns

Figure 66 shows timing for MDMA read, Figure 67 shows timing for MDMA write, and Table 75 lists the timing parameters for MDMA read and write.

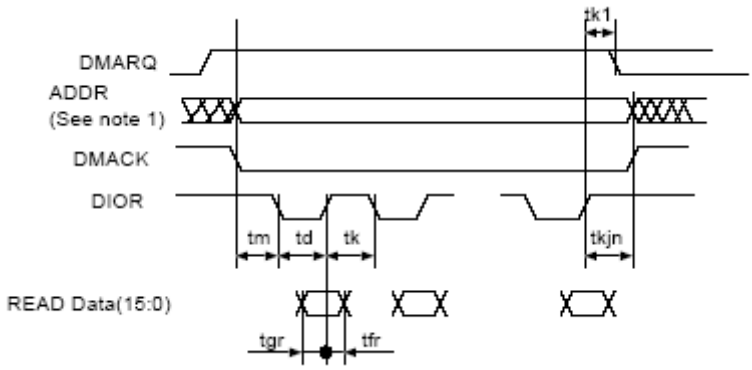

Figure 66. MDMA Read Timing Diagram

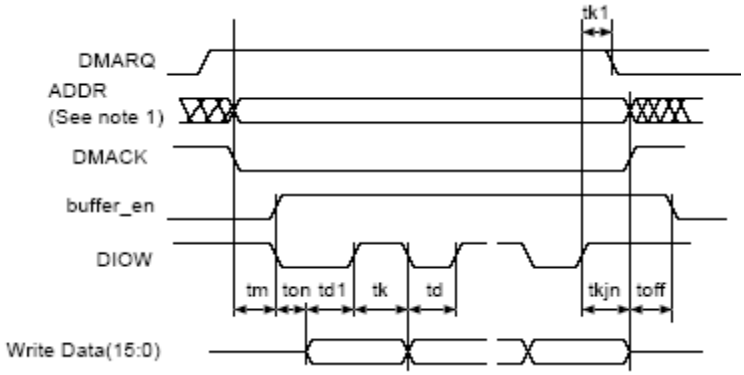

Figure 67. MDMA Write Timing Diagram

Table 75. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 66 (Read), Figure 67 (Write)	Value	Controlling Variable
tm, ti	tm	tm(min) = ti(min) = time_m x T - (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1(min) = td(min) = time_d x T - (tskew1 + tskew2 + tskew6)	time_d
tk	tk[1]	tk(min) = time_k x T - (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0(min) = (time_d + time_k) x T	time_d, time_k
tg(read)	tgr	tgr(min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr(min-drive) = td - te(drive)	time_d
tf(read)	tfr	tfr(min) = 5 ns	—
tg(write)	—	tg(min-write) = time_d x T - (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf(min-write) = time_k x T - (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k - 2)×T - (tsu + tco + 2×tbuf + 2×tcable2)	time_d, time_k[2]

4.7.13 SCAN JTAG Controller (SJC) Timing Parameters

Figure 75 depicts the SJC test clock input timing. Figure 76 depicts the SJC boundary scan timing. Figure 77 depicts the SJC test access port. Signal parameters are listed in Table 81.

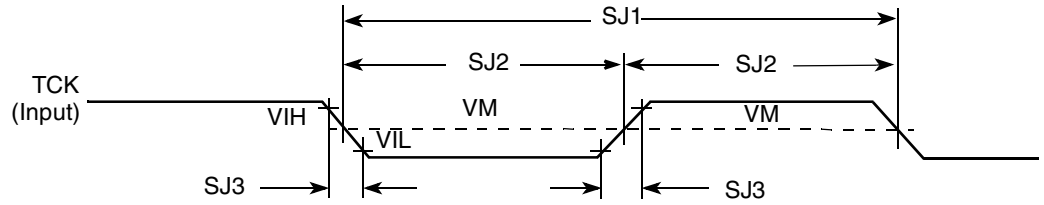

Figure 75. Test Clock Input Timing Diagram

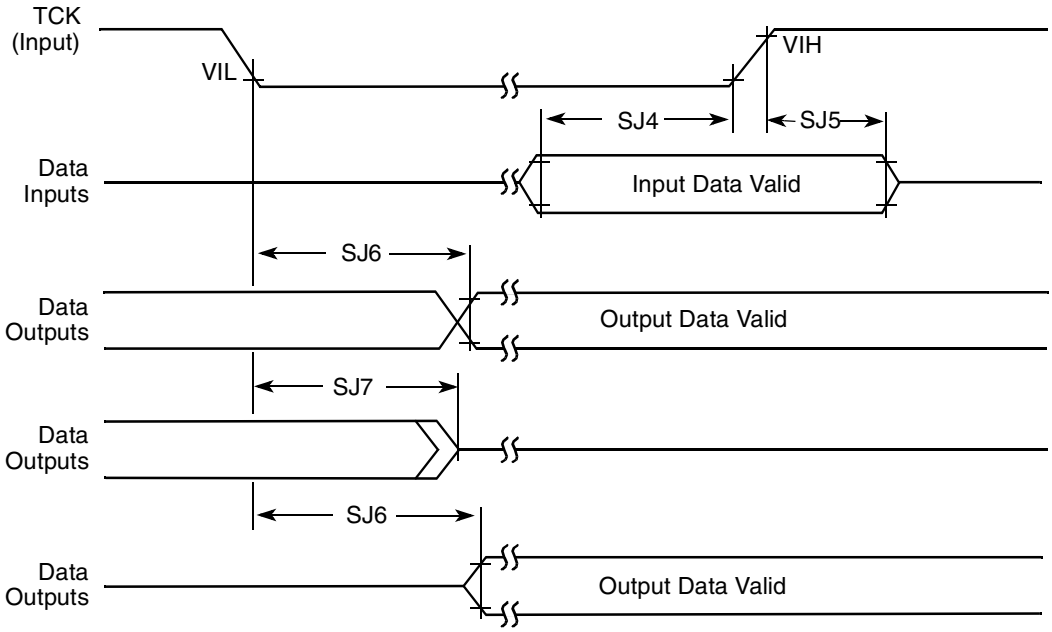

Figure 76. Boundary Scan (JTAG) Timing Diagram

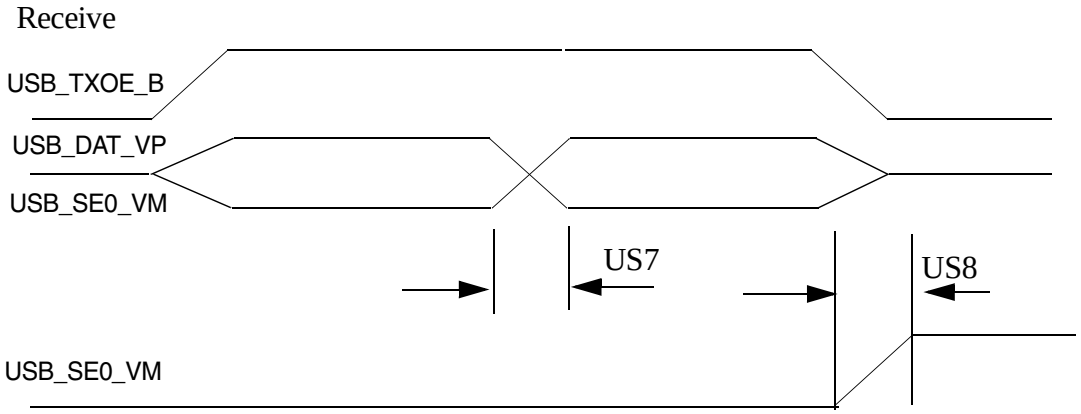

Figure 90. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 94. Definitions of USB Waveform in DAT_SE0 Bi — Directional Mode

No.	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions / Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.7.17.1.2 DAT_SE0 Unidirectional Mode

Table 95. Signal Definitions — DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	TX data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high

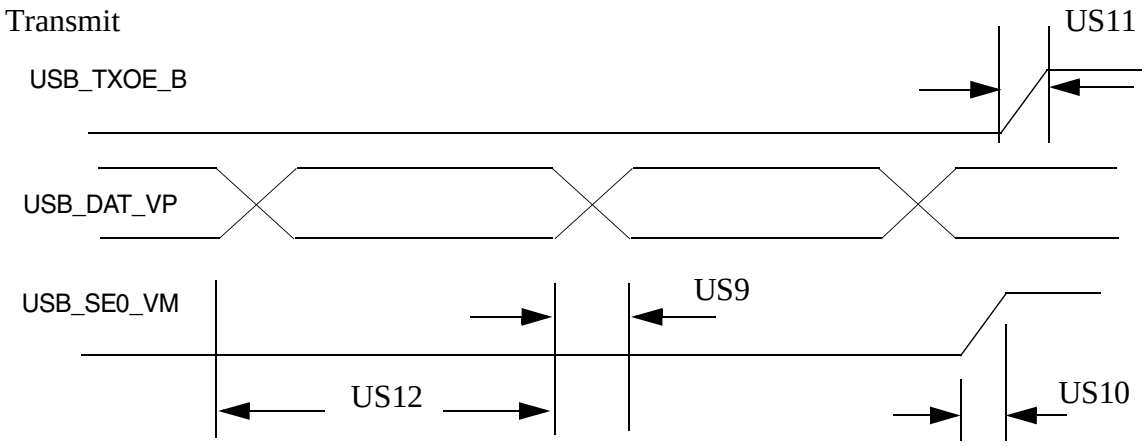

Figure 91. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

Table 113. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
LVDS1_TX0_N	AC14	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[31]	Input	Floating
LVDS1_TX0_P	AB14	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[30]	Input	Floating
LVDS1_TX1_N	AC13	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[29]	Input	Floating
LVDS1_TX1_P	AB13	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[28]	Input	Floating
LVDS1_TX2_N	AC12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[25]	Input	Floating
LVDS1_TX2_P	AB12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[24]	Input	Floating
LVDS1_TX3_N	AA12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[23]	Input	Floating
LVDS1_TX3_P	Y12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[22]	Input	Floating
NANDF_ALE	Y11	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[8]	Input	100 KΩ PU
NANDF_CLE	AA10	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[7]	Input	100 KΩ PU
NANDF_CS0	W12	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[11]	Input	100 KΩ PU
NANDF_CS1	V13	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[14]	Input	100 KΩ PU
NANDF_CS2	V14	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[15]	Input	100 KΩ PU
NANDF_CS3	W13	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[16]	Input	100 KΩ PU
NANDF_RB0	U11	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[10]	Input	100 KΩ PU
NANDF_RE_B	AC8	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-6	gpio6_GPIO[13]	Input	100 KΩ PU
NANDF_WE_B	AB8	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-6	gpio6_GPIO[12]	Input	100 KΩ PU
NANDF_WP_B	AC9	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[9]	Input	100 KΩ PU
PATA_BUFFER_EN	K4	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[1]	Input	100 KΩ PU
PATA_CS_0	L5	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[9]	Input	100 KΩ PU
PATA_CS_1	L2	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[10]	Input	100 KΩ PU
PATA_DA_0	K6	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[6]	Input	100 KΩ PU

Table 113. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
PATA_DIOW	J3	NVCC_PATA	UHVIO	ALT1	GPIO-6	gpio6_GPIO[17]	Input	100 KΩ PU
PATA_DMACK	J2	NVCC_PATA	UHVIO	ALT1	GPIO-6	gpio6_GPIO[18]	Input	100 KΩ PU
PATA_DMARQ	J1	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[0]	Input	100 KΩ PU
PATA_INTRQ	K5	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[2]	Input	100 KΩ PU
PATA_IORDY	K1	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[5]	Input	100 KΩ PU
PATA_RESET_B	K2	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[4]	Input	100 KΩ PU
PMIC_ON_REQ	W14	NVCC_SRTC_POW	GPIO	ALT0	SRTC	srtc_SRTCALARM	Output	—
PMIC_STBY_REQ	W15	NVCC_SRTC_POW	GPIO	ALT0	CCM	ccm_PMIC_VSTBY_REQ	Output	—
POR_B	C19	NVCC_RESET	LVIO	ALT0	SRC	src_POR_B	Input	100 KΩ PU
RESET_IN_B	A21	NVCC_RESET	LVIO	ALT0	SRC	src_RESET_B	Input	100 KΩ PU
SATA_REFCLKM	A14	VPH	ANALOG	—	SATA	SATA_REFCLKM	—	—
SATA_REFCLKP	B14	VPH	ANALOG	—	SATA	SATA_REFCLKP	—	—
SATA_REXT	C13	VPH	ANALOG	—	SATA	SATA_REXT	—	—
SATA_RXM	A12	VPH	ANALOG	—	SATA	SATA_RXM	—	—
SATA_RXP	B12	VPH	ANALOG	—	SATA	SATA_RXP	—	—
SATA_TXM	B10	VPH	ANALOG	—	SATA	SATA_TXM	—	—
SATA_TXP	A10	VPH	ANALOG	—	SATA	SATA_TXP	—	—
SD1_CLK	E16	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[20]	Input	100 KΩ PU
SD1_CMD	F18	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[18]	Input	100 KΩ PU
SD1_DATA0	A20	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[16]	Input	100 KΩ PU
SD1_DATA1	C17	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[17]	Input	100 KΩ PU

Table 114. 19 x 19 mm, 0.8 mm Pitch Ball Map (continued)

N	M	L	K	J	H	G
PATA_DATA6	PATA_DATA1	PATA_DATA0	PATA_IORDY	PATA_DMARQ	DISP0_DAT12	DISP0_DAT6
PATA_DATA8	PATA_DATA3	PATA_CS_1	PATA_RESET_B	PATA_DMACK	DISP0_DAT2	DISP0_DAT4
PATA_DATA9	PATA_DATA4	PATA_DA_1	PATA_DIOR	PATA_DIOW	DISP0_DAT5	DISP0_DAT10
PATA_DATA10	PATA_DATA5	PATA_DA_2	PATA_BUFFER_EN	DISP0_DAT1	DI0_DISP_CLK	DISP0_DAT18
PATA_DATA12	PATA_DATA7	PATA_CS_0	PATA_INTRQ	DISP0_DAT0	DISP0_DAT11	DISP0_DAT19
PATA_DATA13	PATA_DATA11	PATA_DATA2	PATA_DA_0	NVCC_LCD	DISP0_DAT7	DISP0_DAT8
NVCC_PATA	VDDA	GND	VDDGP	NVCC_LCD	VDDGP	GND
VCC	GND	VDDGP	GND	VDDGP	GND	VDDGP
GND	VCC	GND	VDDGP	GND	VDDGP	NVCC_JTAG
VCC	GND	VDDGP	GND	VDDGP	GND	VDDGP
GND	VCC	GND	VDDGP	GND	VDDGP	VDDGP
VCC	GND	VDDGP	GND	VDDGP	GND	VDDA
GND	VCC	GND	VCC	GND	VCC	USB_H1_VDDA33
VCC	GND	VCC	GND	VCC	NVCC_SD2	USB_OTG_VDDA33
GND	VCC	GND	VCC	GND	NVCC_SD1	VDD_FUSE
VCC	GND	VCC	GND	VCC	NVCC_RESET	VDD_ANA_PLL
NVCC_EMI_DRAM	VDDA	DDR_VREF	NVCC_EMI_DRAM	GND	VDD_DIG_PLL	NVCC_CKIH
DRAM_A14	DRAM_A15	DRAM_CAS	DRAM_CS0	DRAM_SDODT0	NVCC_EMI_DRAM	VDD_REG
DRAM_SDBA2	DRAM_A0	DRAM_SDWE	DRAM_A10	DRAM_RAS	DRAM_SDCKE0	GND
DRAM_A3	DRAM_A2	DRAM_A12	DRAM_A4	GND	DRAM_D0	DRAM_D3
DRAM_A5	DRAM_A9	DRAM_A1	GND	DRAM_D2	DRAM_DQM0	DRAM_D1
DRAM_A7	DRAM_A6	DRAM_A11	DRAM_SDCLK_0_B	DRAM_D6	DRAM_SDQS0_B	DRAM_D7
DRAM_A8	DRAM_CALIBRATION	DRAM_A13	DRAM_SDCLK_0	DRAM_D4	DRAM_SDQS0	DRAM_D5
N	M	L	K	J	H	G

Table 119. 12 x 12 mm PoP Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment (Top)	Contact Assignment (Bottom)	Power Rail	I/O Buffer Type	Out of Reset Condition[1]			
					Alt. Mode	Function	Direction	Config. Value
DRAM_CS0	AB3	AB23	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_CS[0]	Output	High
DRAM_CS1	AB4	J24	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_CS[1]	Output	High
DRAM_D0	W22	T29	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[0]	Output	High
DRAM_D1	AA23	V27	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[1]	Output	High
DRAM_D10	AC13	AG22	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[10]	Output	High
DRAM_D11	AC17	AG29	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[11]	Output	High
DRAM_D12	AB14	AG23	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[12]	Output	High
DRAM_D13	AB15	AF29	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[13]	Output	High
DRAM_D14	AB12	AG28	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[14]	Output	High
DRAM_D15	AC16	AJ27	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[15]	Output	High
DRAM_D16	C22	D29	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[16]	Output	High
DRAM_D17	E23	E29	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[17]	Output	High
DRAM_D18	D23	D28	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[18]	Output	High
DRAM_D19	G23	F28	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[19]	Output	High
DRAM_D2	U22	R29	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[2]	Output	High
DRAM_D20	F22	F27	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[20]	Output	High
DRAM_D21	H22	G27	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[21]	Output	High
DRAM_D22	E22	E28	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[22]	Output	High
DRAM_D23	H23	F29	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[23]	Output	High
DRAM_D24	A17	F21	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[24]	Output	High
DRAM_D25	A14	C19	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[25]	Output	High
DRAM_D26	B17	G21	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[26]	Output	High
DRAM_D27	A13	G18	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[27]	Output	High
DRAM_D28	B15	G20	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[28]	Output	High
DRAM_D29	B12	F17	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[29]	Output	High
DRAM_D3	Y22	U27	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[3]	Output	High
DRAM_D30	A16	F20	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[30]	Output	High
DRAM_D31	B14	G19	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[31]	Output	High
DRAM_D4	T23	R27	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[4]	Output	High
DRAM_D5	V23	R28	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_D[5]	Output	High

Table 119. 12 x 12 mm PoP Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment (Top)	Contact Assignment (Bottom)	Power Rail	I/O Buffer Type	Out of Reset Condition[1]			
					Alt. Mode	Function	Direction	Config. Value
TVDAC_COMP	—	A25	TVDAC_AHVDDRGB	ANALOG	—	TVDAC_COMP	—	—
TVDAC_IOB	—	A23	TVDAC_AHVDDRGB	ANALOG	—	TVDAC_IOB	—	—
TVDAC_IOG	—	B24	TVDAC_AHVDDRGB	ANALOG	—	TVDAC_IOG	—	—
TVDAC_IOR	—	C29	TVDAC_AHVDDRGB	ANALOG	—	TVDAC_IOR	—	—
USB_H1_DN	—	AH21	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB_H1_DN	—	—
USB_H1_DP	—	AJ21	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB_H1_DP	—	—
USB_H1_GPANAIO	—	AJ20	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	USB_H1_GPANAIO	—	—
USB_H1_RREFEXT	—	AH20	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	USB_H1_RREFEXT	—	—
USB_H1_VBUS	—	AJ22	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB_H1_VBUS	—	—
USB_OTG_DN	—	AJ23	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB_OTG_DN	—	—
USB_OTG_DP	—	AH23	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB_OTG_DP	—	—
USB_OTG_GPANAIO	—	AH24	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB_OTG_GPANAIO	—	—
USB_OTG_ID	—	AH22	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB_OTG_ID	—	—
USB_OTG_RREFEXT	—	AJ24	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB_OTG_RREFEXT	—	—

Table 120. PoP 12 × 12 mm, 0.4 mm Pitch Top Ball Map (continued)

	AC
1	NC
2	NC
3	DRAM_SDCKE0
4	DRAM_SDCKE1
5	GND
6	DRAM_A0
7	DRAM_A2
8	POP_VDDCA
9	GND
10	POP_VDDMM
11	POP_VACC
12	GND
13	DRAM_D10
14	DRAM_D8
15	GND
16	DRAM_D15
17	DRAM_D11
18	GND
19	DRAM_SDQS1_B
20	POP_VDD1
21	GND
22	NC
23	NC
	AC

Table 121. PoP 12 × 12 mm, 0.4 mm Pitch Bottom Ball Map

	F	E	D	C	B	A	
1	EIM_D23	EIM_D25	EIM_D26	EIM_D30	GND	GND	1
2	EIM_DA13	EIM_DA12	EIM_D28	EIM_A22	GND	GND	2
3	EIM_DA5	EIM_DA4	POP_VDD2	POP_VDD1	EIM_A23	EIM_A25	3
4	NC	NC	NC	EIM_CS1	PATA_RESET_B	EIM_A24	4
5	NC	NC	NC	PATA_DATA3	PATA_IORDY	EIM_LBA	5
6	EIM_EB3	NC	NC	EIM_A21	PATA_DATA2	EIM_A19	6
7	EIM_D31	NC	NC	EIM_D29	EIM_A20	EIM_A16	7
8	EIM_A18	NC	NC	POP_VCCMM	PATA_DATA1	EIM_DA3	8
9	EIM_D24	NC	NC	PATA_DATA11	PATA_DATA0	EIM_OE	9
10	EIM_DA2	NC	NC	EIM_D27	PATA_DATA10	EIM_DA8	10
11	EIM_BCLK	NC	NC	POP_VCCQMM	PATA_DATA9	NANDF_CS1	11
12	PMIC_ON_REQ	NC	NC	NANDF_CS2	PATA_DATA8	NANDF_CS3	12
13	NVCC_SRTC_POW	NC	NC	POP_VDD1	LVDS1_TX3_P	LVDS1_TX3_N	13
14	NVCC_XTAL	NC	NC	POP_VDD2	LVDS1_TX2_P	LVDS1_TX2_N	14
15	XTAL	NC	NC	NANDF_RB0	LVDS1_CLK_P	LVDS1_CLK_N	15
16	VDDA	NC	NC	POP_VDDQ	LVDS1_TX1_P	LVDS1_TX1_N	16
17	DRAM_D29	NC	NC	GND	LVDS1_TX0_N	LVDS1_TX0_P	17
18	NVCC_LVDS_BG	NC	NC	LVDS_BG_RES	LVDS0_TX3_N	LVDS0_TX3_P	18
19	NVCC_LVDS	NC	NC	DRAM_D25	LVDS0_CLK_N	LVDS0_CLK_P	19
20	DRAM_D30	NC	NC	POP_VDDQ	LVDS0_TX2_N	LVDS0_TX2_P	20
21	DRAM_D24	NC	NC	DRAM_SDQS3_B	LVDS0_TX1_P	LVDS0_TX1_N	21
22	DRAM_SDCKE1	NC	NC	DRAM_SDQS3	LVDS0_TX0_N	LVDS0_TX0_P	22
23	TVDAC_DHVDD	NC	NC	DRAM_DQM3	TVCDC_IOB_BACK	TVDAC_IOB	23
24	NVCC_EMI_DRAM	NC	NC	POP_VDDQ	TVDAC_IOG	TVCDC_IOG_BACK	24
25	NC	NC	NC	GPIO_13	GPIO_10	TVDAC_COMP	25
26	NC	NC	NC	POP_VDD1	GPIO_11	GPIO_12	26
27	DRAM_D20	POP_VDDQ	DRAM_A15	POP_VDD2	GPIO_14	TVDAC_VREF	27
28	DRAM_D19	DRAM_D22	DRAM_D18	TVCDC_IOR_BACK	GND	GND	28
29	DRAM_D23	DRAM_D17	DRAM_D16	TVDAC_IOR	GND	GND	29
	F	E	D	C	B	A	

7 Revision History

Table 122 provides a revision history for this data sheet.

Table 122. i.MX53xD Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 6	03/2013	In Table 2, “Ordering Information” removed MCIMX535DVV2C, as it no longer exists. In Table 8, “i.MX53xD Operating Ranges,” updated minimum values of LVDS interface supply (NVCC_LVDS) and LVDS band gap supply (NVCC_LVDS_BG) to 2.375 volts.
Rev. 5	09/2012	• In Table 2, "Ordering Information," on page 4,” renamed “Features” column as “CPU Frequency.” • Added Table 1, "i.MX53 Parts Functional Differences," on page 3. • In Section 1.2, “Features,” changed “SATA I” to “SATA II” under Hard disk drives bullet. • Removed the note shown at the end of Section 1.2, “Features.” • Removed mention of FlexCAN feature from the entire document. • Removed mention of IEEE1588 standard from the entire document. • In Table 3, "i.MX53xD Digital and Analog Blocks," on page 9, removed details of MPEG2 encoder, as this is not supported on i.MX53. • In Table 8, "i.MX53xD Operating Ranges," on page 21: —Changed VDDGP max voltage, for all frequency ranges and for STOP mode, to 1.4 V —Updated footnote on TVDAC_DHVDD and TVDAC_AHVDDRGB • In Table 10, "Maximal Supply Currents," on page 24: —Corrected power line name, MVCC_XTAL, to NVCC_XTAL —Added a footnote on NVCC_EMI_DRAM —Updated max current value and added a footnote for power line, NVCC_SRTC_POW —Removed duplicate entries for NVCC_EMI_DRAM and NVCC_XTAL • In Section 4.2.3, “Power Supplies Usage,” updated the fourth bullet item. • In Figure 25, "Asynchronous A/D Muxed Write Access," on page 61, renamed “WE41” as “WE41A” and shifted its position to left. • In Table 59, "Camera Input Signal Cross Reference, Format and Bits Per Cycle," on page 83, added a footnote on “YCbCr 8 bits 2 cycles” column header.
Rev. 4.1	02/2012	• In Table 2, "Ordering Information," on page 4, changed the part number PCIMX538DZK1C to SCIMX538DZK1C.
Rev. 4	11/2011	• In Section 1, “Introduction,” changed 1 GHz to 1.2 GHz in the second paragraph and updated the bulleted list after the second paragraph. • In Table 2, "Ordering Information," on page 4: —Removed part numbers “PCIMX535DVV1C” and “MCIMX538DZK1C” —Added a new part number “MCIMX535DVV2C” —Updated package information for part number “PCIMX538DZK1C” —Updated the second footnote • In Section 1.2, “Features,” changed “Target frequency” to “Maximum frequency” and 1 GHz to 1–1.2 GHz in the third bullet item of the first bulleted list. • In Table 3, "i.MX53xD Digital and Analog Blocks," on page 9, removed “Sorenson H.263 decode, 4CIF resolution, 8 Mbps bit rate” from VPU brief description. • In Table 5, "Absolute Maximum Ratings," on page 18, changed the maximum voltage for VDDGP from 1.35V to 1.4V. • In Table 8, "i.MX53xD Operating Ranges," on page 21: —Added a row and a footnote for “ARM core supply voltage $f_{ARM} \leq$ 1200 MHz” parameter of VDDGP —Added a new footnote for “Peripheral supply voltage” parameter of VCC —Updated the footnote for “Junction temperature” parameter (continued on next page)