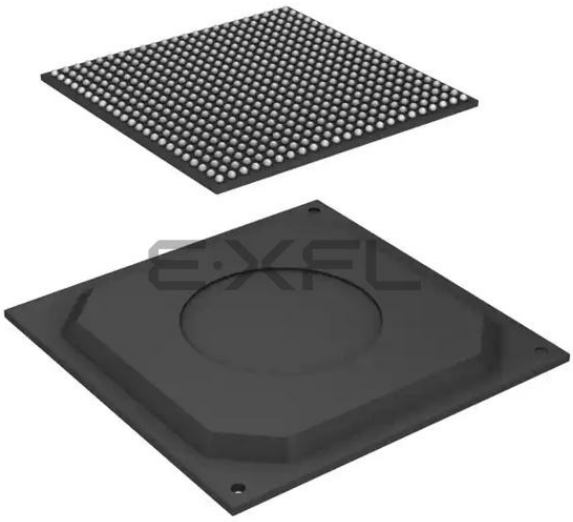

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx535dvv2c

3 Modules List

The i.MX53xD processor contains a variety of digital and analog modules. Table 3 describes these modules in alphabetical order.

Table 3. i.MX53xD Digital and Analog Blocks

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM	ARM Platform	ARM	The ARM Cortex™ A8 platform consists of the ARM processor version r2p5 (with TrustZone) and its essential sub-blocks. It contains the 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, Level 2 cache controller and a 256 Kbyte L2 cache. The platform also contains an event monitor and debug modules. It also has a NEON coprocessor with SIMD media processing architecture, a register file with 32/64-bit general-purpose registers, an integer execute pipeline (ALU, Shift, MAC), dual single-precision floating point execute pipelines (FADD, FMUL), a load/store and permute pipeline and a non-pipelined vector floating point (VFP Lite) coprocessor supporting VFPv3.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The asynchronous sample rate converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Multiplexer	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports (three internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CAMP-1 CAMP-2	Clock Amplifier	Clocks, Resets, and Power Control	Clock amplifier
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, as well as for system power management. The system includes four PLLs.
CSPI ECSPI-1 ECSPI-2	Configurable SPI, Enhanced CSPI	Connectivity Peripherals	Full-duplex enhanced synchronous serial interface, with data rates 16-60 Mbit/s. It is configurable to support master/slave modes. In Master mode it supports four slave selects for multiple peripherals.
CSU	Central Security Unit	Security	The central security unit (CSU) is responsible for setting comprehensive security policy within the i.MX53xD platform, and for sharing security information between the various security modules. The security control registers (SCR) of the CSU are set during boot time by the high assurance boot (HAB) code and are locked to prevent further writing.

Table 3. i.MX53xD Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
USB	USB Controller	Connectivity Peripherals	USB supports USB2.0 480 MHz, and contains: • One high-speed OTG sub-block with integrated HS USB PHY • One high-speed host sub-block with integrated HS USB PHY • Two identical high-speed Host modules The high-speed OTG module, which is internally connected to the HS USB PHY, is equipped with transceiver-less logic to enable on-board USB connectivity without USB transceivers All the USB ports are equipped with standard digital interfaces (ULPI, HS IC-USB) and transceiver-less logic to enable onboard USB connectivity without USB transceivers.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU) version 3, which covers many SD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing such as rotation and mirroring. VPU Features: • MPEG-2 decode, Mail-High profile, up to 1080i/p resolution, 40 Mbps bit rate • MPEG4/XviD decode, SP/ASP profile, up to 1080 i/p resolution, 40 Mbps bit rate • H.263 decode, P0/P3 profile, up to 16CIF resolution, 20 Mbps bit rate • H.264 decode, BP/MP/HP profile, up to 1080 i/p resolution, 40 Mbps bit rate • VC1 decode, SP/MP/AP profile, up to 1080 i/p resolution, 40 Mbps bit rate • RV10 decode, 8/9/2010 profile, up to 1080 i/p resolution, 40 Mbps bit rate • DivX decode, 3/4/5/6 profile, up to 1080 i/p resolution, 40 Mbps bit rate • MJPEG decode, Baseline profile, up to 8192 x 8192 resolution, 40 Mpixel/s bit rate for 4:4:4 format • MPEG4 encode, Simple profile, up to 720p resolution, 12 Mbps bit rate[1] • H.263 encode, P0/P3 profile, up to 4CIF resolution, 8 Mbps bit rate[1] • H.264 encode, Baseline profile, up to 720p resolution, 14 Mbps bit rate[1] • MJPEG encode, Baseline profile, up to 8192 x 8192 resolution, 80 Mpixel/s bit rate for 4:2:2 format
WDOG-1	Watch Dog	Timer Peripherals	The watch dog timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. This situation should be avoided, as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.

- I/O Supplies (NVCC_xxx) below or equal to 2.8 V nom./3.1 V max. should not precede NVCC_CKIH. They can start powering ON during NVCC_CKIH ramp-up, before it is stabilized. Within this group, the supplies can be powered-up in any order.
  Alternatively, the on-chip regulator VDD_ANA_PLL can be used to power NVCC_CKIH and NVCC_RESET. In this case, the sequence defined in the “Interfacing the i.MX53 Processor with LTC3589-1” section of the *i.MX53 System Development User's Guide* (MX53UG) must be followed.
- I/O Supplies (NVCC_xxx) above 2.8 V nom./3.1 V max. should be powered ON only after NVCC_CKIH is stable.
- In case VDD_DIG_PLL and VDD_ANA_PLL are powered ON from internal voltage regulator (default case for i.MX53xD), there are no related restrictions on VDD_REG, as it is used as their internal regulators power source.
  If VDD_DIG_PLL and VDD_ANA_PLL are powered on externally, to reduce current leakage during the power-up, it is recommended to activate the VDD_REG before or at the same time with VDD_DIG_PLL and VDD_ANA_PLL. If this sequencing is not possible, make sure that the 2.5 V VDD_REG supply shut-off output impedance is higher than 1 kΩ when it is inactive.
- VDD_REG supply is required to be powered ON to enable DDR operation. It must be powered on after VCC and before NVCC_EMI_DRAM. The sequence should be:

  VCC $\rightarrow$VDD_REG $\rightarrow$NVCC_EMI_DRAM
- NVCC_EIM_DRAM_2P5 PoP additional power line timing is the same as DVV_REG
- VDDA and VDDAL1 can be powered ON anytime before POR_B, regardless of any other power signal.
- VDDGP can be powered ON anytime before POR_B, regardless of any other power signal.
- VP and VPH can be powered up together, or anytime after, the VCC. VP and VPH should come before POR.
- TVDAC_DHVDD and TVDAC_AHVDDRGB should be powered from the same regulator. This is due to ESD diode protection circuit, that may cause current leakage if one of the supplies is powered ON before the other.

NOTE

The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4 The typical value of Vox(ac) is expected to be about 0.5 x OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

Table 25 shows the AC parameters for LPDDR2 I/O operating in LPDDR2 mode.

Table 25. LPDDR2 I/O LPDDR2 mode AC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to OVDD/2	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	266 MHz	—	—	0.6	V-ns
Single output slew rate	tsr	50 Ω to Vref. 5pF load. Drive impedance= 40 Ω ± 30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5 pF load. Drive impedance= 60 Ω ± 30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 266 MHz clk = 400 MHz	—	—	0.2 0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 26 shows the AC parameters for LPDDR2 I/O operating in DDR3 mode.

Table 26. LPDDR2 I/O DDR3 mode AC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	—	Vref - 0.15	—	Vref + 0.15	V
Output AC differential cross point voltage[4]	Vox(ac)	—	Vref - 0.15	—	Vref + 0.15	V

Table 40. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE3	BCLK High Level Width	0.4 x t		0.8 x t		1.2 x t		1.6 x t	
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to BEy_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to BEy_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to ADV_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to ADV_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—

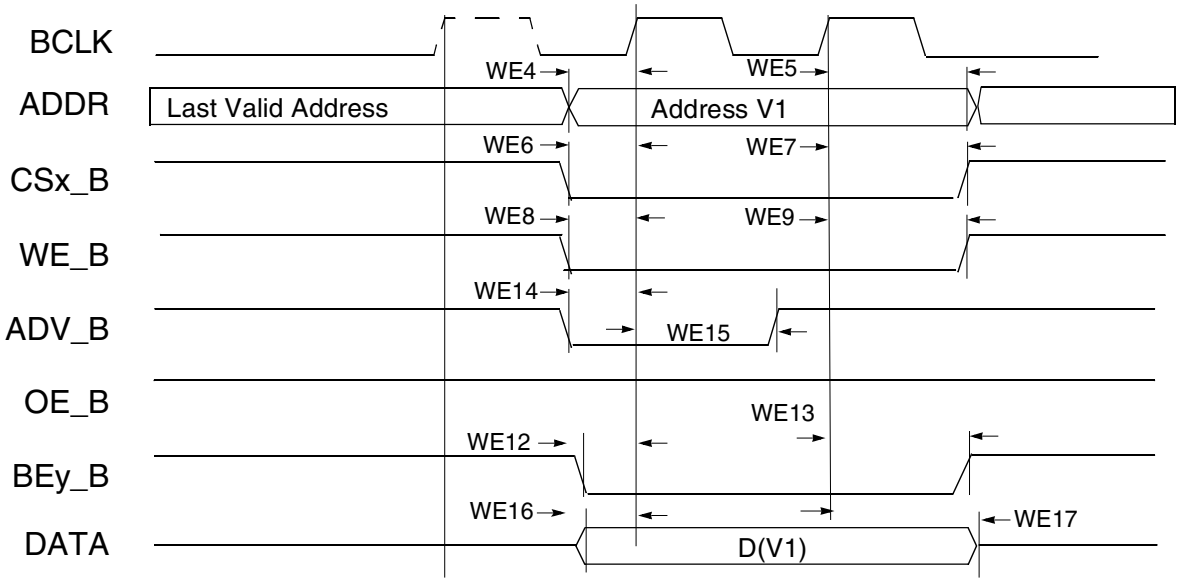

Figure 19. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

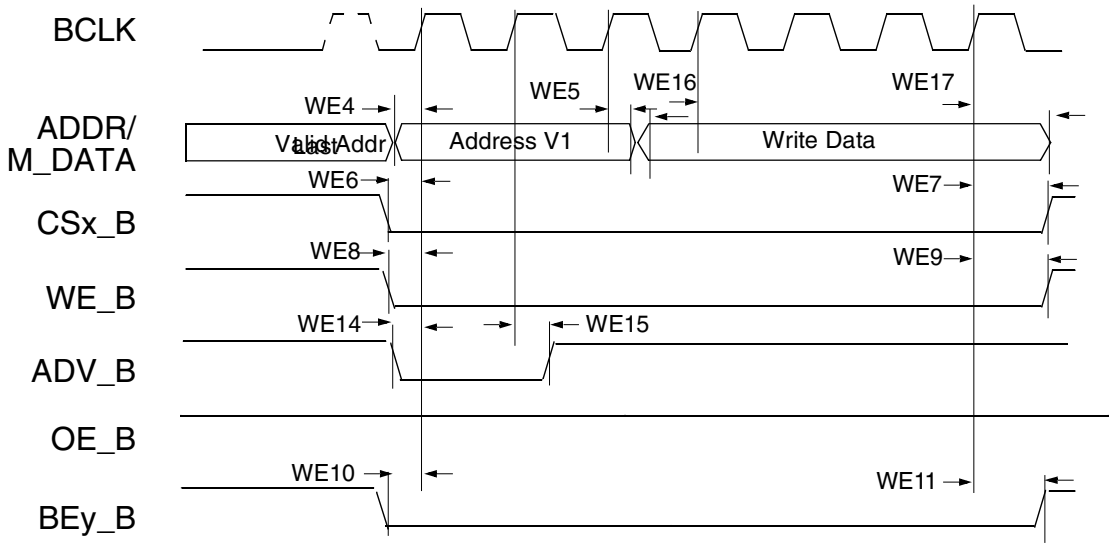

Figure 20. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

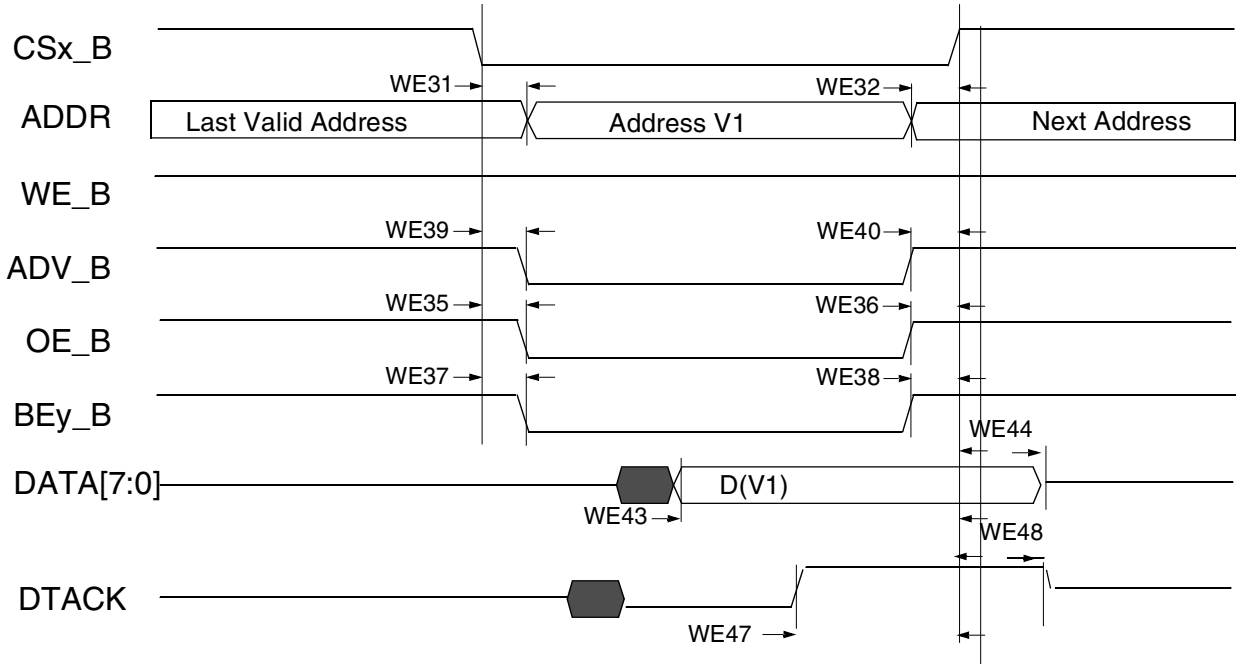

Figure 26. DTACK Read Access (DAP=0)

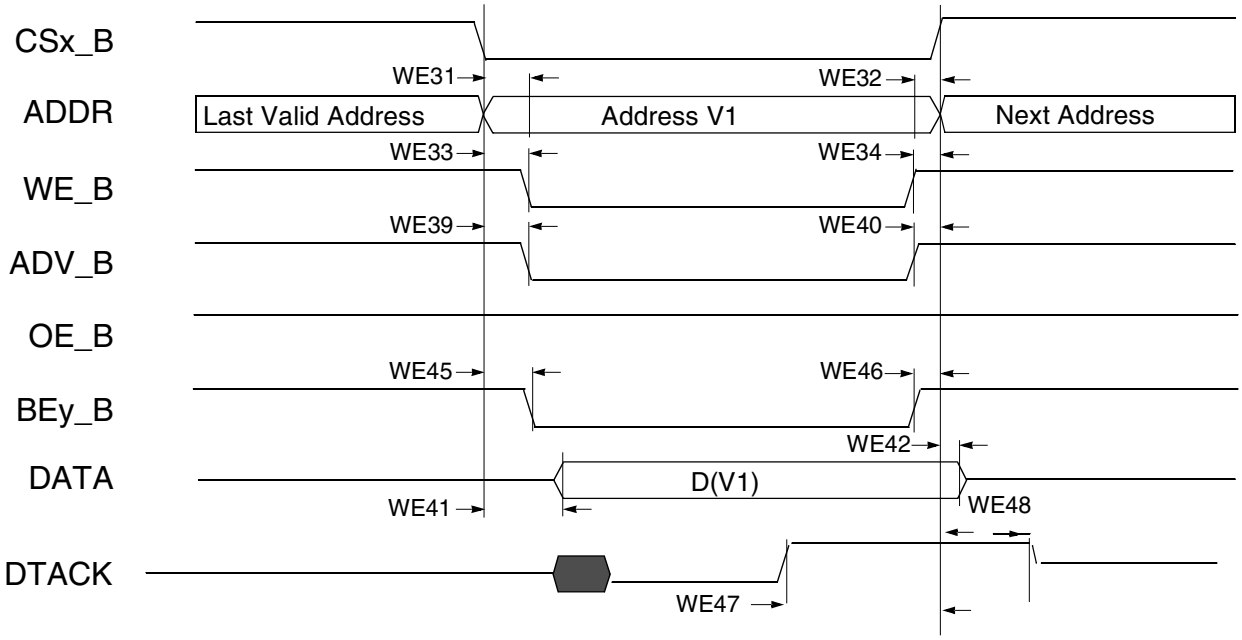

Figure 27. DTACK Write Access (DAP=0)

Figure 28 and Table 42 show the address and control timing parameters for DDR2 and DDR3.

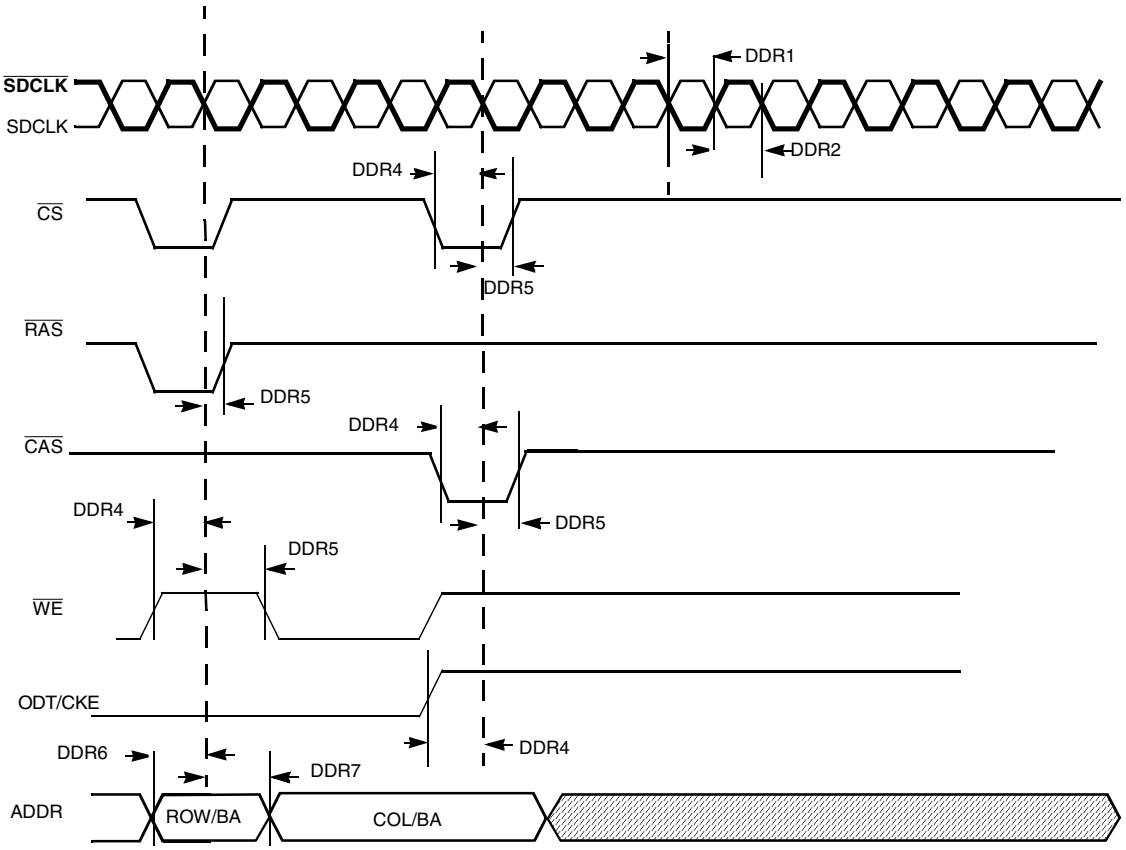

Figure 28. DDR SDRAM Address and Control Parameters for DDR2 and DDR3

Table 42. DDR SDRAM Timing Parameter Table[1] [2]

ID	Parameter	Symbol	SDCLK = 400 MHz		Units
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.48	0.52	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.48	0.52	t_{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}	0.6	—	ns
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}	0.6	—	ns
DDR6	Address output setup time	t_{IS}	0.6	—	ns
DDR7	Address output hold time	t_{IH}	0.6	—	ns

1 All timings are refer to Vref level cross point.

2 Reference load model is 25 Ω resistor from each of the DDR outputs to VDD_REF.

Table 58. I²C Module Timing Parameters

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.7.7 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.7.7.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 59 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

valid and cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

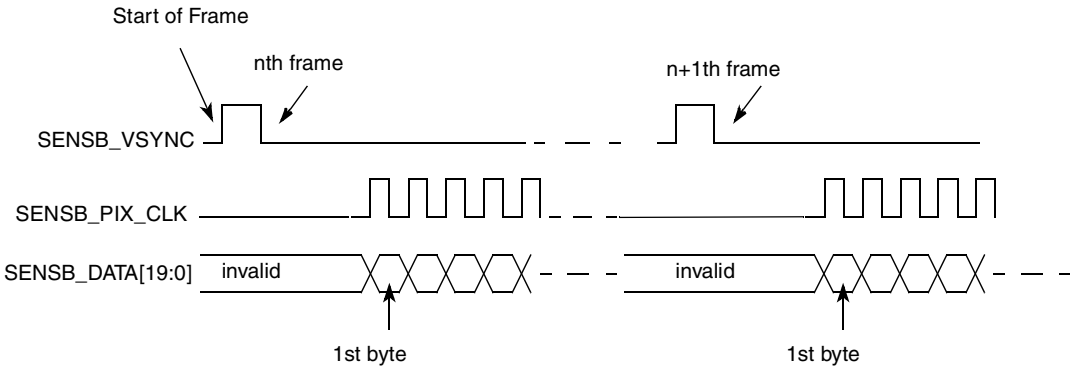

Figure 45. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 45 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.7.7.3 Electrical Characteristics

Figure 46 depicts the sensor interface timing. SENSB_MCLK signal described here is not generated by the IPU. Table 60 lists the sensor interface timing characteristics.

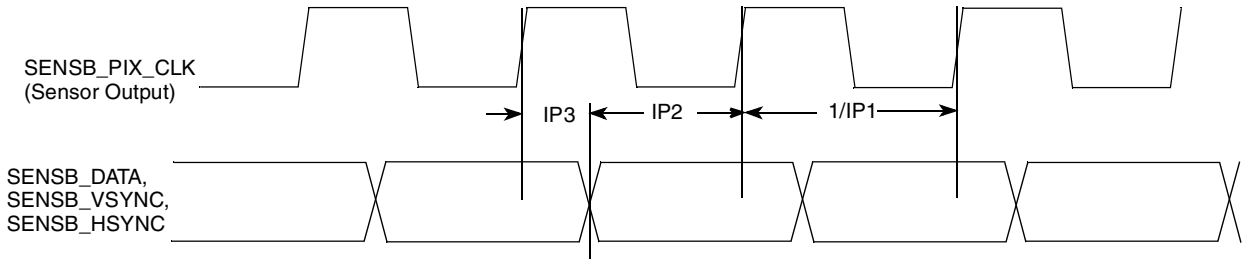

Figure 46. Sensor Interface Timing Diagram

Table 60. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.7.7.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.7.7.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.7.7.6.2 LCD Interface Functional Description

Figure 47 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock, used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

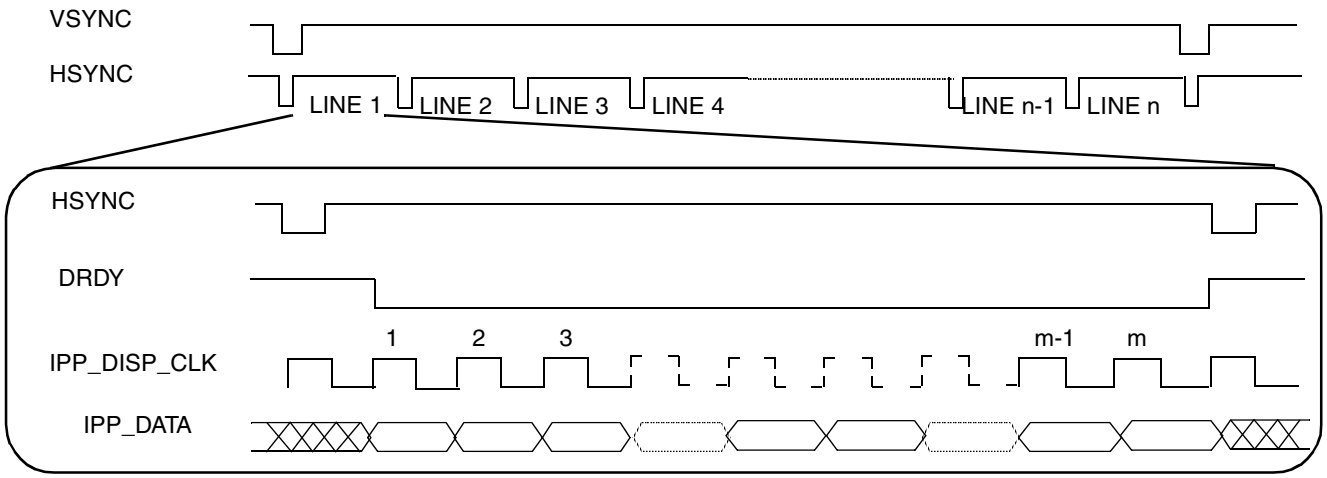

Figure 47. Interface Timing Diagram for TFT (Active Matrix) Panels

Figure 59 depicts Write 0 Sequence timing, and Table 68 lists the timing parameters.

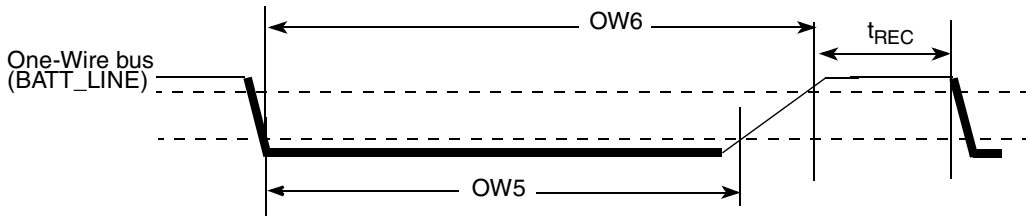

Figure 59. Write 0 Sequence Timing Diagram

Table 68. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW5	Write 0 Low Time	t_{LOW0}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs
	Recovery time	t_{REC}	1	—	—	µs

Figure 60 depicts Write 1 Sequence timing, Figure 61 depicts the Read Sequence timing, and Table 69 lists the timing parameters.

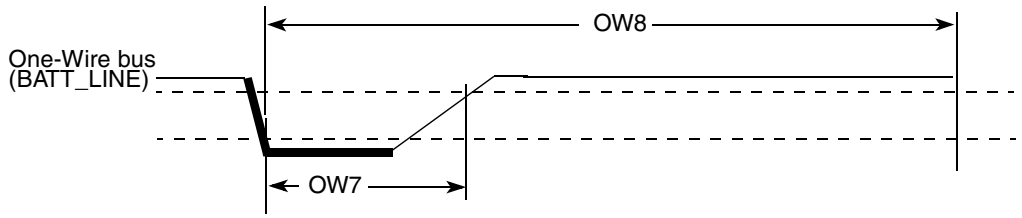

Figure 60. Write 1 Sequence Timing Diagram

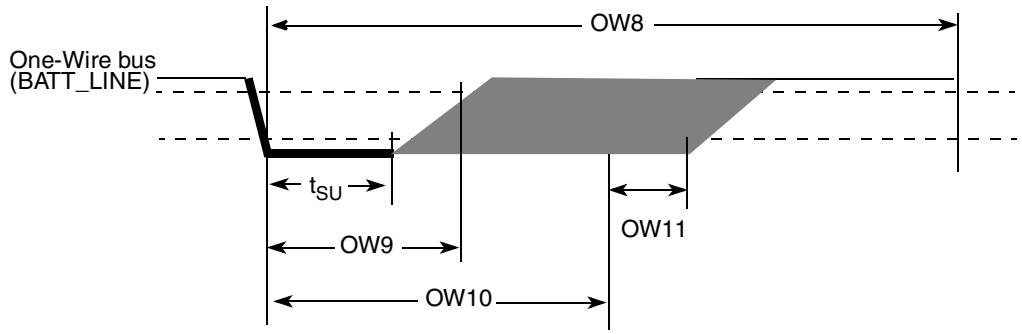

Figure 61. Read Sequence Timing Diagram

4.7.11 PATA Timing Parameters

This section describes the timing parameters of the Parallel ATA module which are compliant with ATA/ATAPI-6 specification.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100MB/s. Parallel ATA module interface consist of a total of 29 pins. Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-6 specification and these requirements are configurable by the ATA module registers.

Table 71 and Figure 63 define the AC characteristics of all the PATA interface signals in all data transfer modes.

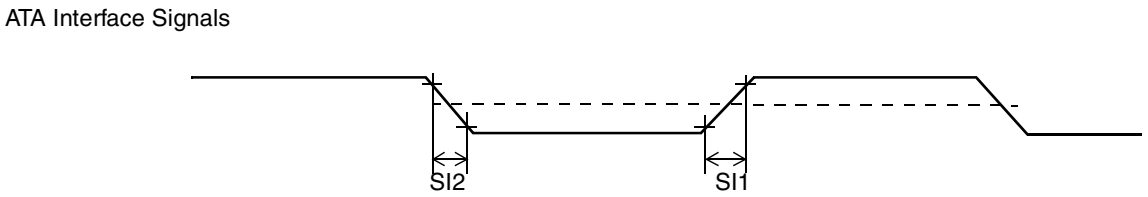

Figure 63. PATA Interface Signals Timing Diagram

Table 71. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min	Max	Unit
SI1	Rising edge slew rate for any signal on ATA interface[1]	S_{rise}	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on ATA interface[1]	S_{fall}	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL shall meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15–40 pF where all signals have the same capacitive load value.

The user must use level shifters for 5.0 V compatibility on the ATA interface. The i.MX53xD PATA interface is 3.3 V compatible.

The use of bus buffers introduces delay on the bus and skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

Table 86. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

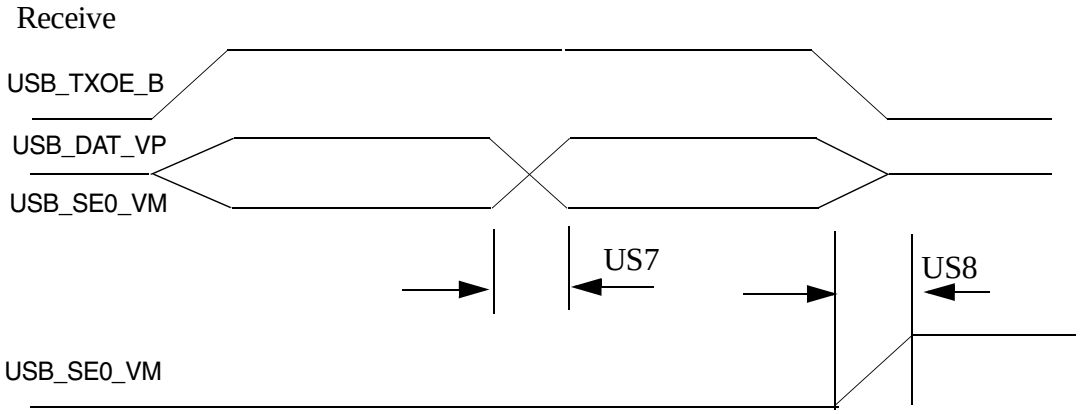

Figure 90. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 94. Definitions of USB Waveform in DAT_SE0 Bi — Directional Mode

No.	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions / Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

Table 113. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
CSI0_DAT10	R5	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[28]	Input	100 KΩ PU
CSI0_DAT11	T2	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[29]	Input	100 KΩ PU
CSI0_DAT12	T3	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[30]	Input	360 KΩ PD
CSI0_DAT13	T6	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[31]	Input	360 KΩ PD
CSI0_DAT14	U1	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[0]	Input	360 KΩ PD
CSI0_DAT15	U2	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[1]	Input	360 KΩ PD
CSI0_DAT16	T4	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[2]	Input	360 KΩ PD
CSI0_DAT17	T5	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[3]	Input	360 KΩ PD
CSI0_DAT18	U3	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[4]	Input	360 KΩ PD
CSI0_DAT19	U4	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[5]	Input	360 KΩ PD
CSI0_DAT4	R1	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[22]	Input	100 KΩ PU
CSI0_DAT5	R2	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[23]	Input	360 KΩ PD
CSI0_DAT6	R6	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[24]	Input	100 KΩ PU
CSI0_DAT7	R3	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[25]	Input	100 KΩ PU
CSI0_DAT8	T1	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[26]	Input	100 KΩ PU
CSI0_DAT9	R4	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[27]	Input	360 KΩ PD
CSI0_DATA_EN	P3	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[20]	Input	100 KΩ PU
CSI0_MCLK	P2	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[19]	Input	100 KΩ PU
CSI0_PIXCLK	P1	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[18]	Input	100 KΩ PU

Table 119. 12 x 12 mm PoP Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment (Top)	Contact Assignment (Bottom)	Power Rail	I/O Buffer Type	Out of Reset Condition[1]			
					Alt. Mode	Function	Direction	Config. Value
DI0_PIN3	—	AC7	NVCC_LCD	GPIO	ALT1	gpio4_GPIO[19]	Input	100 KΩ PU
DI0_PIN4	—	AC6	NVCC_LCD	GPIO	ALT1	gpio4_GPIO[20]	Input	100 KΩ PU
DISP0_DAT 0	—	AD1	NVCC_LCD	GPIO	ALT1	gpio4_GPIO[21]	Input	100 KΩ PD
DISP0_DAT 1	—	AC3	NVCC_LCD	GPIO	ALT1	gpio4_GPIO[22]	Input	100 KΩ PD
DISP0_DAT 10	—	AG2	NVCC_LCD	GPIO	ALT1	gpio4_GPIO[31]	Input	100 KΩ PU
DISP0_DAT 11	—	AE3	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[5]	Input	100 KΩ PD
DISP0_DAT 12	—	AC1	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[6]	Input	100 KΩ PU
DISP0_DAT 13	—	AH3	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[7]	Input	100 KΩ PU
DISP0_DAT 14	—	AG3	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[8]	Input	100 KΩ PU
DISP0_DAT 15	—	AH4	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[9]	Input	100 KΩ PU
DISP0_DAT 16	—	AG5	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[10]	Input	100 KΩ PU
DISP0_DAT 17	—	AB6	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[11]	Input	100 KΩ PU
DISP0_DAT 18	—	AJ4	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[12]	Input	100 KΩ PU
DISP0_DAT 19	—	AA7	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[13]	Input	100 KΩ PU
DISP0_DAT 2	—	AC2	NVCC_LCD	GPIO	ALT1	gpio4_GPIO[23]	Input	100 KΩ PD
DISP0_DAT 20	—	AJ5	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[14]	Input	100 KΩ PU
DISP0_DAT 21	—	AB7	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[15]	Input	100 KΩ PU
DISP0_DAT 22	—	AH5	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[16]	Input	100 KΩ PU
DISP0_DAT 23	—	AJ6	NVCC_LCD	GPIO	ALT1	gpio5_GPIO[17]	Input	100 KΩ PU

Table 120. PoP 12 × 12 mm, 0.4 mm Pitch Top Ball Map (continued)

	AC
1	NC
2	NC
3	DRAM_SDCKE0
4	DRAM_SDCKE1
5	GND
6	DRAM_A0
7	DRAM_A2
8	POP_VDDCA
9	GND
10	POP_VDDMM
11	POP_VACC
12	GND
13	DRAM_D10
14	DRAM_D8
15	GND
16	DRAM_D15
17	DRAM_D11
18	GND
19	DRAM_SDQS1_B
20	POP_VDD1
21	GND
22	NC
23	NC
	AC

Table 121. PoP 12 × 12 mm, 0.4 mm Pitch Bottom Ball Map

	F	E	D	C	B	A	
1	EIM_D23	EIM_D25	EIM_D26	EIM_D30	GND	GND	1
2	EIM_DA13	EIM_DA12	EIM_D28	EIM_A22	GND	GND	2
3	EIM_DA5	EIM_DA4	POP_VDD2	POP_VDD1	EIM_A23	EIM_A25	3
4	NC	NC	NC	EIM_CS1	PATA_RESET_B	EIM_A24	4
5	NC	NC	NC	PATA_DATA3	PATA_IORDY	EIM_LBA	5
6	EIM_EB3	NC	NC	EIM_A21	PATA_DATA2	EIM_A19	6
7	EIM_D31	NC	NC	EIM_D29	EIM_A20	EIM_A16	7
8	EIM_A18	NC	NC	POP_VCCMM	PATA_DATA1	EIM_DA3	8
9	EIM_D24	NC	NC	PATA_DATA11	PATA_DATA0	EIM_OE	9
10	EIM_DA2	NC	NC	EIM_D27	PATA_DATA10	EIM_DA8	10
11	EIM_BCLK	NC	NC	POP_VCCQMM	PATA_DATA9	NANDF_CS1	11
12	PMIC_ON_REQ	NC	NC	NANDF_CS2	PATA_DATA8	NANDF_CS3	12
13	NVCC_SRTC_POW	NC	NC	POP_VDD1	LVDS1_TX3_P	LVDS1_TX3_N	13
14	NVCC_XTAL	NC	NC	POP_VDD2	LVDS1_TX2_P	LVDS1_TX2_N	14
15	XTAL	NC	NC	NANDF_RB0	LVDS1_CLK_P	LVDS1_CLK_N	15
16	VDDA	NC	NC	POP_VDDQ	LVDS1_TX1_P	LVDS1_TX1_N	16
17	DRAM_D29	NC	NC	GND	LVDS1_TX0_N	LVDS1_TX0_P	17
18	NVCC_LVDS_BG	NC	NC	LVDS_BG_RES	LVDS0_TX3_N	LVDS0_TX3_P	18
19	NVCC_LVDS	NC	NC	DRAM_D25	LVDS0_CLK_N	LVDS0_CLK_P	19
20	DRAM_D30	NC	NC	POP_VDDQ	LVDS0_TX2_N	LVDS0_TX2_P	20
21	DRAM_D24	NC	NC	DRAM_SDQS3_B	LVDS0_TX1_P	LVDS0_TX1_N	21
22	DRAM_SDCKE1	NC	NC	DRAM_SDQS3	LVDS0_TX0_N	LVDS0_TX0_P	22
23	TVDAC_DHVDD	NC	NC	DRAM_DQM3	TVCDC_IOB_BACK	TVDAC_IOB	23
24	NVCC_EMI_DRAM	NC	NC	POP_VDDQ	TVDAC_IOG	TVCDC_IOG_BACK	24
25	NC	NC	NC	GPIO_13	GPIO_10	TVDAC_COMP	25
26	NC	NC	NC	POP_VDD1	GPIO_11	GPIO_12	26
27	DRAM_D20	POP_VDDQ	DRAM_A15	POP_VDD2	GPIO_14	TVDAC_VREF	27
28	DRAM_D19	DRAM_D22	DRAM_D18	TVCDC_IOR_BACK	GND	GND	28
29	DRAM_D23	DRAM_D17	DRAM_D16	TVDAC_IOR	GND	GND	29
	F	E	D	C	B	A	

Table 121. PoP 12 × 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

	AJ	AH
1	GND	GND
2	GND	SVDDGP
3	DISP0_DAT9	DISP0_DAT13
4	DISP0_DAT18	DISP0_DAT15
5	DISP0_DAT20	DISP0_DAT22
6	DISP0_DAT23	DI0_PIN15
7	KEY_ROW2	KEY_COL4
8	KEY_COL3	KEY_ROW1
9	KEY_COL1	KEY_ROW0
10	GPIO_19	GPIO_16
11	GPIO_5	GPIO_4
12	GPIO_6	GPIO_1
13	VPH	VPH
14	SATA_TXP	SATA_TXM
15	GND	GND
16	SATA_RXP	SATA_RXM
17	SATA_REXT	SD2_DATA0
18	SATA_REFCLKM	SATA_REFCLKP
19	VP	VP
20	USB_H1_GPANAIO	USB_H1_RREFEXT
21	USB_H1_DP	USB_H1_DN
22	USB_H1_VBUS	USB_OTG_ID
23	USB_OTG_DN	USB_OTG_DP
24	USB_OTG_RREFEXT	USB_OTG_GPANAIO
25	SD1_DATA3	SD1_DATA2
26	SD1_CLK	SD1_CMD
27	DRAM_D15	SD1_DATA0
28	GND	SVCC
29	GND	GND
	AJ	AH

Table 122. i.MX53xD Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)

Rev. 1	03/2011	• Updated the first sentence of Section 3.1, “Special Signal Considerations.”
		• Deleted two tables, “Special Signal Considerations” and “JTAG Controller Interface Summary,” in Section 3.1, “Special Signal Considerations.”
		• Updated Table 8, "i.MX53xD Operating Ranges," on page 21.
		  • Changed VDDGP voltages as follows:
		  — 400 MHz from 1.35 to 1.05 V maximum.
		  — 800 MHz from 1.0/1.05/1.1 to 1.05/1.1/1.15 V minimum/nominal/maximum.
		  — Stop mode from 0.9/0.95/1.1 to 0.8/0.85/1.3 V minimum/nominal/maximum.
		  • Added statements to footnotes 5 and 6.
		  • Added footnote on voltage ramping.
		• In Section 1, “Introduction,” the second bullet item changed from “Smartbooks” to “Smart mobile devices.”
		• In Table 2, "Ordering Information," on page 4, added two new rows for part numbers PCIMX535DVV1C and MCIMX535DVV1C.

Rev. 0	02/2011	Initial release.