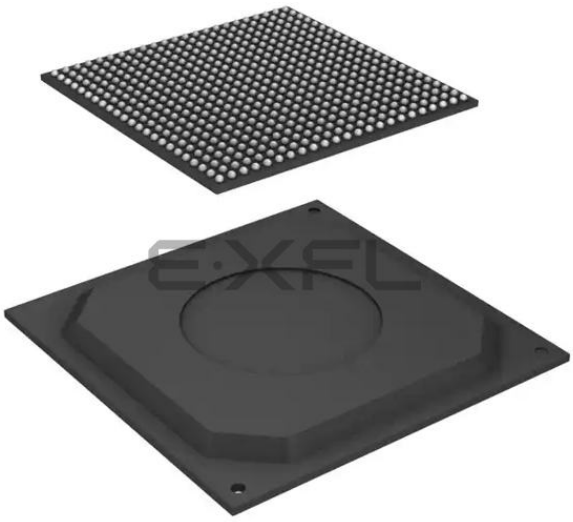

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx535dvv2c2

[7] By default, VDD_DIG_PLL is driven from internal on-die 1.2 V linear regulator (LDO). In this case, there is no need driving this supply externally. LDO output to VDD_DIG_PLL should be configured by software after power-up to 1.3 V output. A bypass capacitor of minimal value 22 µF should be connected to this pad in any case whether it is driven internally or externally. Use of the on-chip LDO is preferred. See i.MX53 System Development User's Guide.

[8] By default, the VDD_ANA_PLL is driven from internal on-die 1.8 V linear regulator (LDO). In this case there is no need driving this supply externally. A bypass capacitor of minimal value 22 µF should be connected to this pad in any case whether it is driven internally or externally. Use of the on-chip LDO is preferred. See i.MX53 System Development User's Guide.

[9] After fuses are programmed, Freescale strongly recommends the best practice of reading the fuses to verify that they are written correctly. In Read mode, VDD_FUSE should be floated or grounded. Tying VDD_FUSE to a positive supply (3.0 V–3.3 V) increases the possibility of inadvertently blowing fuses and is not recommended in read mode.

[10] If not using the TVE module or other pads in this power domain for the product, the TVDAC_DHVDD and TVDAC_AHVDDRGB can be kept floating or tied to GND—the recommendation is to float.

[11] GPIO pad operational at low frequency

[12] The analog supplies should be isolated in the application design. Use of series inductors is recommended.

[13] VDD_REG is power supply input for the integrated linear regulators of VDD_ANA_PLL and VDD_DIG_PLL when they are configured to the internal supply option. VDDR_REG still has to be tied to 2.5 V supply when VDD_ANA_PLL and VDD_DIG_PLL are configured for external power supply mode although in this case it is not used as supply source.

[14] For part number MCIMX535DVV1C, lifetime of 21,900 hours based on 95 ^{o}C junction temperature and nominal supply voltages. For part number MCIMX535DVV2C, lifetime of 4,380 hours at 1.2 GHz frequency and lifetime of 17,520 hours at 1 GHz frequency, based on 95 ^{o}C junction temperature and nominal supply voltages.

4.1.4 External Clock Sources

The i.MX53xD device has four external input system clocks, a low frequency (CKIL), a high frequency (XTAL), and two general purpose CKIH1 and CKIH2 clocks.

The CKIL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

CKIH1 and CKIH2 provide additional clock source option for peripherals that require specific and accurate frequencies.

Table 9 shows the interface frequency requirements. See Chapter 1 of *i.MX53 System Development User's Guide* (MX53UG) for additional clock and oscillator information.

Table 9. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
CKIL Oscillator[1]	f_{ckil}	—	32.768[2]/32.0	—	kHz
CKIH1, CKIH2 Operating Frequency	f_{ckih1}, f_{ckih2}	See Table 34, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 47			MHz
XTAL Oscillator	f_{xtal}	22	24	27	MHz

[1] External oscillator or a crystal with internal oscillator amplifier.

[2] Recommended nominal frequency 32.768 kHz.

4.5.1 GPIO I/O AC Electrical Characteristics

AC electrical characteristics for GPIO I/O in slow and fast modes are presented in the Table 22 and Table 23, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUXC control registers.

Table 22. GPIO I/O AC Parameters Slow Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.91/1.52 3.07/2.65	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	2.22/1.81 3.81/3.42	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.88/2.42 5.43/5.02	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.94/4.50 10.55/9.70	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.5/0.65 0.32/0.37	—	—	V/ns
Output Pad Slew Rate (High Drive)[1]	tps	15 pF 35 pF	0.43/0.54 0.26/0.41	—	—	
Output Pad Slew Rate (Medium Drive)[1]	tps	15 pF 35 pF	0.34/0.41 0.18/0.2	—	—	
Output Pad Slew Rate (Low Drive)[1]	tps	15 pF 35 pF	0.20/0.22 0.09/0.1	—	—	
Output Pad di/dt (Max Drive)	tdit	—	—	—	30	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	23	
Output Pad di/dt (Medium drive)	tdit	—	—	—	15	
Output Pad di/dt (Low drive)	tdit	—	—	—	7	
Input Transition Times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 23. GPIO I/O AC Parameters Fast Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.45/1.24 2.76/2.54	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	1.81/1.59 3.57/3.33	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.54/2.29 5.25/5.01	ns

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4 The typical value of Vox(ac) is expected to be about 0.5 x OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

Table 25 shows the AC parameters for LPDDR2 I/O operating in LPDDR2 mode.

Table 25. LPDDR2 I/O LPDDR2 mode AC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to OVDD/2	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	266 MHz	—	—	0.6	V-ns
Single output slew rate	tsr	50 Ω to Vref. 5pF load. Drive impedance= 40 Ω ± 30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5 pF load. Drive impedance= 60 Ω ± 30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 266 MHz clk = 400 MHz	—	—	0.2 0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 26 shows the AC parameters for LPDDR2 I/O operating in DDR3 mode.

Table 26. LPDDR2 I/O DDR3 mode AC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	—	Vref - 0.15	—	Vref + 0.15	V
Output AC differential cross point voltage[4]	Vox(ac)	—	Vref - 0.15	—	Vref + 0.15	V

Figure 28 and Table 42 show the address and control timing parameters for DDR2 and DDR3.

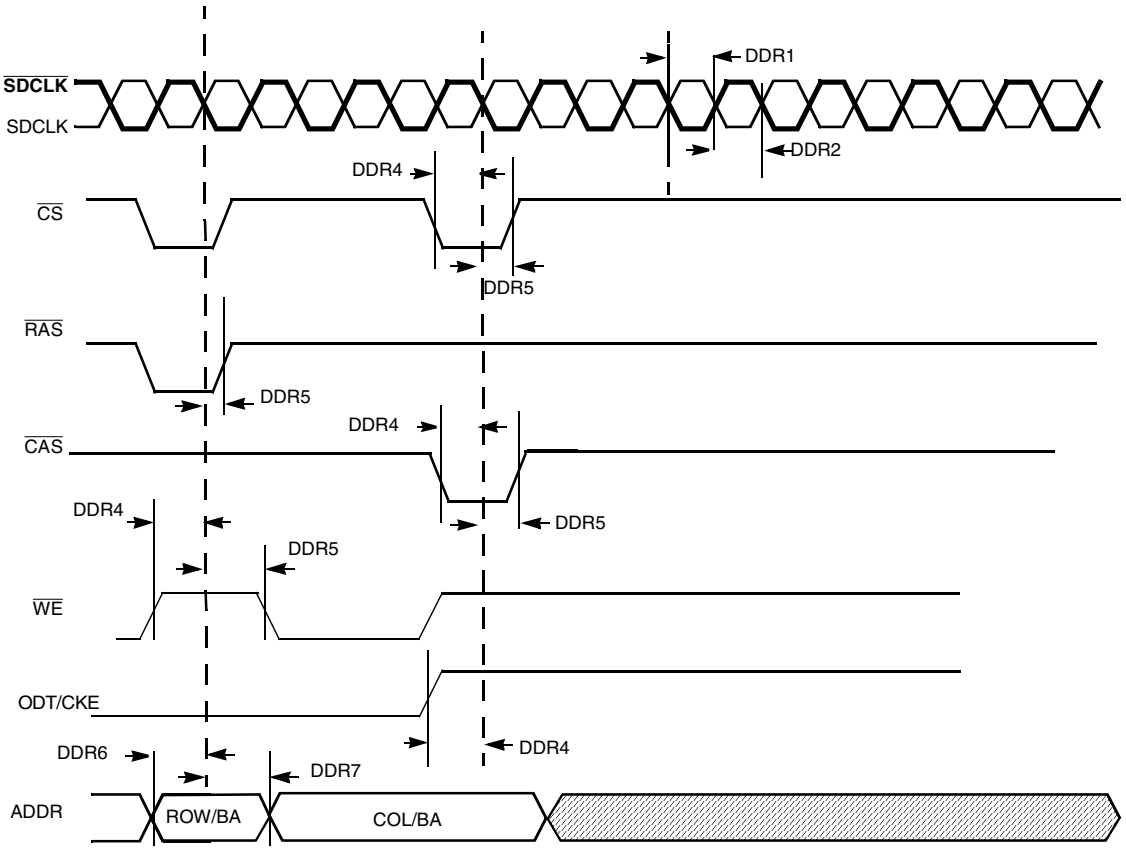

Figure 28. DDR SDRAM Address and Control Parameters for DDR2 and DDR3

Table 42. DDR SDRAM Timing Parameter Table[1] [2]

ID	Parameter	Symbol	SDCLK = 400 MHz		Units
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.48	0.52	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.48	0.52	t_{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}	0.6	—	ns
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}	0.6	—	ns
DDR6	Address output setup time	t_{IS}	0.6	—	ns
DDR7	Address output hold time	t_{IH}	0.6	—	ns

1 All timings are refer to Vref level cross point.

2 Reference load model is 25 Ω resistor from each of the DDR outputs to VDD_REF.

4.7.4 Enhanced Secured Digital Host Controller(eSDHCv2/v3) AC timing

This section describes the electrical information of the eSDHCv2/v3, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.7.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 36 depicts the timing of SD/eMMC4.3, and Table 51 lists the SD/eMMC4.3 timing characteristics.

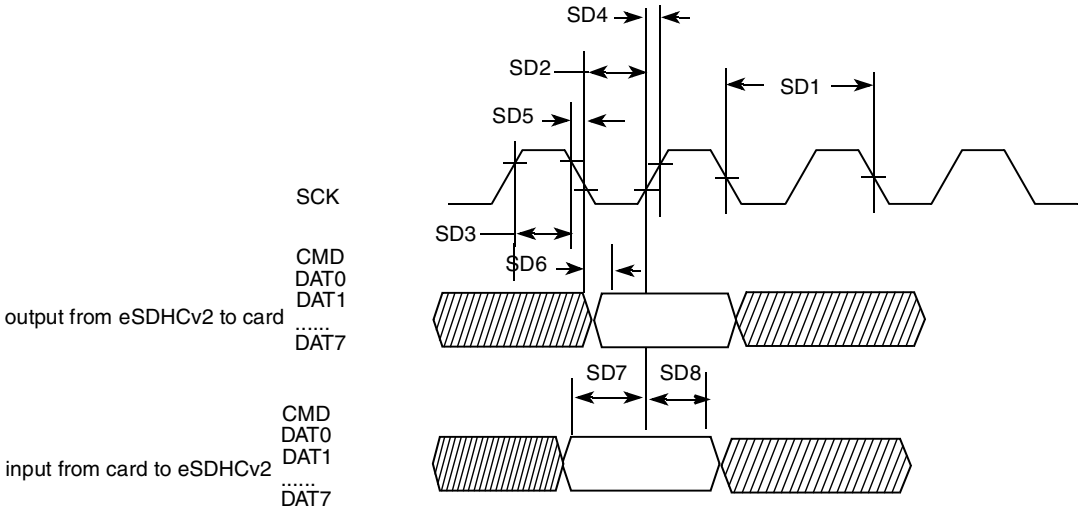

Figure 36. SD/eMMC4.3 Timing

Table 51. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHCv2 Output Delay (port 1, 2, and 4)	t_{OD}	-3.5	3.5	ns
	eSDHCv3 Output Delay (port 3)	t_{OD}	-4.5	4.5	ns

4.7.7.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.7.7.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.7.7.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 44.

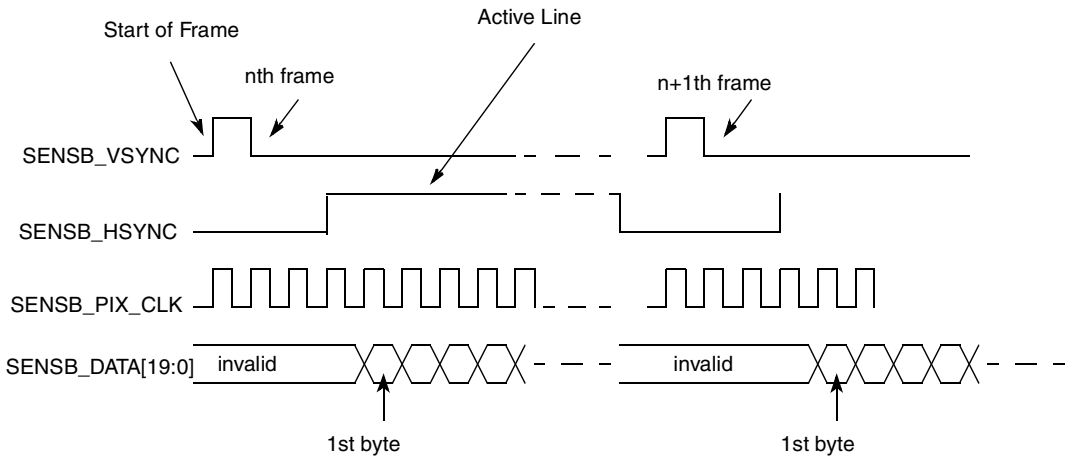

Figure 44. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

4.7.7.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.7.7.2.2, “Gated Clock Mode,”) except for the SENSB_HSYNC signal, which is not used (see Figure 45). All incoming pixel clocks are

NOTE

Table 61 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.7.7.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.7.7.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as HSYNC/VSYCN and so on) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the i.MX53 Reference Manual.

4.7.7.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

Table 62 shows timing characteristics of signals presented in Figure 48 and Figure 49.

Table 62. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH - BGXP - FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line.The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT - BGYP - FH) × Tsw	Width of second Vertical blanking interval in line.The FH should be built by suitable DI's counter.	ns

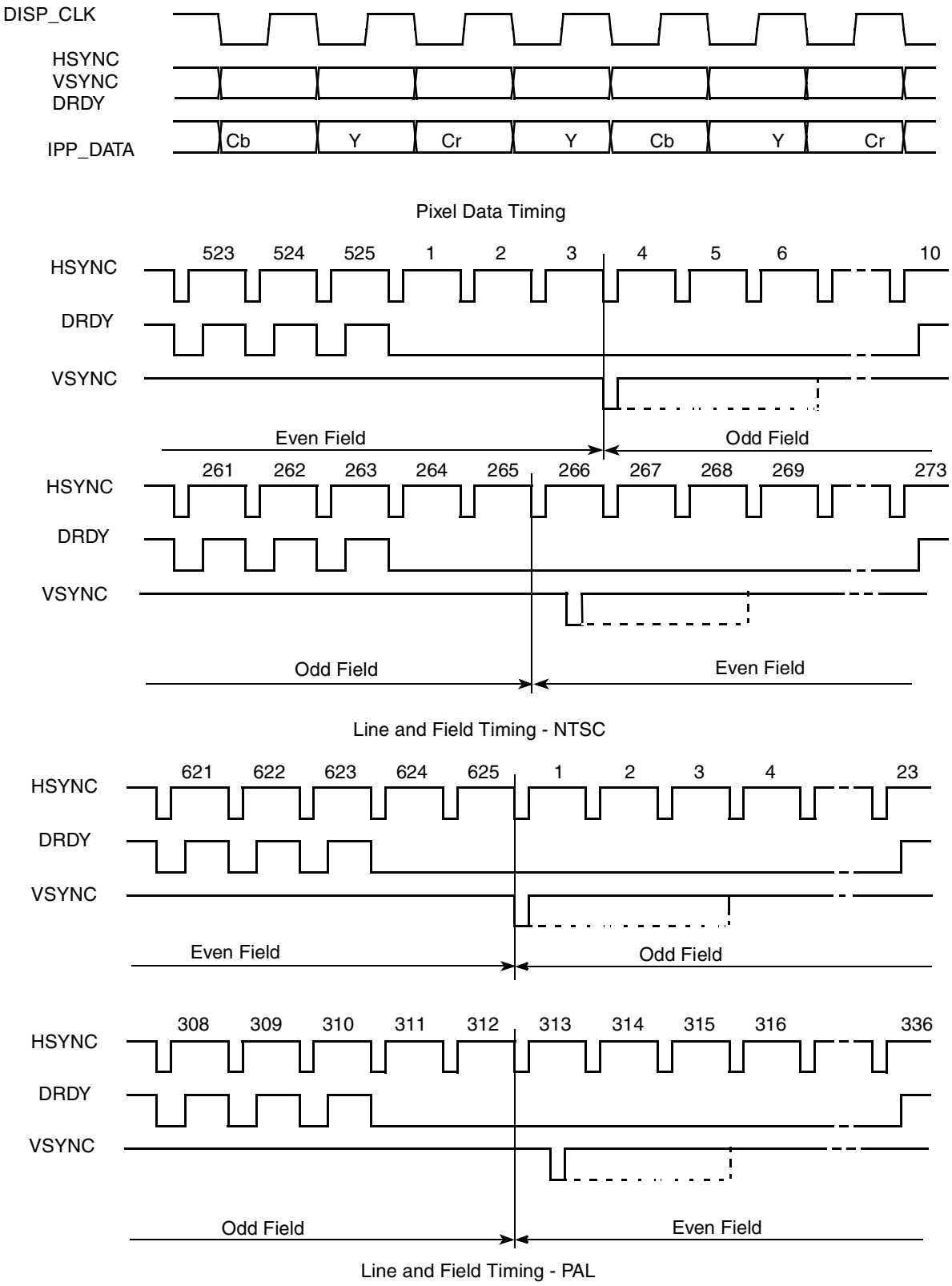

Figure 51. TV Encoder Interface Timing Diagram

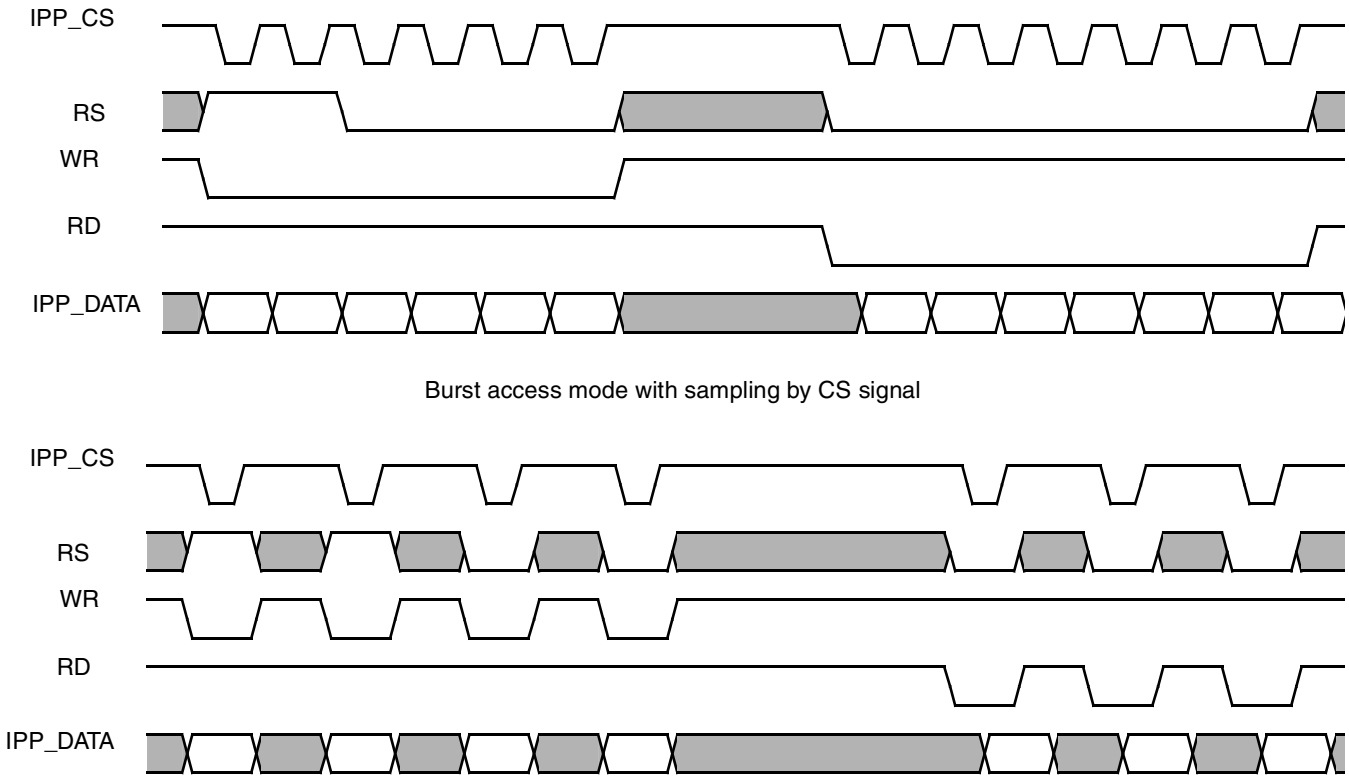

Figure 52. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

4.7.17.2 Parallel Interface (Normal ULPI) Timing

Electrical and timing specifications of Parallel Interface (Normal ULPI) for Host Port2 and Port3 are presented in the subsequent sections.

Table 101. Signal Definitions — Parallel Interface (Normal ULPI)

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to Clock.
USB_Data[7:0]	I/O	Bi-directional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the Data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

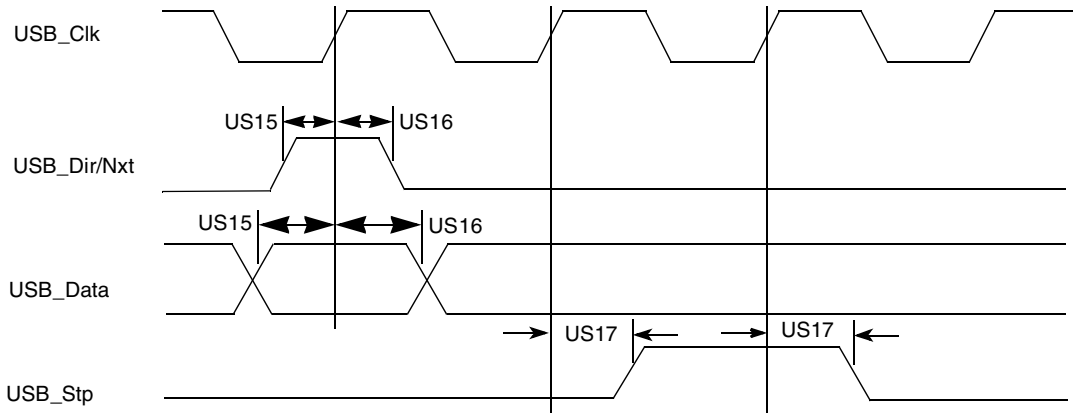

Figure 97. USB Transmit/Receive Waveform in Parallel Mode

Table 102. USB Timing Specification for Normal ULPI Mode

ID	Parameter	Min	Max	Unit	Conditions / Reference Signal
US15	Setup Time (Dir&Nxt in, Data in)	6.0	—	ns	10 pF
US16	Hold Time (Dir&Nxt in, Data in)	0.0	—	ns	10 pF
US17	Output Delay Time (Stp out, Data out	—	9.0	ns	10 pF

4.7.18 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

4.7.18.1 USB PHY AC Parameters

Table 103 lists the AC timing parameters for USB PHY.

Table 109. LDO Voltage Regulators Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Units
VDD_DIG_PLL functional Voltage Range[1]	$V_{VID\_DIG\_PLL}$	1.15	1.2	1.3	V
VDD_ANA_PLL functional Voltage Range[1]	$V_{VDD\_ANA\_PLL}$	1.7	1.8	1.95	V
VDD_DIG_PLL and VDD_ANA_PLL accuracy	—	—	—	±3	%
VDD_DIG_PLL power-supply rejection ratio[2]	—	—	-18	—	dB
VDD_ANA_PLL power-supply rejection ratio[2]	—	—	-15	—	dB
Output current[3]	$I_{VID\_DIG\_PLL}$+ $I_{VDD\_ANA\_PLL}$	—	—	125	mA

1 VDD_DIG_PLL and VDD_ANA_PLL voltages are programmable, but should not be set outside the target functional range for proper PLL operation.

2 The gain or attenuation from the input supply variation to the output of the LDO (by design).

3 The limitation is for sum of the VDD_DIG_PLL and VDD_ANA_PLL current.

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 110 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is ‘0’ (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see i.MX53 Fuse Map document and Boot chapter in i.MX53 reference manual.

Table 110. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFUSE Name	Details
BOOT_MODE[1]	Input	N/A	Boot Mode selection
BOOT_MODE[0]	Input		

The following notes apply to Figure 98, Figure 99, and Figure 100.

1. All dimensions are in millimeters.
2. Dimensions and tolerancing per ASME Y14.5M1–994.

6.1.2 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

Table 112 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 112. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

Contact Name	Package Contact Assignment(s)
DDR_VREF	L17
GND	A1, A11, A13, A18, A2, A22, A23, AA11, AA15, AA20, AA21, AB1, AB18, AB2, AB22, AB23, AC1, AC18, AC2, AC22, AC23, B1, B11, B13, B18, B23, C12, C20, C21, D19, E19, F19, F20, F21, F22, G19, G7, H10, H12, H8, J11, J13, J15, J17, J20, J9, K10, K12, K14, K16, K21, K8, L11, L13, L15, L7, L9, M10, M12, M14, M16, M8, N11, N13, N15, N9, P10, P12, P14, P16, P21, P7, P8, R11, R13, R15, R17, R20, R9, T10, T14, T16, T8, U15, U19, V15, V18, V19, V20, V21, V22, W19, Y14, Y15, Y19
NVCC_CKIH	G17
NVCC_CSI	R7
NVCC_EIM_MAIN	U10, U9
NVCC_EIM_SEC	U7
NVCC_EMI_DRAM	H18, K17, N17, P17, T18
NVCC_FEC	F11
NVCC_GPIO	F8
NVCC_JTAG	G9
NVCC_KEYPAD	F7
NVCC_LCD	J6, J7
NVCC_LVDS	U13
NVCC_LVDS_BG	U14
NVCC_NANDF	T12
NVCC_PATA	N7
NVCC_RESET	H16
NVCC_SD1	H15
NVCC_SD2	H14
NVCC_SRTC_POW	V11
NVCC_XTAL	V12
SVCC	B22

Table 113. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
DRAM_A3	N20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[3]	Output	Low
DRAM_A4	K20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[4]	Output	Low
DRAM_A5	N21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[5]	Output	Low
DRAM_A6	M22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[6]	Output	Low
DRAM_A7	N22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[7]	Output	Low
DRAM_A8	N23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[8]	Output	Low
DRAM_A9	M21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[9]	Output	Low
DRAM_CALIBRATION	M23	NVCC_EMI_DRAM	special	—	—	(used in DRAM driver calibration. See Section 3.1, “Special Signal Considerations”)	Input	—
DRAM_CAS	L18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CAS	Output	High
DRAM_CS0	K18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CS[0]	Output	High
DRAM_CS1	P19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CS[1]	Output	High
DRAM_D0	H20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[0]	Output	High
DRAM_D1	G21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[1]	Output	High
DRAM_D10	E22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[10]	Output	High
DRAM_D11	D20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[11]	Output	High
DRAM_D12	E23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[12]	Output	High
DRAM_D13	C23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[13]	Output	High
DRAM_D14	F23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[14]	Output	High
DRAM_D15	C22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[15]	Output	High
DRAM_D16	U20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[16]	Output	High

Table 113. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
EIM_DA10	AB7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[10]	Input[2]	100 KΩ PU
EIM_DA11	AC6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[11]	Input	100 KΩ PU
EIM_DA12	V10	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[12]	Input	100 KΩ PU
EIM_DA13	AC7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[13]	Input	100 KΩ PU
EIM_DA14	Y10	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[14]	Input	100 KΩ PU
EIM_DA15	AA9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[15]	Input	100 KΩ PU
EIM_DA2	AA7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[2]	Input[2]	100 KΩ PU
EIM_DA3	W9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[3]	Input[2]	100 KΩ PU
EIM_DA4	AB6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[4]	Input[2]	100 KΩ PU
EIM_DA5	V9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[5]	Input[2]	100 KΩ PU
EIM_DA6	Y9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[6]	Input[2]	100 KΩ PU
EIM_DA7	AC5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[7]	Input[2]	100 KΩ PU
EIM_DA8	AA8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[8]	Input[2]	100 KΩ PU
EIM_DA9	W10	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[9]	Input[2]	100 KΩ PU
EIM_EB0	AC3	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_EB[0]	Output[2]	—
EIM_EB1	AB5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_EB[1]	Output[2]	—
EIM_EB2	Y3	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-2	gpio2_GPIO[30]	Input	100 KΩ PU
EIM_EB3	Y4	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-2	gpio2_GPIO[31]	Input	100 KΩ PU
EIM_LBA	AA6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_LBA	Output[2]	—
EIM_OE	V8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_OE	Output	—
EIM_RW	AB4	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_RW	Output	—

Table 119. 12 x 12 mm PoP Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment (Top)	Contact Assignment (Bottom)	Power Rail	I/O Buffer Type	Out of Reset Condition[1]			
					Alt. Mode	Function	Direction	Config. Value
CSI0_DAT14	—	T1	NVCC_CSI	UHVIO	ALT1	gpio6_GPIO[0]	Input	360 KΩ PD
CSI0_DAT15	—	P1	NVCC_CSI	UHVIO	ALT1	gpio6_GPIO[1]	Input	360 KΩ PD
CSI0_DAT16	—	M1	NVCC_CSI	UHVIO	ALT1	gpio6_GPIO[2]	Input	360 KΩ PD
CSI0_DAT17	—	N1	NVCC_CSI	UHVIO	ALT1	gpio6_GPIO[3]	Input	360 KΩ PD
CSI0_DAT18	—	L2	NVCC_CSI	UHVIO	ALT1	gpio6_GPIO[4]	Input	360 KΩ PD
CSI0_DAT19	—	L1	NVCC_CSI	UHVIO	ALT1	gpio6_GPIO[5]	Input	360 KΩ PD
CSI0_DAT4	—	T7	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[22]	Input	100 KΩ PU
CSI0_DAT5	—	R3	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[23]	Input	360 KΩ PD
CSI0_DAT6	—	P7	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[24]	Input	100 KΩ PU
CSI0_DAT7	—	N7	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[25]	Input	100 KΩ PU
CSI0_DAT8	—	U2	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[26]	Input	100 KΩ PU
CSI0_DAT9	—	P3	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[27]	Input	360 KΩ PD
CSI0_DATA_EN	—	P6	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[20]	Input	100 KΩ PU
CSI0_MCLK	—	T6	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[19]	Input	100 KΩ PU
CSI0_PIXCLK	—	U6	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[18]	Input	100 KΩ PU
CSI0_VSYNC	—	U7	NVCC_CSI	UHVIO	ALT1	gpio5_GPIO[21]	Input	100 KΩ PU
DI0_DISP_CLK	—	AF2	NVCC_LCD	GPIO	ALT1	gpio4_GPIO[16]	Input	100 KΩ PU
DI0_PIN15	—	AH6	NVCC_LCD	GPIO	ALT1	gpio4_GPIO[17]	Input	100 KΩ PU
DI0_PIN2	—	AD7	NVCC_LCD	GPIO	ALT1	gpio4_GPIO[18]	Input	100 KΩ PU

Table 119. 12 x 12 mm PoP Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment (Top)	Contact Assignment (Bottom)	Power Rail	I/O Buffer Type	Out of Reset Condition[1]			
					Alt. Mode	Function	Direction	Config. Value
DRAM_SDQS0_B	P22	P28	NVCC_EMI_DRAM	DDR3CLK	ALT0	emi_DRAM_SDQS_B[0]	Input	High
DRAM_SDQS1	AB18	AE28	NVCC_EMI_DRAM	DDR3CLK	ALT0	emi_DRAM_SDQS[1]	Input	Low
DRAM_SDQS1_B	AC19	AE27	NVCC_EMI_DRAM	DDR3CLK	ALT0	emi_DRAM_SDQS_B[1]	Input	High
DRAM_SDQS2	J22	G28	NVCC_EMI_DRAM	DDR3CLK	ALT0	emi_DRAM_SDQS[2]	Input	Low
DRAM_SDQS2_B	K23	G29	NVCC_EMI_DRAM	DDR3CLK	ALT0	emi_DRAM_SDQS_B[2]	Input	High
DRAM_SDQS3	B18	C22	NVCC_EMI_DRAM	DDR3CLK	ALT0	emi_DRAM_SDQS[3]	Input	Low
DRAM_SDQS3_B	A19	C21	NVCC_EMI_DRAM	DDR3CLK	ALT0	emi_DRAM_SDQS_B[3]	Input	High
DRAM_SDWE	—	K29	NVCC_EMI_DRAM	DDR3	ALT0	emi_DRAM_SDWE	Output	High
ECKIL	—	G14	NVCC_SRTC_POW	ANALOG		ECKIL	—	—
EIM_A16	—	A7	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[16]	Output[2]	—
EIM_A17	—	G8	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[17]	Output[2]	—
EIM_A18	—	F8	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[18]	Output[2]	—
EIM_A19	—	A6	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[19]	Output[2]	—
EIM_A20	—	B7	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[20]	Output[2]	—
EIM_A21	—	C6	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[21]	Output[2]	—
EIM_A22	—	C2	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[22]	Output[2]	—
EIM_A23	—	B3	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[23]	Output	—
EIM_A24	—	A4	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[24]	Output	—
EIM_A25	—	A3	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_A[25]	Output	—
EIM_BCLK	—	F11	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_BCLK	Output	—
EIM_CS0	—	G10	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_CS[0]	Output	—
EIM_CS1	—	C4	NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_CS[1]	Output	—
EIM_D16	—	H1	NVCC_EIM_SEC	UHVIO	ALT1	gpio3_GPIO[16]	Input	100 KΩ PU
EIM_D17	—	G3	NVCC_EIM_SEC	UHVIO	ALT1	gpio3_GPIO[17]	Input	100 KΩ PU

Table 119. 12 x 12 mm PoP Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment (Top)	Contact Assignment (Bottom)	Power Rail	I/O Buffer Type	Out of Reset Condition[1]			
					Alt. Mode	Function	Direction	Config. Value
LVDS1_CLK_N	—	A15	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[27]	Input	Floating
LVDS1_CLK_P	—	B15	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[26]	Input	Floating
LVDS1_TX0_N	—	B17	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[31]	Input	Floating
LVDS1_TX0_P	—	A17	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[30]	Input	Floating
LVDS1_TX1_N	—	A16	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[29]	Input	Floating
LVDS1_TX1_P	—	B16	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[28]	Input	Floating
LVDS1_TX2_N	—	A14	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[25]	Input	Floating
LVDS1_TX2_P	—	B14	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[24]	Input	Floating
LVDS1_TX3_N	—	A13	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[23]	Input	Floating
LVDS1_TX3_P	—	B13	NVCC_LVDS	LVDS	ALT0	gpio6_GPI[22]	Input	Floating
NANDF_ALE	L2	N3	NVCC_NANDF	UHVIO	ALT1	gpio6_GPIO[8]	Input	100 KΩ PU
NANDF_CLE	—	G16	NVCC_NANDF	UHVIO	ALT1	gpio6_GPIO[7]	Input	100 KΩ PU
NANDF_CS0	M1	P2	NVCC_NANDF	UHVIO	ALT1	gpio6_GPIO[11]	Input	100 KΩ PU
NANDF_CS1	—	A11	NVCC_NANDF	UHVIO	ALT1	gpio6_GPIO[14]	Input	100 KΩ PU
NANDF_CS2	—	C12	NVCC_NANDF	UHVIO	ALT1	gpio6_GPIO[15]	Input	100 KΩ PU
NANDF_CS3	—	A12	NVCC_NANDF	UHVIO	ALT1	gpio6_GPIO[16]	Input	100 KΩ PU
NANDF_RB0	—	C15	NVCC_NANDF	UHVIO	ALT1	gpio6_GPIO[10]	Input	100 KΩ PU
NANDF_RE_B	K2	M3	NVCC_EIM_MAIN	UHVIO	ALT1	gpio6_GPIO[13]	Input	100 KΩ PU
NANDF_WE_B	K1	M2	NVCC_EIM_MAIN	UHVIO	ALT1	gpio6_GPIO[12]	Input	100 KΩ PU

Table 119. 12 x 12 mm PoP Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment (Top)	Contact Assignment (Bottom)	Power Rail	I/O Buffer Type	Out of Reset Condition[1]			
					Alt. Mode	Function	Direction	Config. Value
TVDAC_COMP	—	A25	TVDAC_AHVDDRGB	ANALOG	—	TVDAC_COMP	—	—
TVDAC_IOB	—	A23	TVDAC_AHVDDRGB	ANALOG	—	TVDAC_IOB	—	—
TVDAC_IOG	—	B24	TVDAC_AHVDDRGB	ANALOG	—	TVDAC_IOG	—	—
TVDAC_IOR	—	C29	TVDAC_AHVDDRGB	ANALOG	—	TVDAC_IOR	—	—
USB_H1_DN	—	AH21	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB_H1_DN	—	—
USB_H1_DP	—	AJ21	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB_H1_DP	—	—
USB_H1_GPANAIO	—	AJ20	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	USB_H1_GPANAIO	—	—
USB_H1_RREFEXT	—	AH20	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	USB_H1_RREFEXT	—	—
USB_H1_VBUS	—	AJ22	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB_H1_VBUS	—	—
USB_OTG_DN	—	AJ23	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB_OTG_DN	—	—
USB_OTG_DP	—	AH23	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB_OTG_DP	—	—
USB_OTG_GPANAIO	—	AH24	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB_OTG_GPANAIO	—	—
USB_OTG_ID	—	AH22	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB_OTG_ID	—	—
USB_OTG_RREFEXT	—	AJ24	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB_OTG_RREFEXT	—	—

Table 121. PoP 12 × 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

AG	AF	AE	AD	AC	AB	AA
DISP0_DAT7	DISP0_DAT4	DISP0_DAT5	DISP0_DAT0	DISP0_DAT12	PATA_CS_1	PATA_DATA13
DISP0_DAT10	DI0_DISP_CLK	DISP0_DAT3	DISP0_DAT6	DISP0_DAT2	PATA_DA_1	PATA_CS_0
DISP0_DAT14	POP_VDD2	DISP0_DAT11	POP_VDDCA	DISP0_DAT1	PATA_DIOR	POP_VDDCA
DISP0_DAT8	NC	NC	NC	NC	NC	NC
DISP0_DAT16	NC	NC	NC	NC	NC	NC
POP_VDD1	NC	NC	NVCC_KEYPAD	DI0_PIN4	DISP0_DAT17	PATA_DIOW
KEY_ROW3	NC	NC	DI0_PIN2	DI0_PIN3	DISP0_DAT21	DISP0_DAT19
KEY_COL2	NC	NC	KEY_ROW4	VDDAL1	NC	NC
KEY_COL0	NC	NC	NVCC_GPIO	GPIO_18	NC	NC
POP_VDDCA	NC	NC	GPIO_8	GPIO_17	NC	NC
GPIO_2	NC	NC	NVCC_JTAG	GPIO_7	NC	NC
POP_VDD2	NC	NC	GPIO_0	GPIO_3	NC	NC
POP_VDDMM	NC	NC	JTAG_TCK	GPIO_9	NC	NC
POP_VACC	NC	NC	VDDA	NVCC_FEC	NC	NC
JTAG_TDO	NC	NC	JTAG_MOD	JTAG_TDI	NC	NC
POP_VDDQ	NC	NC	JTAG_TMS	NVCC_SD2	NC	NC
SD2_DATA1	NC	NC	SD2_DATA2	JTAG_TRSTB	NC	NC
SD2_DATA3	NC	NC	NVCC_RESET	USB_H1_VDDA33	NC	NC
SD2_CLK	NC	NC	USB_H1_VDDA25	USB_OTG_VDDA25	NC	NC
POP_VDDQ	NC	NC	USB_OTG_VDDA33	NVCC_SD1	NC	NC
USB_OTG_VBUS	NC	NC	SD2_CMD	VDD_FUSE	NC	NC
DRAM_D10	NC	NC	NVCC_CKIH	VDD_ANA_PLL	NC	NC
DRAM_D12	NC	NC	VDD_REG	VDD_DIG_PLL	DRAM_CS0	DRAM_CAS
POP_VDDQ	NC	NC	NVCC_EMI_DRAM	NVCC_EMI_DRAM	DRAM_SDCKE0	DRAM_A4
SD1_DATA1	NC	NC	NC	NC	NC	NC
POP_VDD1	NC	NC	NC	NC	NC	NC
POP_VDD2	POP_VDDQ	DRAM_SDQS1_B	DRAM_DQM1	POR_B	POP_VDDQ	TEST_MODE
DRAM_D14	DRAM_D8	DRAM_SDQS1	FASTR_DIG	CKIH2	RESET_IN_B	BOOT_MODE0
DRAM_D11	DRAM_D13	DRAM_D9	FASTR_ANA	CKIH1	BOOT_MODE1	FEC_MDIO
AG	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**