Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	32KB (16K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18c658t-e-l

5.0 TABLE READS/TABLE WRITES

All PICmicro® devices have two memory spaces: the program memory space and the data memory space. Table Reads and Table Writes have been provided to move data between these two memory spaces through an 8-bit register (TABLAT).

The operations that allow the processor to move data between the data and program memory spaces are:

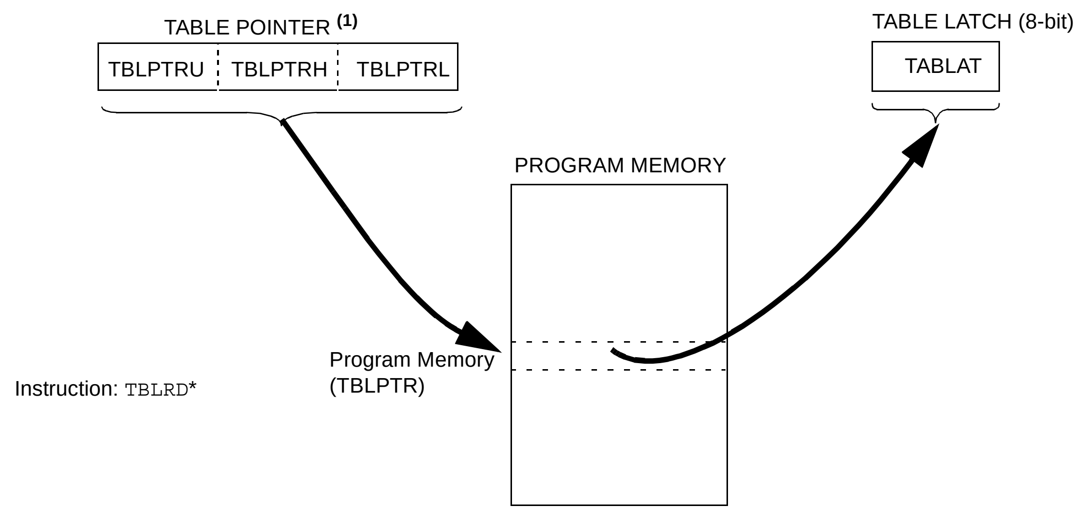
- Table Read (TBLRD)
- Table Write (TBLWT)

Table Read operations retrieve data from program memory and place it into the data memory space. Figure 5-1 shows the operation of a Table Read with program and data memory.

Table Write operations store data from the data memory space into program memory. Figure 5-2 shows the operation of a Table Write with program and data memory.

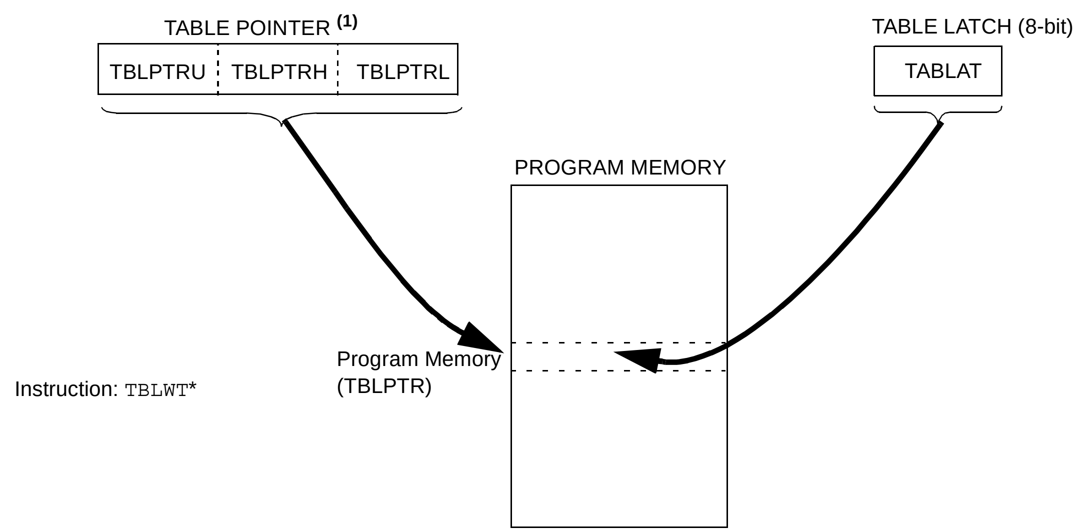
Table operations work with byte entities. A table block containing data is not required to be word aligned, so a table block can start and end at any byte address. If a table write is being used to write an executable program to program memory, program instructions will need to be word aligned.

FIGURE 5-1: TABLE READ OPERATION



Note 1: Table Pointer points to a byte in program memory.

FIGURE 5-2: TABLE WRITE OPERATION



Note 1: Table Pointer points to a byte in program memory.

5.2.3 LONG WRITE INTERRUPTS

The long write must be terminated by a RESET or any interrupt.

The interrupt source must have its interrupt enable bit set. When the source sets its interrupt flag, programming will terminate. This will occur regardless of the settings of interrupt priority bits, the GIE/GIEH bit or the PIE/GIEL bit.

Depending on the states of interrupt priority bits, the GIE/GIEH bit or the PIE/GIEL bit, program execution can either be vectored to the high or low priority Interrupt Service Routine (ISR), or continue execution from where programming commenced.

In either case, the interrupt flag will not be cleared when programming is terminated and will need to be cleared by the software.

5.3 Unexpected Termination of Write Operations

If a write is terminated by an unplanned event such as loss of power, an unexpected RESET, or an interrupt that was not disabled, the memory location just programmed should be verified and reprogrammed if needed.

TABLE 5-2: SLEEP MODE, INTERRUPT ENABLE BITS AND INTERRUPT RESULTS

GIE/ GIEH	PIE/ GIEL	Priority	Interrupt Enable	Interrupt Flag	Action
X	X	X	0 (default)	X	Long write continues even if interrupt flag becomes set during SLEEP.
X	X	X	1	0	Long write continues, will wake when the interrupt flag is set.
0 (default)	0 (default)	X	1	1	Terminates long write, executes next instruction. Interrupt flag not cleared.
0 (default)	1	1 high priority (default)	1	1	Terminates long write, executes next instruction. Interrupt flag not cleared.
1	0 (default)	0 low	1	1	Terminates long write, executes next instruction. Interrupt flag not cleared.
0 (default)	1	0 low	1	1	Terminates long write, branches to low priority interrupt vector. Interrupt flag can be cleared by ISR.
1	0 (default)	1 high priority (default)	1	1	Terminates long write, branches to high priority interrupt vector. Interrupt flag can be cleared by ISR.

REGISTER 7-6: PIE REGISTERS (CONT'D)

PIE2

bit 7 **Unimplemented:** Read as '0'

bit 6 **CMIE:** Comparator Interrupt Enable bit
1 = Enables the comparator interrupt
0 = Disables the comparator interrupt

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **BCLIE**: Bus Collision Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 **LVDIE**: Low-voltage Detect Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 1 **TMR3IE**: TMR3 Overflow Interrupt Enable bit
1 = Enables the TMR3 overflow interrupt
0 = Disables the TMR3 overflow interrupt

bit 0 **CCP2IE**: CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

PIE3

bit 7 **IVRE:** Invalid CAN Message Received Interrupt Enable bit
1 = Enables the Invalid CAN Message Received Interrupt
0 = Disables the Invalid CAN Message Received Interrupt

bit 6 **WAKIE:** Bus Activity Wake-up Interrupt Enable bit
1 = Enables the Bus Activity Wake-Up Interrupt
0 = Disables the Bus Activity Wake-Up Interrupt

bit 5 **ERRIE:** CAN Bus Error Interrupt Enable bit
1 = Enables the CAN Bus Error Interrupt
0 = Disables the CAN Bus Error Interrupt

bit 4 **TXB2IE:** Transmit Buffer 2 Interrupt Enable bit
1 = Enables the Transmit Buffer 2 Interrupt
0 = Disables the Transmit Buffer 2 Interrupt

bit 3 **TXB1IE:** Transmit Buffer 1 Interrupt Enable bit
1 = Enables the Transmit Buffer 1 Interrupt
0 = Disables the Transmit Buffer 1 Interrupt

bit 2 **TXB0IE:** Transmit Buffer 0 Interrupt Enable bit
1 = Enables the Transmit Buffer 0 Interrupt
0 = Disables the Transmit Buffer 0 Interrupt

bit 1 **RXB1IE:** Receive Buffer 1 Interrupt Enable bit
1 = Enables the Receive Buffer 1 Interrupt
0 = Disables the Receive Buffer 1 Interrupt

bit 0 **RXB0IE:** Receive Buffer 0 Interrupt Enable bit
1 = Enables the Receive Buffer 0 Interrupt
0 = Disables the Receive Buffer 0 Interrupt

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

8.4 PORTD, TRISD and LATD Registers

PORTD is an 8-bit wide, bi-directional port. The corresponding Data Direction register is TRISD. Setting a TRISD bit (=1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a hi-impedance mode). Clearing a TRISD bit (=0) will make the corresponding PORTD pin an output (i.e., put the contents of the output latch on the selected pin).

Read-modify-write operations on the LATD register reads and writes the latched output value for PORTD.

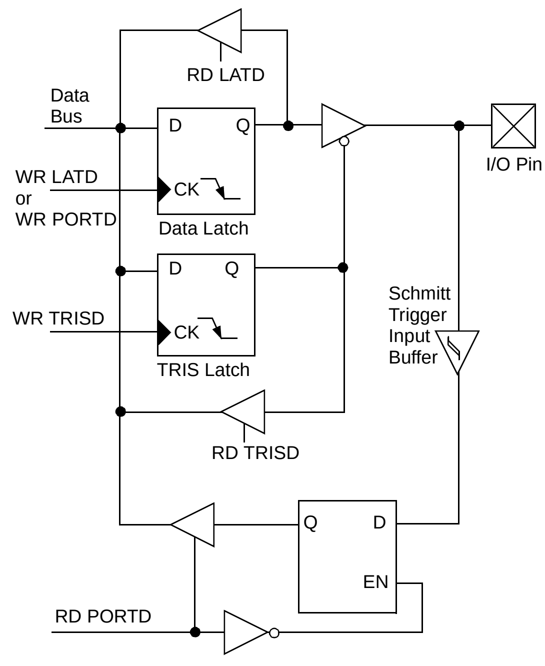
PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port), by setting control bit PSPMODE (PSPCON register). In this mode, the input buffers are TTL. See Section 9.0 for additional information on the Parallel Slave Port (PSP).

EXAMPLE 8-4: INITIALIZING PORTD

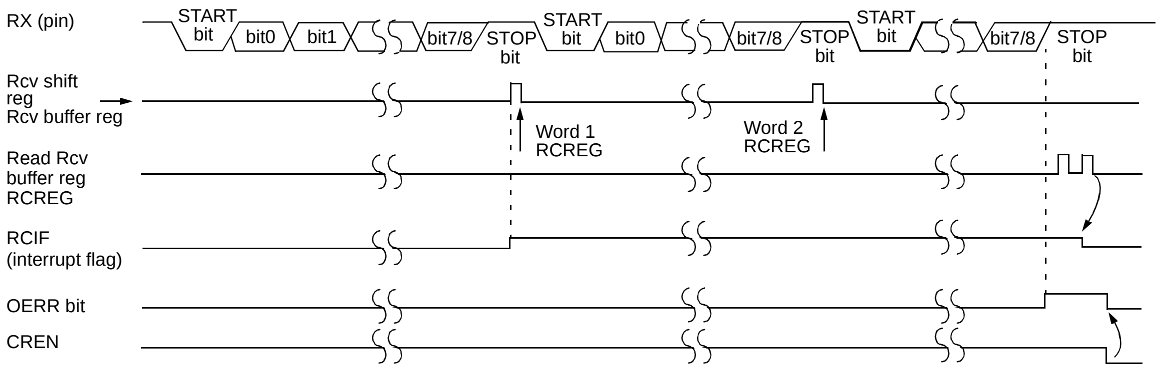
```
CLRF    PORTD     ; Initialize PORTD by
                  ; clearing output
                  ; data latches
CLRF    LATD      ; Alternate method
                  ; to clear output
                  ; data latches
MOVLW   0xCF      ; Value used to
                  ; initialize data
                  ; direction
MOVWF   TRISD     ; Set RD3:RD0 as inputs
                  ; RD5:RD4 as outputs
                  ; RD7:RD6 as inputs
```

FIGURE 8-7: PORTD BLOCK DIAGRAM IN I/O PORT MODE



Note: I/O pins have diode protection to VDD and VSS.

FIGURE 16-5: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.

TABLE 16-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
RCREG	USART Receive Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	ADDEN	BRGH	TRMT	TX9D	0000 0010	0000 0010
SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.

 Advanced Information

16.4 USART Synchronous Slave Mode

Synchronous Slave mode differs from the Master mode, in that the shift clock is supplied externally at the RC6/TX/CK pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTA register).

16.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes are identical, except in the case of the SLEEP mode.

If two words are written to the TXREG and then the `SLEEP` instruction is executed, the following will occur:

a) The first word will immediately transfer to the TSR register and transmit.

b) The second word will remain in TXREG register.

c) Flag bit TXIF will not be set.

d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will be set.

e) If enable bit TXIE is set, the interrupt will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector.

Steps to follow when setting up a Synchronous Slave Transmission:

1. Enable the synchronous slave serial port by setting bits SYNC and SPEN and clearing bit CSRC.
2. Clear bits CREN and SREN.
3. If interrupts are desired, set enable bit TXIE.
4. If 9-bit transmission is desired, set bit TX9.
5. Enable the transmission by setting enable bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.

16.4.2 USART SYNCHRONOUS SLAVE RECEPTION

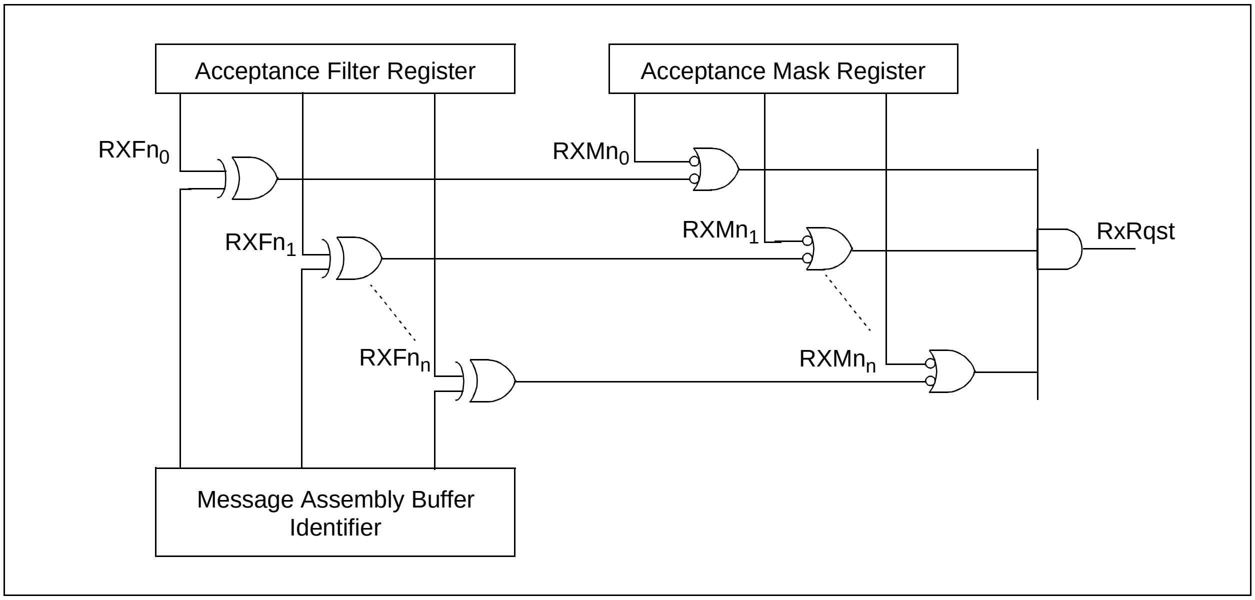
The operation of the Synchronous Master and Slave modes is identical, except in the case of the SLEEP mode and bit SREN, which is a "don't care" in Slave mode.

If receive is enabled by setting bit CREN prior to the `SLEEP` instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register, and if enable bit RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector.

Steps to follow when setting up a Synchronous Slave Reception:

1. Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
2. If interrupts are desired, set enable bit RCIE.
3. If 9-bit reception is desired, set bit RX9.
4. To enable reception, set enable bit CREN.
5. Flag bit RCIF will be set when reception is complete. An interrupt will be generated if enable bit RCIE was set.
6. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
7. Read the 8-bit received data by reading the RCREG register.
8. If any error occurred, clear the error by clearing bit CREN.

FIGURE 17-5: MESSAGE ACCEPTANCE MASK AND FILTER OPERATION



17.8 Synchronization

To compensate for phase shifts between the oscillator frequencies of each of the nodes on the bus, each CAN controller must be able to synchronize to the relevant signal edge of the incoming signal. When an edge in the transmitted data is detected, the logic will compare the location of the edge to the expected time (Sync Seg). The circuit will then adjust the values of phase segment 1 and phase segment 2, as necessary. There are two mechanisms used for synchronization.

17.8.1 HARD SYNCHRONIZATION

Hard Synchronization is only done when there is a recessive to dominant edge during a BUS IDLE condition, indicating the start of a message. After hard synchronization, the bit time counters are restarted with Sync Seg. Hard synchronization forces the edge, which has occurred to lie within the synchronization segment of the restarted bit time. Due to the rules of synchronization, if a hard synchronization occurs, there will not be a resynchronization within that bit time.

17.8.2 RESYNCHRONIZATION

As a result of Resynchronization, phase segment 1 may be lengthened, or phase segment 2 may be shortened. The amount of lengthening or shortening of the phase buffer segments has an upper bound given by the Synchronization Jump Width (SJW). The value of the SJW will be added to phase segment 1 (see Figure 17-7), or subtracted from phase segment 2 (see Figure 17-8). The SJW is programmable between 1 T_Q and 4 T_Q.

Clocking information will only be derived from recessive to dominant transitions. The property that only a fixed maximum number of successive bits have the same value, ensures resynchronization to the bit stream during a frame.

The phase error of an edge is given by the position of the edge relative to Sync Seg, measured in T_Q. The phase error is defined in magnitude of T_Q as follows:

- e = 0 if the edge lies within SYNCESEG.
- e > 0 if the edge lies before the SAMPLE POINT.
- e < 0 if the edge lies after the SAMPLE POINT of the previous bit.

If the magnitude of the phase error is less than, or equal to, the programmed value of the synchronization jump width, the effect of a resynchronization is the same as that of a hard synchronization.

If the magnitude of the phase error is larger than the synchronization jump width, and if the phase error is positive, then phase segment 1 is lengthened by an amount equal to the synchronization jump width.

If the magnitude of the phase error is larger than the resynchronization jump width, and if the phase error is negative, then phase segment 2 is shortened by an amount equal to the synchronization jump width.

17.8.3 SYNCHRONIZATION RULES

- Only one synchronization within one bit time is allowed.
- An edge will be used for synchronization only if the value detected at the previous sample point (previously read bus value) differs from the bus value immediately after the edge.
- All other recessive to dominant edges, fulfilling rules 1 and 2, will be used for resynchronization with the exception that a node transmitting a dominant bit will not perform a resynchronization, as a result of a recessive to dominant edge with a positive phase error.

21.1 Control Register

The Low Voltage Detect Control register (Register 21-1) controls the operation of the Low Voltage Detect circuitry.

REGISTER 21-1: LVDCON REGISTER

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
—	—	IRVST	LVDEN	LVDL3	LVDL2	LVDL1	LVDL0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit
1 = Indicates that the Low Voltage Detect logic will generate the interrupt flag at the specified voltage range
0 = Indicates that the Low Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the LVD interrupt should not be enabled

bit 4 **LVDEN:** Low Voltage Detect Power Enable bit
1 = Enables LVD, powers up LVD circuit
0 = Disables LVD, powers down LVD circuit

bit 3-0 **LVDL3:LVDL0:** Low Voltage Detection Limit bits
1111 = External analog input is used (input comes from the LVDIN pin)
1110 = 4.5V min - 4.77V max.
1101 = 4.2V min - 4.45V max.
1100 = 4.0V min - 4.24V max.; Reserved on PIC18CXX8
1011 = 3.8V min - 4.03V max.; Reserved on PIC18CXX8
1010 = 3.6V min - 3.82V max.; Reserved on PIC18CXX8
1001 = 3.5V min - 3.71V max.; Reserved on PIC18CXX8
1000 = 3.3V min - 3.50V max.; Reserved on PIC18CXX8
0111 = 3.0V min - 3.18V max.; Reserved on PIC18CXX8
0110 = 2.8V min - 2.97V max.; Reserved on PIC18CXX8
0101 = 2.7V min - 2.86V max.; Reserved on PIC18CXX8
0100 = 2.5V min - 2.65V max.; Reserved on PIC18CXX8
0011 = Reserved on PIC18CXX8 and PIC18LCXX8
0010 = Reserved on PIC18CXX8 and PIC18LCXX8
0001 = Reserved on PIC18CXX8 and PIC18LCXX8
0000 = Reserved on PIC18CXX8 and PIC18LCXX8

Note: LVDL3:LVDL0 modes which result in a trip point below the valid operating voltage of the device are not tested.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

21.2 Operation

Depending on the power source for the device voltage, the voltage normally decreases relatively slowly. This means that the LVD module does not need to be constantly operating. To decrease current consumption, the LVD circuitry only needs to be enabled for short periods, where the voltage is checked. After doing the check, the LVD module may be disabled.

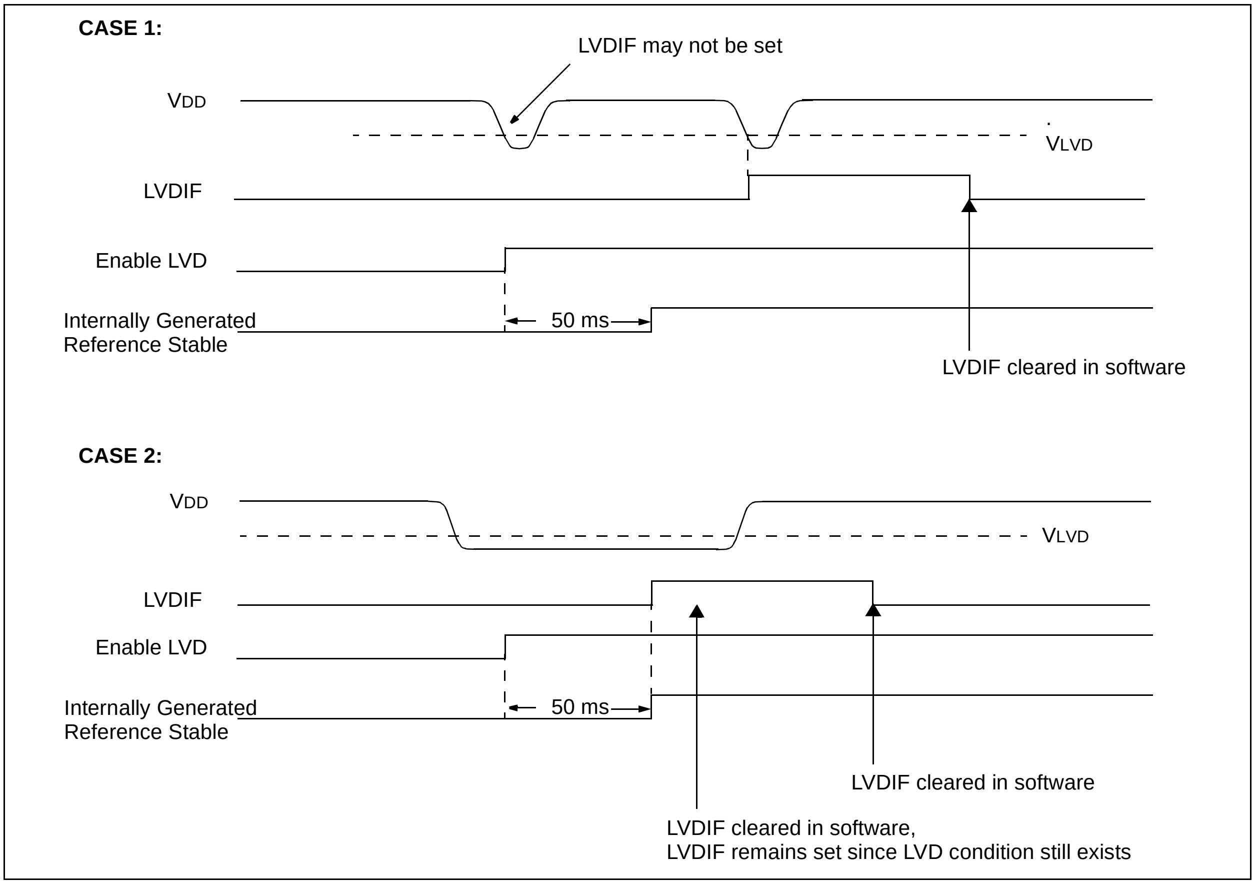
Each time that the LVD module is enabled, the circuitry requires some time to stabilize. After the circuitry has stabilized, all status flags may be cleared. The module will then indicate the proper state of the system.

The following steps are needed to setup the LVD module:

1. Write the value to the LVDL3:LVDL0 bits (LVDCON register), which selects the desired LVD Trip Point.
2. Ensure that LVD interrupts are disabled (the LVDIE bit is cleared or the GIE bit is cleared).
3. Enable the LVD module (set the LVDEN bit in the LVDCON register).
4. Wait for the LVD module to stabilize (the IRVST bit to become set).
5. Clear the LVD interrupt flag, which may have falsely become set, until the LVD module has stabilized (clear the LVDIF bit).
6. Enable the LVD interrupt (set the LVDIE and the GIE bits).

Figure 21-3 shows typical waveforms that the LVD module may be used to detect.

FIGURE 21-3: LOW VOLTAGE DETECT WAVEFORMS



22.0 SPECIAL FEATURES OF THE CPU

There are several features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection:

- OSC Selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Programmable Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code Protection
- ID Locations
- In-circuit Serial Programming

PIC18CXX8 devices have a Watchdog Timer, which is permanently enabled via the configuration bits or it can be software-controlled. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay on power-up only, designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer Wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

22.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 300000h.

The user will note that address 300000h is beyond the user program memory space. In fact, it belongs to the configuration memory space (300000h - 3FFFFFh), which can only be accessed using table reads and table writes.

TABLE 22-1: CONFIGURATION BITS AND DEVICE ID'S

Filename		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300000h	CONFIG1L	CP	CP	CP	CP	CP	CP	CP	CP	1111 1111
300001h	CONFIG1H	r	r	$\overline{\text{OSCSEN}}$	—	—	FOSC2	FOSC1	FOSC0	111- -111
300002h	CONFIG2L	—	—	—	—	BORV1	BORV0	BODEN	$\overline{\text{PWRTEN}}$	---- 1111
300003h	CONFIG2H	—	—	—	—	WDTPS2	WDTPS1	WDTPS0	WDTEN	---- 1111
300006h	CONFIG4L	—	—	—	—	—	—	r	STVREN	---- --11
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	1111 1111
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved.
Grayed cells are unimplemented, read as '0'.

ADDWFC — ADD WREG and Carry bit to f

Syntax:	[*label*] ADDWFC f [,d [,a]]
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]
Operation:	(WREG) + (f) + (C) → dest
Status Affected:	N,OV, C, DC, Z
Encoding:	`0010` `00da` `ffff` `ffff`
Description:	Add WREG, the Carry Flag and data memory location 'f'. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed in data memory location 'f'. If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the Bank will be selected as per the BSR value.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `ADDWFC REG, W`

Before Instruction

C	=	1
REG	=	0x02
WREG	=	0x4D
N	=	?
OV	=	?
DC	=	?
Z	=	?

After Instruction

C	=	0
REG	=	0x02
WREG	=	0x50
N	=	0
OV	=	0
DC	=	0
Z	=	0

ANDLW — AND literal with WREG

Syntax:	[*label*] ANDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(WREG) .AND. k → WREG
Status Affected:	N,Z
Encoding:	`0000` `1011` `kkkk` `kkkk`
Description:	The contents of WREG are AND'ed with the 8-bit literal 'k'. The result is placed in WREG.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example: `ANDLW 0x5F`

Before Instruction

WREG	=	0xA3
N	=	?
Z	=	?

After Instruction

WREG	=	0x03
N	=	0
Z	=	0

SWAPF **Swap nibbles in f**

Syntax: [*label*] SWAPF f [,d [,a]]

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f<3:0>) → dest<7:4>,
(f<7:4>) → dest<3:0>

Status Affected: None

Encoding:

`0011`	`10da`	`ffff`	`ffff`

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, the Bank will be selected as per the BSR value.

Words: 1

Cycles: 1

Q Cycle Activity:

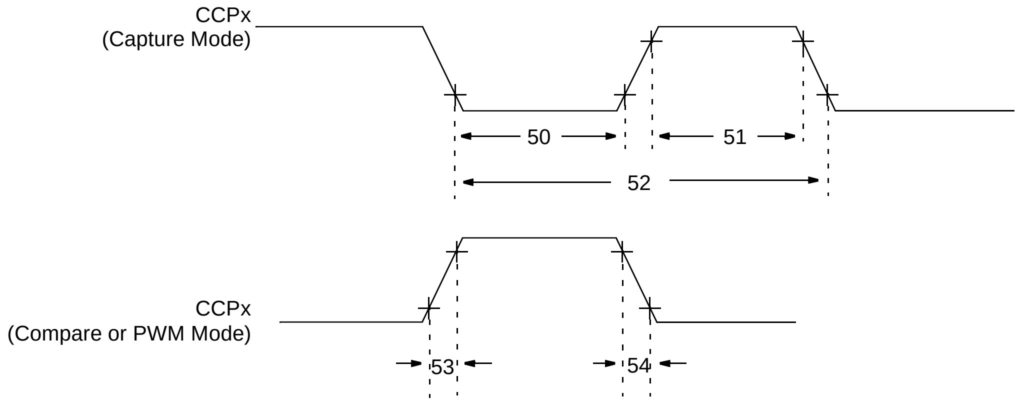
Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `SWAPF REG`

Before Instruction
REG = 0x53

After Instruction
REG = 0x35

FIGURE 25-10: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



Note: Refer to Figure 25-4 for load conditions.

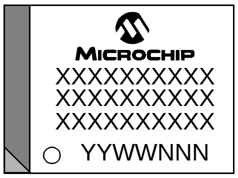
TABLE 25-9: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param. No.	Symbol	Characteristic			Min	Max	Units	Conditions
50	TccL	CCPx input low time	No Prescaler		0.5TCY + 20	—	ns	
			With Prescaler	PIC18**C**XX8	10	—	ns	
				PIC18**LC**XX8	20	—	ns	
51	TccH	CCPx input high time	No Prescaler		0.5TCY + 20	—	ns	
			With Prescaler	PIC18**C**XX8	10	—	ns	
				PIC18**LC**XX8	20	—	ns	
52	TccP	CCPx input period			$\frac{3T_{CY} + 40}{N}$	—	ns	N = prescale value (1,4 or 16)
53	TccR	CCPx output fall time		PIC18**C**XX8	—	25	ns	
				PIC18**LC**XX8	—	45	ns	
54	TccF	CCPx output fall time		PIC18**C**XX8	—	25	ns	
				PIC18**LC**XX8	—	45	ns	

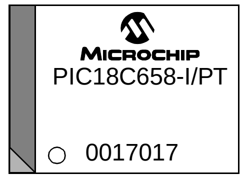
27.0 PACKAGING INFORMATION

27.1 Package Marking Information

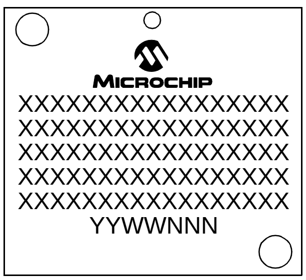
64-Lead TQFP



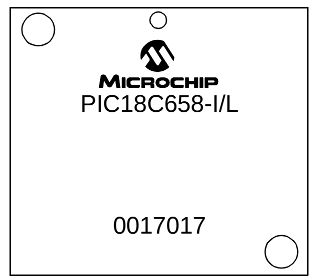
Example



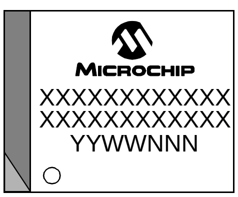
68-Lead PLCC



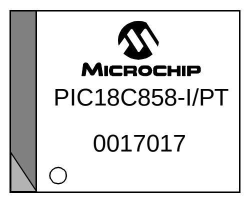
Example



80-Lead TQFP



Example

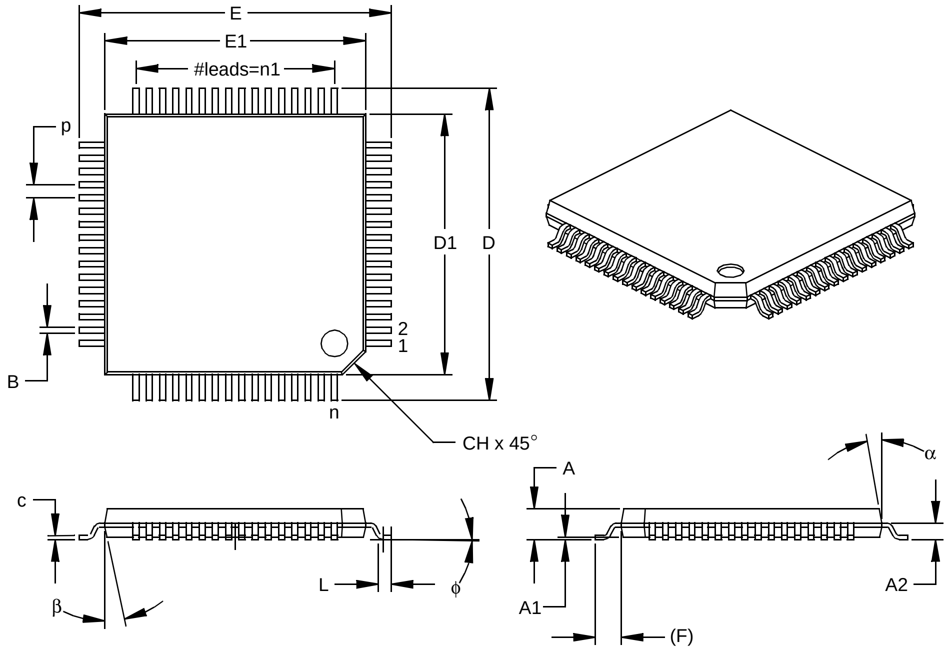


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code and traceability code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		64			64	
Pitch	p		.020			0.50	
Pins per Side	n1		16			16	
Overall Height	A	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039			1.00	
Foot Angle	φ	0	3.5	7	0	3.5	7
Overall Width	E	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	c	.005	.007	.009	0.13	0.18	0.23
Lead Width	B	.007	.009	.011	0.17	0.22	0.27
Pin 1 Corner Chamfer	CH	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-026
Drawing No. C04-085

W

X

NOTES: