Renesas Electronics America Inc - UPD78F0472GC-GAD-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0472gc-gad-ax

CHAPTER 1 OUTLINE

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.2 μs: @ 10 MHz operation with high-speed system clock) to ultra low-speed (122 μs: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM, RAM capacities

Item / Part Number	Program Memory (ROM)		Data Memory		
			Internal High-Speed RAM[Note 1]	Internal Expansion RAM[Note 1]	LCD Display RAM
μPD78F0471, 78F0481, 78F0491	Flash memory[Note 1]	16 KB	768 bytes	–	<μPD78F047x, 78F048x> 40 × 4 bits (36 × 8 bits) [36 × 4 bits (32 × 8 bits)][Note 2]
μPD78F0472, 78F0482, 78F0492		24 KB	1 KB		
μPD78F0473, 78F0483, 78F0493		32 KB			
μPD78F0474, 78F0484, 78F0494		48 KB		1 KB	<μPD78F049x> 32 × 4 bits (28 × 8 bits) [28 × 4 bits (24 × 8 bits)][Note 2]
μPD78F0475, 78F0485, 78F0495		60 KB			

Notes 1. The internal flash memory, internal high-speed RAM capacities, and internal expansion RAM capacities can be changed using the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

<R> **2.** The items in parentheses are applicable when 8com is used.
The items in square brackets are applicable when using the UART6 pins (RxD6, TxD6) on the bottom side.

- On-chip single-power-supply flash memory
- Self-programming (with boot swap function)
- On-chip debug function
- On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
- On-chip watchdog timer (operable with internal low-speed oscillation clock)
- LCD controller/driver (external resistance division and internal resistance division are switchable)

μPD78F047x: Segment signals: 36, Common signals: 8 (1/4 bias)
: Segment signals: 40, Common signals: 4 (1/3 bias)
: Segment signals: 40, Common signals: 3 (1/3, 1/2 bias)
: Segment signals: 40, Common signals: 2 (1/2 bias)
: Segment signals: 40, Common signals: 1 (Static)

μPD78F048x: Segment signals: 36, Common signals: 8 (1/4 bias)
: Segment signals: 40, Common signals: 4 (1/3 bias)
: Segment signals: 40, Common signals: 3 (1/3, 1/2 bias)
: Segment signals: 40, Common signals: 2 (1/2 bias)
: Segment signals: 40, Common signals: 1 (Static)

μPD78F049x: Segment signals: 28, Common signals: 8 (1/4 bias)
: Segment signals: 32, Common signals: 4 (1/3 bias)
: Segment signals: 32, Common signals: 3 (1/3, 1/2 bias)
: Segment signals: 32, Common signals: 2 (1/2 bias)
: Segment signals: 32, Common signals: 1 (Static)

<R> ○ On-chip segment key scan function: 8 channels
○ On-chip key interrupt function: 8 channels
○ On-chip clock output/buzzer output controller
○ I/O ports: 62
○ Timer: 9 channels
- 16-bit timer/event counter: 1 channel
- 8-bit timer/event counter: 3 channels
- 8-bit timer: 3 channels
- Real-time counter (RTC): 1 channel
- Watchdog timer: 1 channel

○ Serial interface: 3 channels
- UART (LIN (Local Interconnect Network)-bus supported): 1 channel
- CSI/UART[Note]: 1 channel
- CSI with automatic transmit/receive function: 1 channel

Note Select either of the functions of these alternate-function pins.

○ 16-bit ΔΣ type A/D converter[Note]: 3 channels (μPD78F049x only)
○ 10-bit successive approximation type A/D converter: 8 channels (μPD78F048x and 78F049x only)
○ Remote controller receiver
○ Manchester code generator
○ Power supply voltage: V_{DD} = 1.8 to 5.5 V
○ Operating ambient temperature: T_A = −40 to +85°C

Note The specifications of the 16-bit ΔΣ A/D converter may have been changed.
For details of the specifications, contact an NEC Electronics sales representative or authorized dealer.

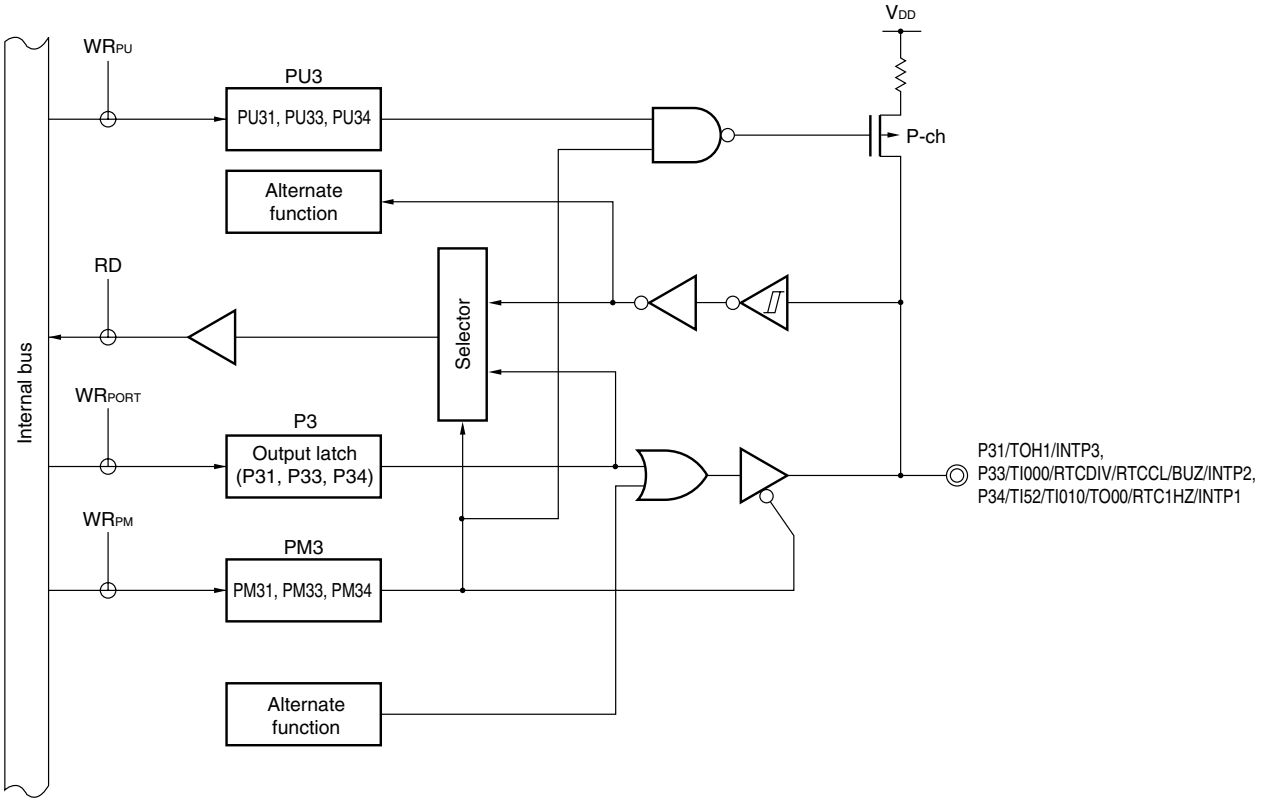
1.2 Applications

Digital cameras, AV equipments, household electrical appliances, utility meters, health care equipments, and measurement equipment, etc.

1.5 78K0/Lx3 Microcontroller Series Lineup

ROM	RAM	78K0/LC3	78K0/LD3	78K0/LE3	78K0/LF3
		48 Pins	52 Pins	64 Pins	80 Pins
60 KB	2 KB	–	–	μPD78F0465 μPD78F0455 μPD78F0445	μPD78F0495 μPD78F0485 μPD78F0475
48 KB	2 KB	–	–	μPD78F0464 μPD78F0454 μPD78F0444	μPD78F0494 μPD78F0484 μPD78F0474
32 KB	1 KB	μPD78F0413 μPD78F0403	μPD78F0433 μPD78F0423	μPD78F0463 μPD78F0453 μPD78F0443	μPD78F0493 μPD78F0483 μPD78F0473
24 KB	1 KB	μPD78F0412 μPD78F0402	μPD78F0432 μPD78F0422	μPD78F0462 μPD78F0452 μPD78F0442	μPD78F0492 μPD78F0482 μPD78F0472
16 KB	768 B	μPD78F0411 μPD78F0401	μPD78F0431 μPD78F0421	μPD78F0461 μPD78F0451 μPD78F0441	μPD78F0491 μPD78F0481 μPD78F0471
8 KB	512 B	μPD78F0410 μPD78F0400	μPD78F0430 μPD78F0420	–	–

Figure 4-10. Block Diagram of P31, P33, P34



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00

6.1 Functions of 16-Bit Timer/Event Counter 00

16-bit timer/event counter 00 has the following functions.

(1) Interval timer

16-bit timer/event counter 00 generates an interrupt request at the preset time interval.

(2) Square-wave output

16-bit timer/event counter 00 can output a square wave with any selected frequency.

(3) External event counter

16-bit timer/event counter 00 can measure the number of pulses of an externally input signal.

(4) One-shot pulse output

16-bit timer event counter 00 can output a one-shot pulse whose output pulse width can be set freely.

(5) PPG output

16-bit timer/event counter 00 can output a rectangular wave whose frequency and output pulse width can be set freely.

(6) Pulse width measurement

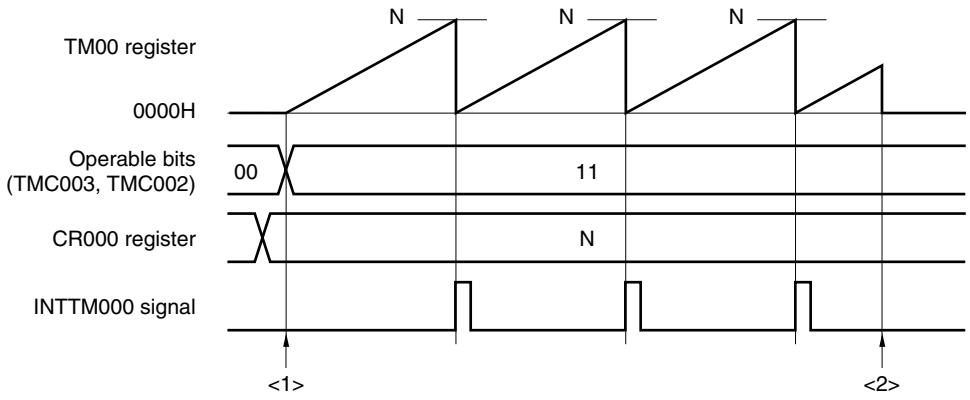
16-bit timer/event counter 00 can measure the pulse width of an externally input signal.

(7) External 24-bit event counter

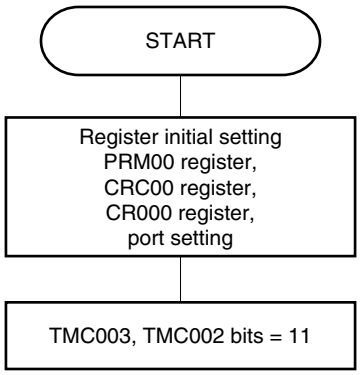
16-bit timer/event counter 00 can be operated to function as an external 24-bit event counter, by connecting 16-bit timer 00 and 8-bit timer/event counter 52 in cascade, and using the external event counter function of 8-bit timer/event counter 52.

When using it as an external 24-bit event counter, external event input gate enable can be controlled via 8-bit timer counter H2 output.

Figure 6-15. Example of Software Processing for Interval Timer Function



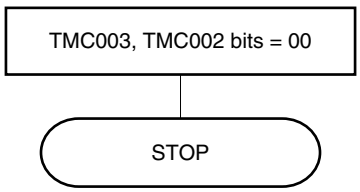
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

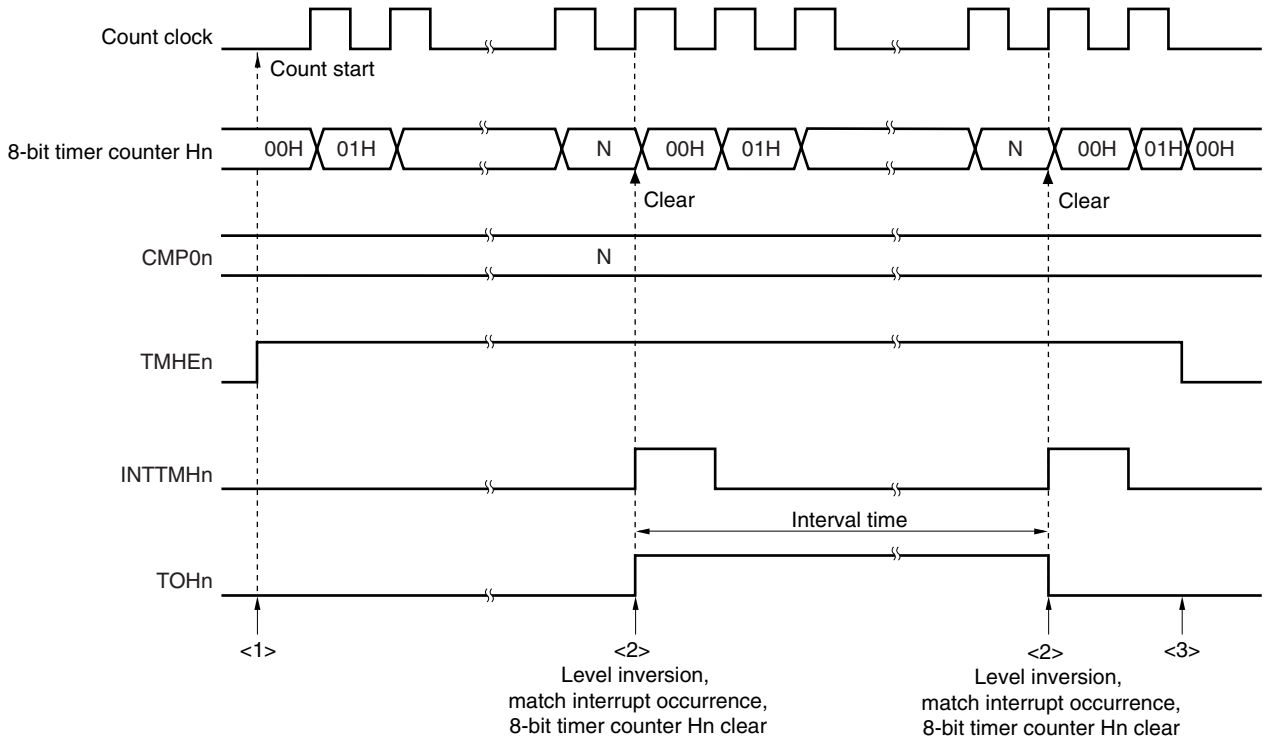
<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

Figure 8-12. Timing of Interval Timer/Square-Wave Output Operation (1/2)

(a) Basic operation (Operation When 01H ≤ CMP0n ≤ FEH)



<1> The count operation is enabled by setting the TMHEn bit to 1. The count clock starts counting no more than 1 clock after the operation is enabled.

<2> When the value of the 8-bit timer counter Hn matches the value of the CMP0n register, the value of the timer counter is cleared, and the level of the TOHn output is inverted. In addition, the INTTMHn signal is output at the rising edge of the count clock.

<3> If the TMHEn bit is cleared to 0 while timer H is operating, the INTTMHn signal and TOHn output are set to the default level. If they are already at the default level before the TMHEn bit is cleared to 0, then that level is maintained.

Remarks 1. n = 0 to 2, however, TOH0 and TOH1 only for TOHn

2. 01H ≤ N ≤ FEH

12.2 Configuration of 10-Bit Successive Approximation Type A/D Converter

The 10-bit successive approximation type A/D converter includes the following hardware.

(1) ANI0 to ANI7 pins

These are the 8-channel analog input pins of the 10-bit successive approximation type A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins or segment output pins (μPD78F048x only).

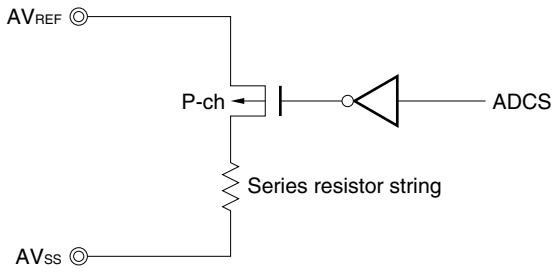
(2) Sample & hold circuit

The sample & hold circuit samples the input voltage of the analog input pin selected by the selector when A/D conversion is started, and holds the sampled voltage value during A/D conversion.

(3) Series resistor string

The series resistor string is connected between AV_{REF} and AV_{SS}, and generates a voltage to be compared with the sampled voltage value.

Figure 12-2. Circuit Configuration of Series Resistor String



(4) Voltage comparator

The voltage comparator compares the sampled voltage value and the output voltage of the series resistor string.

(5) Successive approximation register (SAR)

This register converts the result of comparison by the voltage comparator, starting from the most significant bit (MSB).

When the voltage value is converted into a digital value down to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register are transferred to the A/D conversion result register (ADCR).

(6) 10-bit A/D conversion result register (ADCR)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the A/D conversion result in its higher 10 bits (the lower 6 bits are fixed to 0).

Table 13-1. Sampling Clock (Sampling Time) Setting Conditions

ADDN2	AV_{REF} Condition	Sampling Clock: f_{VP} (Conversion Time in 16-bit Resolution)
Differential input	3.5 V ≤ AV_{REF} ≤ 5.5 V	1.25 MHz max. (52.42 ms min.)
	2.7 V ≤ AV_{REF} < 3.5 V	625 kHz max. (104.85 ms min.)
Single input	2.85 V ≤ AV_{REF} ≤ 5.5 V	625 kHz max. (104.85 ms min.)
	2.7 V ≤ AV_{REF} < 2.85 V	525 kHz max. (124.83 ms min.)

Table 13-2. Examples of Sampling Time under Setting Conditions

		Number of Times of 16-bit ΔΣ Type A/D Sampling: N (Resolution)							
f_{PRS}	f_{VP}	65536 (16-bit)	32768 (15-bit)	16384 (14-bit)	8192 (13-bit)	4096 (12-bit)	2048 (11-bit)	1024 (10-bit)	256 (8-bit)
10 MHz	$f_{PRS}/4$	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
	$f_{PRS}/8$ Note 1	52.42 ms	26.21 ms	13.10 ms	6.55 ms	3.27 ms	1.63 ms	0.81 ms	0.20 ms
	$f_{PRS}/16$ Note 2	104.85 ms	52.42 ms	26.21 ms	13.10 ms	6.55 ms	3.27 ms	1.63 ms	0.41 ms
8 MHz	$f_{PRS}/4$	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
	$f_{PRS}/8$ Note 1	65.53 ms	32.76 ms	16.38 ms	8.19 ms	4.09 ms	2.04 ms	1.02 ms	0.25 ms
	$f_{PRS}/16$	131.07 ms	65.53 ms	32.76 ms	16.38 ms	8.19 ms	4.09 ms	2.04 ms	0.51 ms
5 MHz	$f_{PRS}/4$ Note 1	52.42 ms	26.21 ms	13.10 ms	6.55 ms	3.27 ms	1.63 ms	0.81 ms	0.40 ms
	$f_{PRS}/8$ Note 2	104.85 ms	52.42 ms	26.21 ms	13.10 ms	6.55 ms	3.27 ms	1.63 ms	0.81 ms
	$f_{PRS}/16$	209.71 ms	104.85 ms	52.42 ms	26.21 ms	13.10 ms	6.55 ms	3.27 ms	1.63 ms
4 MHz	$f_{PRS}/4$ Note 1	65.53 ms	32.76 ms	16.38 ms	8.19 ms	4.09 ms	2.04 ms	1.02 ms	0.25 ms
	$f_{PRS}/8$	131.07 ms	65.53 ms	32.76 ms	16.38 ms	8.19 ms	4.09 ms	2.04 ms	0.51 ms
	$f_{PRS}/16$	262.14 ms	131.07 ms	65.53 ms	32.76 ms	16.38 ms	8.19 ms	4.09 ms	1.02 ms
2 MHz	$f_{PRS}/4$	131.07 ms	65.53 ms	32.76 ms	16.38 ms	8.19 ms	4.09 ms	2.04 ms	0.51 ms
	$f_{PRS}/8$	262.14 ms	131.07 ms	65.53 ms	32.76 ms	16.38 ms	8.19 ms	4.09 ms	1.02 ms
	$f_{PRS}/16$	524.28 ms	262.14 ms	131.07 ms	65.53 ms	32.76 ms	16.38 ms	8.19 ms	2.04 ms
–	$f_{SUB}/2$	4 s	2 s	1 s	500 ms	250 ms	125 ms	62.5 ms	15.62 ms

Notes 1. Setting the differential input mode (2.7 V ≤ AV_{REF} < 3.5 V) and single input mode is prohibited since the sampling time conditions are not satisfied in these modes.

2. Setting the single input mode (2.7 V ≤ AV_{REF} < 2.85 V) is prohibited since the sampling time conditions are not satisfied in this modes.

Figure 16-6. Timing in 3-Wire Serial I/O Mode (2/2)

(b) Transmission/reception timing (Type 2: TRMD10 = 1, DIR10 = 0, CKP10 = 0, DAP10 = 1)

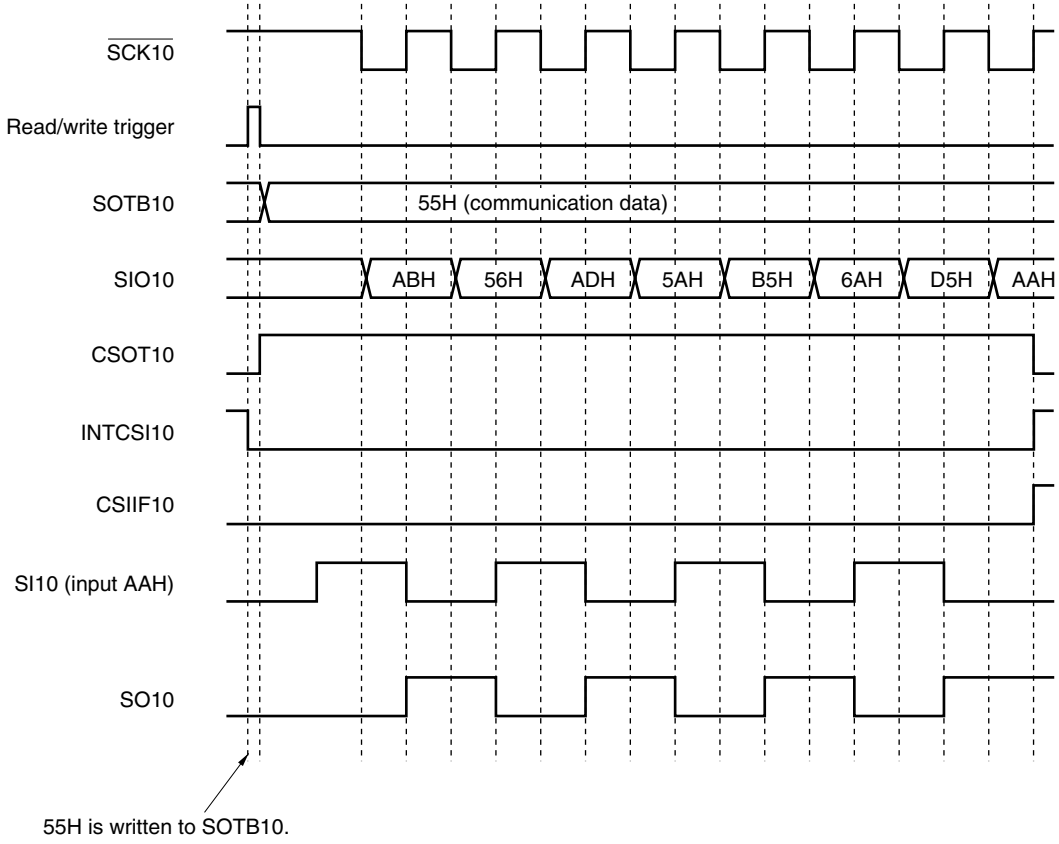
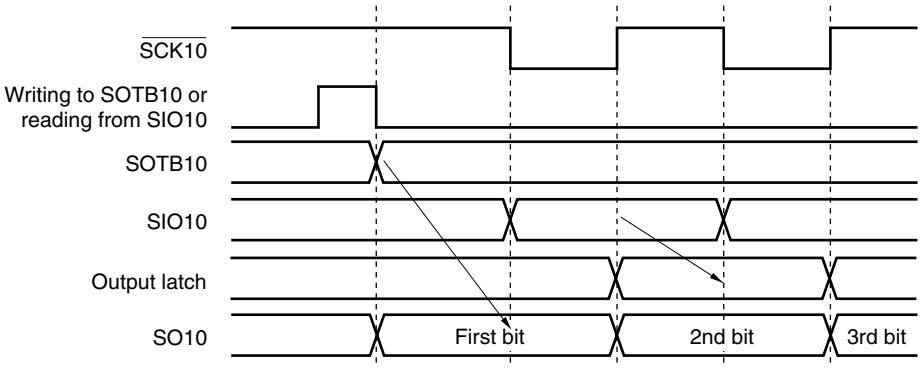
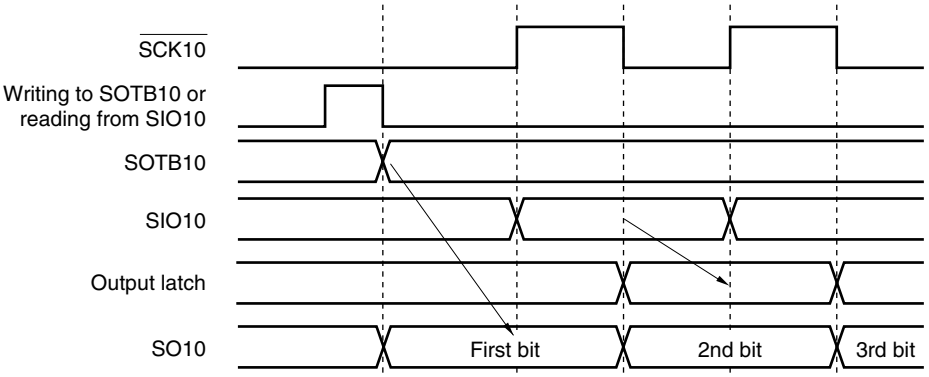


Figure 16-8. Output Operation of First Bit (2/2)

(c) Type 2: CKP10 = 0, DAP10 = 1



(d) Type 4: CKP10 = 1, DAP10 = 1

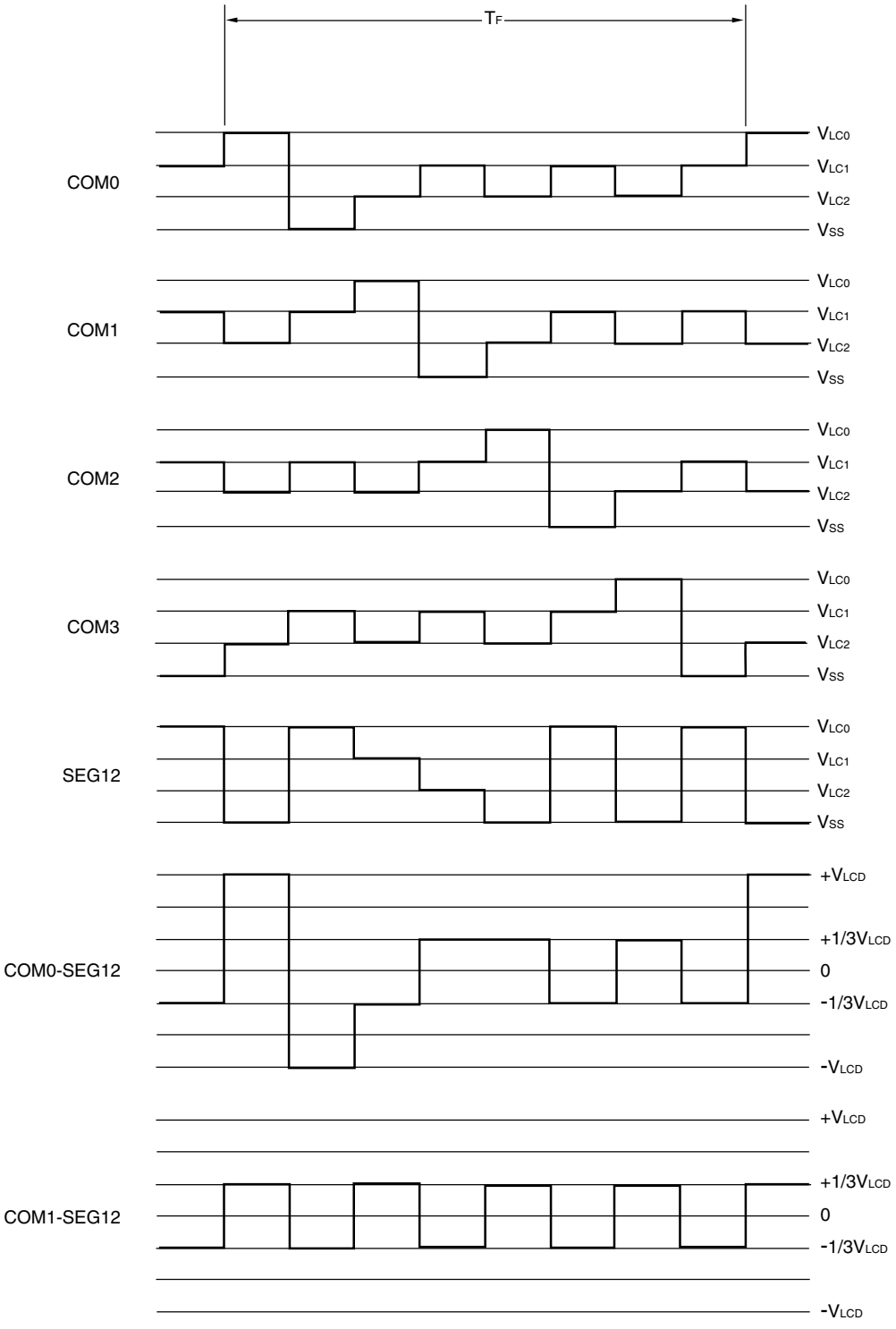


The first bit is directly latched by the SOTB10 register at the falling edge of the write signal of the SOTB10 register or the read signal of the SIO10 register, and output from the SO10 pin via an output selector. Then, the value of the SOTB10 register is transferred to the SIO10 register at the next falling (or rising) edge of $\overline{\text{SCK10}}$, and shifted one bit. At the same time, the first bit of the receive data is stored in the SIO10 register via the SI10 pin.

The second and subsequent bits are latched by the SIO10 register to the output latch at the next rising (or falling) edge of $\overline{\text{SCK10}}$, and the data is output from the SO10 pin.

Figure 18-29. Four-Time-Slice LCD Drive Waveform Examples (1/3 Bias Method)

(a) When segment key scan function is not used (KSON = 0)



Remark The waveforms for COM2 to SEG12 and COM3 to SEG12 are omitted.

19.3 Registers Controlling Manchester Code Generator

The following six types of registers are used to control the Manchester code generator.

- MCG control register 0 (MC0CTL0)
- MCG control register 1 (MC0CTL1)
- MCG control register 2 (MC0CTL2)
- MCG status register (MC0STR)
- Port mode register 3 (PM3)
- Port register 3 (P3)

(1) MCG control register 0 (MC0CTL0)

This register is used to set the operation mode and to enable/disable the operation.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 19-4. Format of MCG Control Register 0 (MC0CTL0)

Address: FF4CH After reset: 10H R/W

Symbol	<7>	6	5	<4>	3	2	<1>	<0>
MC0CTL0	MC0PWR	0	0	MC0DIR	0	0	MC0OSL	MC0OLV

MC0PWR	Operation control
0	Operation stopped
1	Operation enabled

MC0DIR	First bit specification
0	MSB
1	LSB

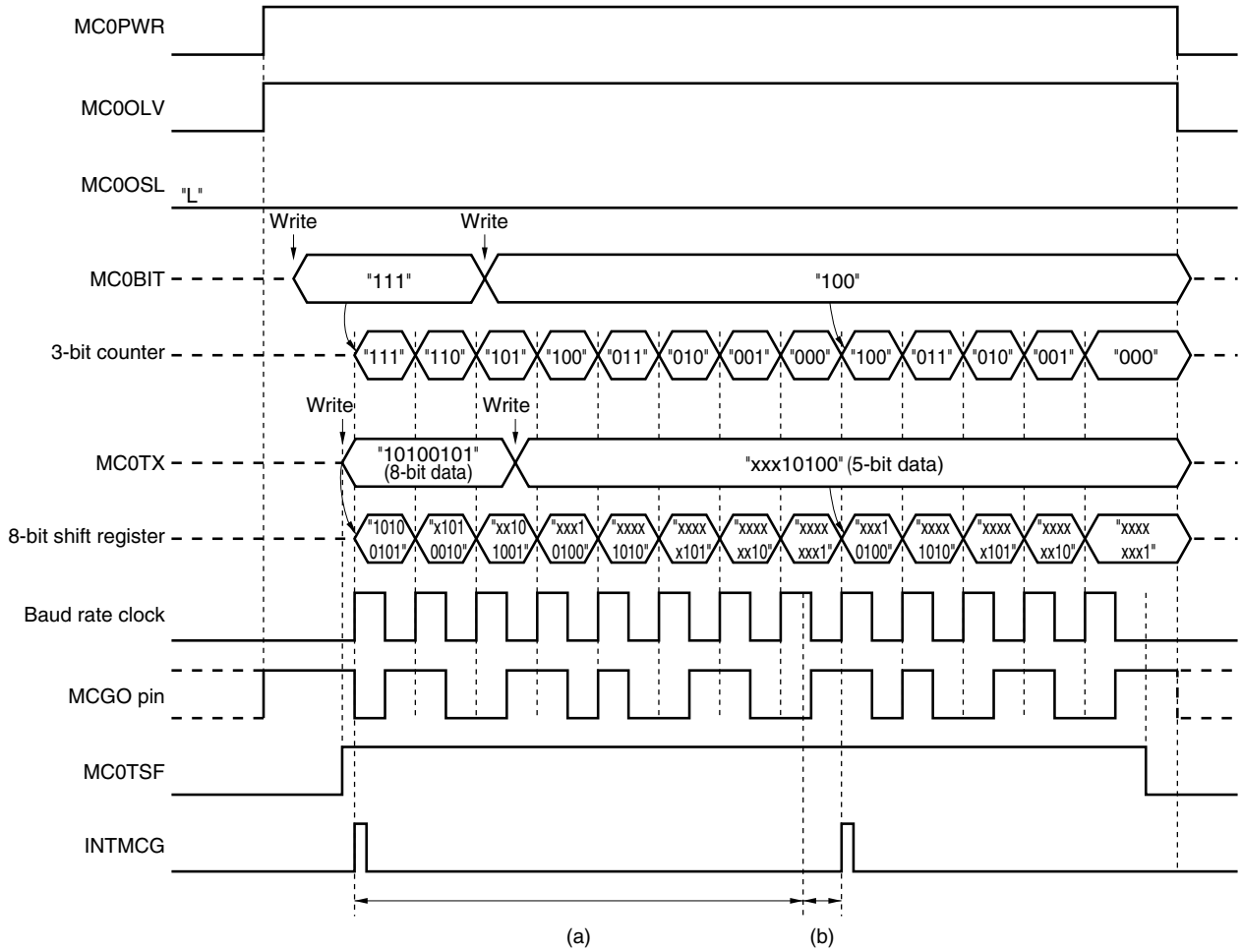
MC0OSL	Data format
0	Manchester code
1	Bit sequential data

MC0OLV	Output level when transmission suspended
0	Low level
1	High level

Caution Clear (0) the MC0PWR bit before rewriting the MC0DIR, MC0OSL, and MC0OLV bits (it is possible to rewrite these bits by an 8-bit memory manipulation instruction at the same time when the MC0PWR bit is set (1)).

Figure 19-8. Timing of Manchester Code Generator Mode (LSB First) (3/4)

(3) Transmit timing (MC0OLV = 1, total transmit bit length = 13 bits)



(a): "8-bit transfer period" – (b)

(b): "1/2 cycle of baud rate" + 1 clock (f_{XCLK}) before the last bit of transmit data

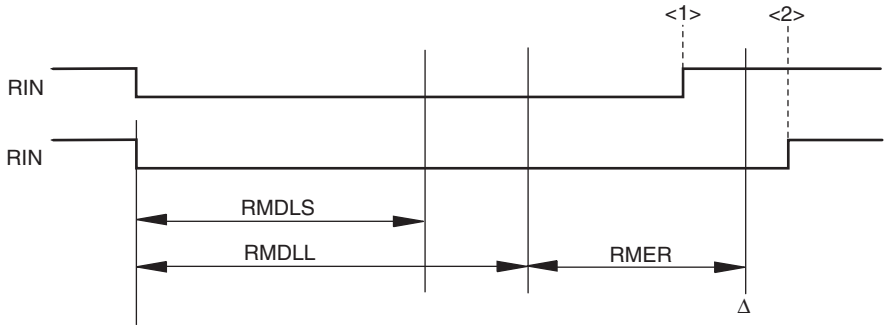
f_{XCLK}: Frequency of the operation base clock selected by using the MC0CKS2 to MC0CKS0 bits of the MC0CTL1 register

Last bit: Transfer bit when 3-bit counter = 000

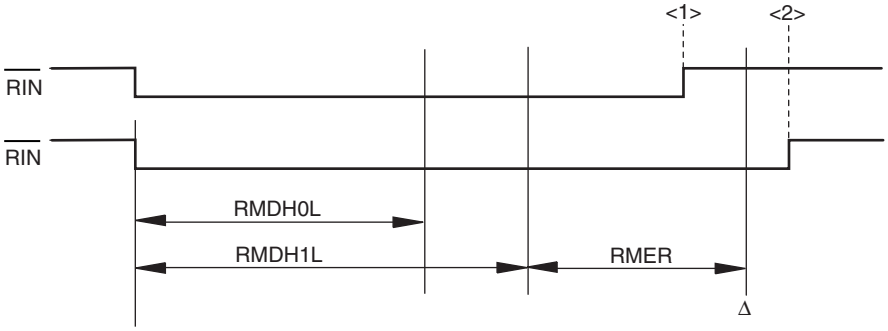
Caution Writing the next transmit data to MC0TX must be complete within the period (a) during continuous transmission. If writing the next transmit data to MC0TX is executed in the period (b), the next data transmission starts 2 clocks (f_{XCLK}) after the last bit has been transmitted. Rewrite the MC0BIT before writing to MC0TX during continuous transmission.

(5) End width determination

(a) Type A reception mode



(b) Type B, Type C reception modes



Relationship Between RMER/Counter	Position of Waveform	Corresponding Operation
Counter < RMER	<1>: Short	Error interrupt INTRERR is generated[Note]. Measuring the guide pulse high-level width is started.
RMER ≤ counter	<2>: Long	INTREND is generated at the Δ point[Note]. Reception via circuit stops until RMSR is read.

Note In type C reception mode, before the first INTDFULL interrupt is generated, INTRERR and INTREND will not be generated. However, RMSR and RMSCR will be cleared.

21.4.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 21-5 shows relationship between interrupt requests enabled for multiple interrupt servicing and Figure 21-10 shows multiple interrupt servicing examples.

Table 21-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request				Software Interrupt Request
		PR = 0		PR = 1		
		IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP = 0	○	×	×	×	○
	ISP = 1	○	×	○	×	○
Software interrupt		○	×	○	×	○

Remarks 1. ○: Multiple interrupt servicing enabled

2. ×: Multiple interrupt servicing disabled

3. ISP and IE are flags contained in the PSW.

ISP = 0: An interrupt with higher priority is being serviced.

ISP = 1: No interrupt request has been acknowledged, or an interrupt with a lower priority is being serviced.

IE = 0: Interrupt request acknowledgment is disabled.

IE = 1: Interrupt request acknowledgment is enabled.

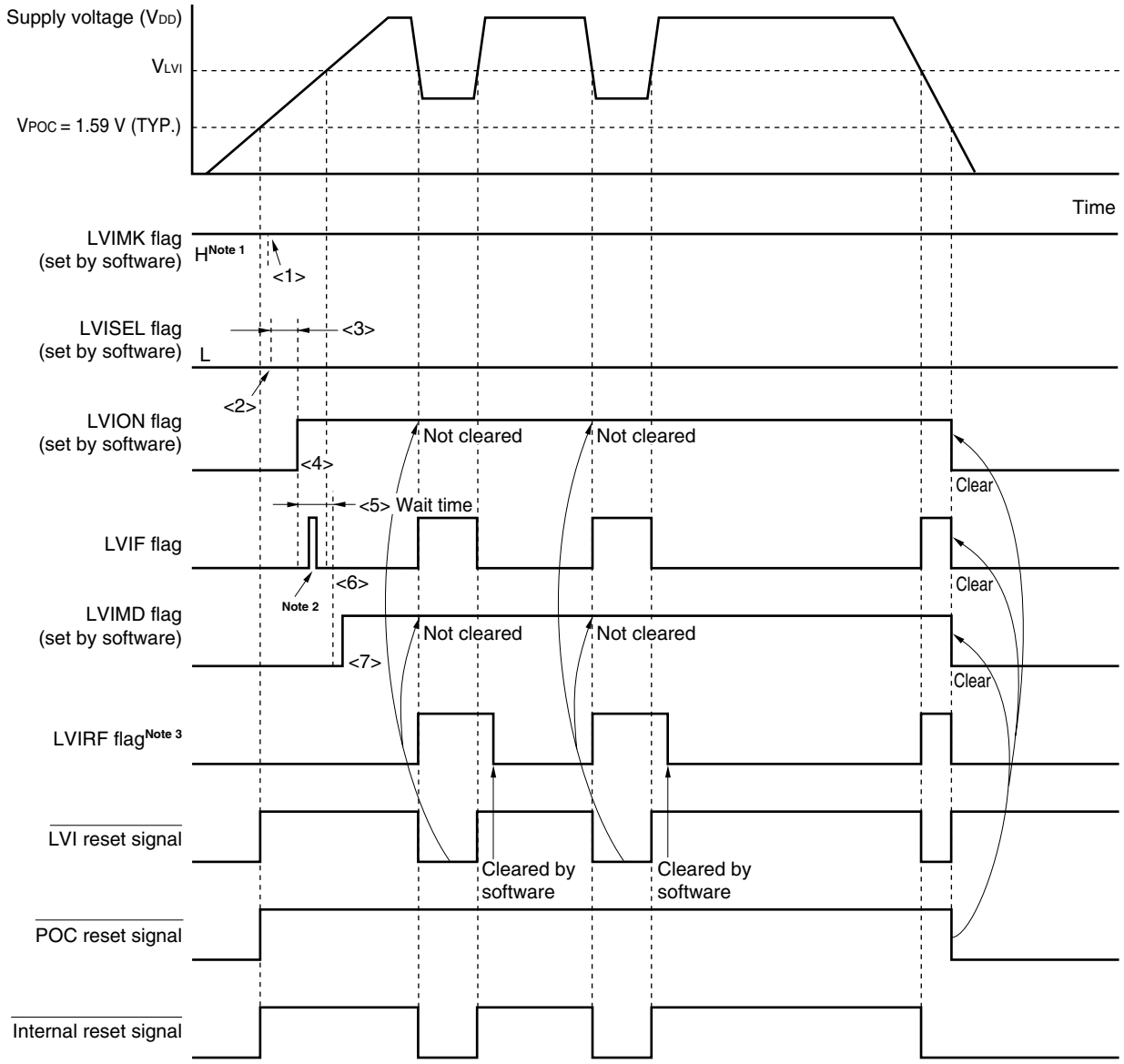
4. PR is a flag contained in PR0L, PR0H, PR1L, and PR1H.

PR = 0: Higher priority level

PR = 1: Lower priority level

Figure 26-5. Timing of Low-Voltage Detector Internal Reset Signal Generation (Detects Level of Supply Voltage (V_{DD})) (1/2)

(1) In 1.59 V POC mode (option byte: POCMODE = 0)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The LVIF flag may be set (1).

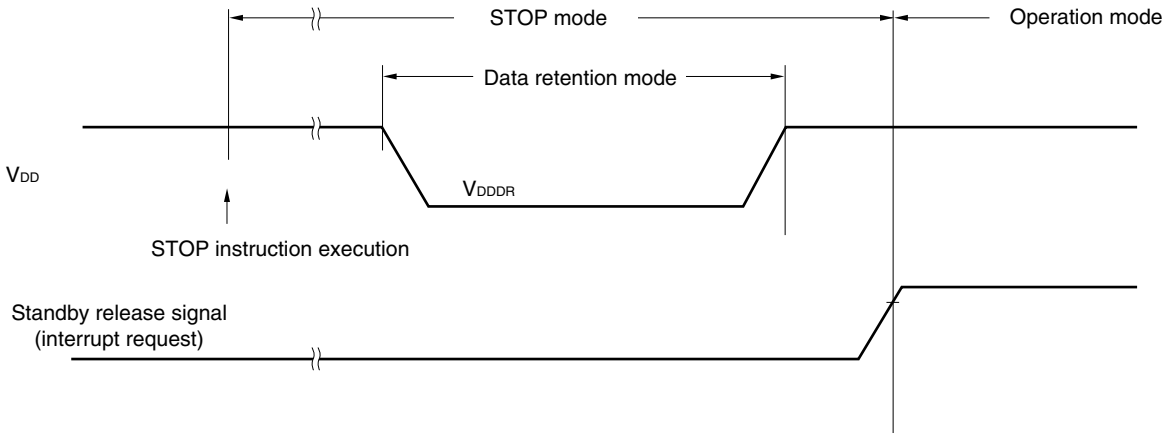
3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, see **CHAPTER 24 RESET FUNCTION**.

Remark <1> to <7> in Figure 26-5 above correspond to <1> to <7> in the description of "When starting operation" in **26.4.1 (1) When detecting level of supply voltage (V_{DD})**.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

• Basic characteristics

Parameter		Symbol	Conditions			MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}					4.5	11.0	mA
Erase time[Note 1, 2]	All block	T_{eraca}					20	200	ms
	Block unit	T_{erasa}					20	200	ms
Write time (in 8-bit units)[Note 1]		T_{wrwa}					10	100	μs
<R> Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite[Note 3]	When a flash memory programmer is used, and the libraries provided by NEC Electronics are used	Retention: 15 years	1000			Times
				When the EEPROM emulation libraries provided by NEC Electronics are used, and the rewritable ROM size is 4 KB	Retention: 3 years[Note 4]	10000			Times

<R> **Notes 1.** Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP5, is used and the rewrite time during self programming, see **Tables 28-12** and **28-13**.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

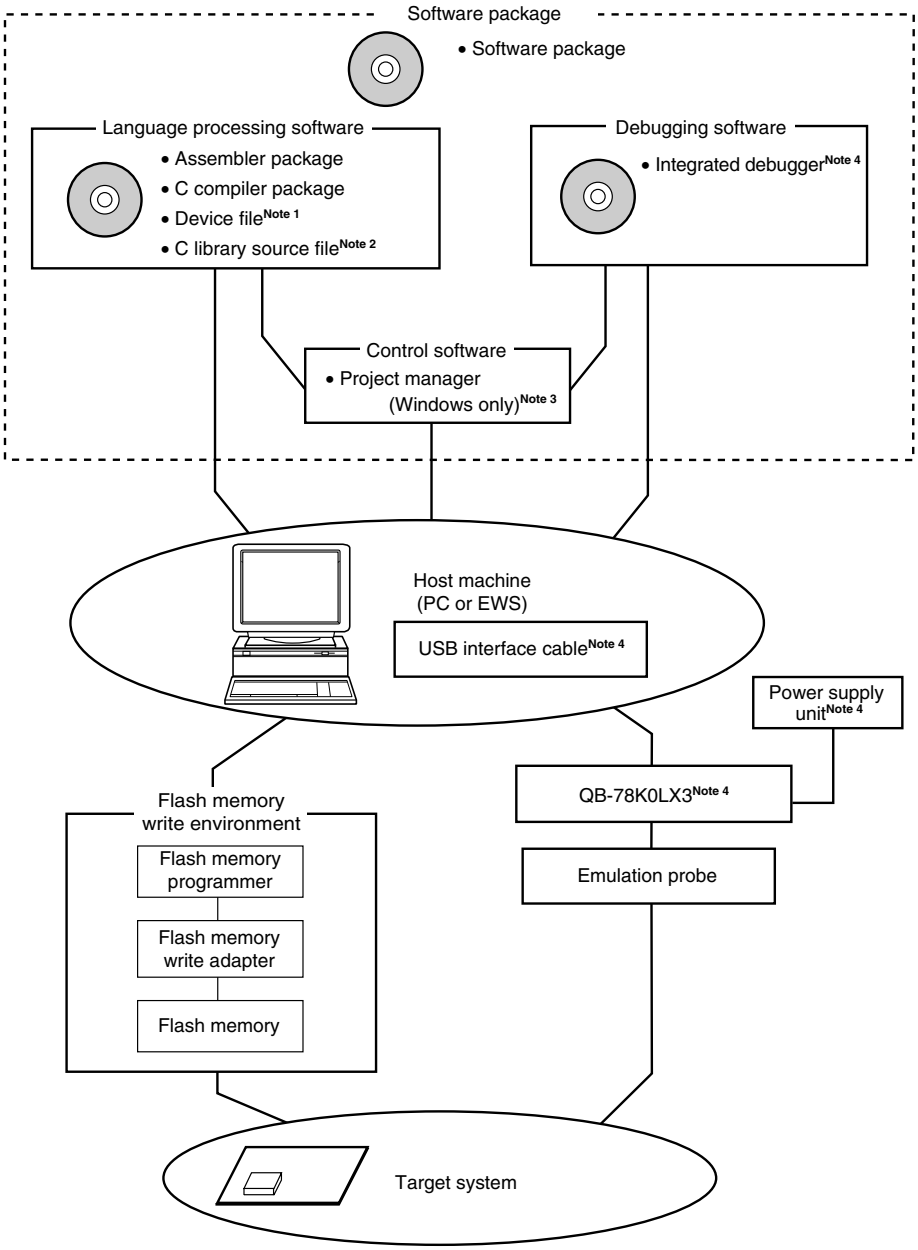
3. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

<R> **4.** Data retention is guaranteed for three years after data has been written. If rewriting has been performed, data retention is guaranteed for another three years thereafter.

Remark f_{XP}: Main system clock oscillation frequency

Figure A-1. Development Tool Configuration (1/2)

(1) When using the in-circuit emulator QB-78K0LX3



Notes 1. Download the device file (DF780495) for the 78K0/LF3 from the download site for development tools (http://www.necel.com/micro/ods/eng/index.html).

2. The C library source file is not included in the software package.

3. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

4. The QB-78K0LX3 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, a power supply unit, the on-chip debug emulator QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board. Any other products are sold separately.
Download the software for operating the QB-MINI2 from the download site for development tools (http://www.necel.com/micro/ods/eng/index.html) when using the QB-MINI2.

A.1 Software Package

SP78K0 78K0 microcontroller software package	Development tools (software) common to the 78K0 microcontrollers are combined in this package.
	Part number: μS××××SP78K0

Remark ×××× in the part number differs depending on the host machine and OS used.

μS××××SP78K0

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	

A.2 Language Processing Software

RA78K0 Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (DF780495) (sold separately). **<Precaution when using RA78K0 in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (included in assembler package) on Windows.
	Part number: μS××××RA78K0
CC78K0 C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file (both sold separately). **<Precaution when using CC78K0 in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (included in assembler package) on Windows.
	Part number: μS××××CC78K0
DF780495 [Note 1] Device file	This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0, CC78K0, and ID78K0-QB) (all sold separately). The corresponding OS and host machine differ depending on the tool to be used.
	Part number: μS××××DF780495
CC78K0-L [Note 2] C library source file	This is a source file of the functions that configure the object library included in the C compiler package. This file is required to match the object library included in the C compiler package to the user's specifications.
	Part number: μS××××CC78K0-L

Notes 1. The DF780495 can be used in common with the RA78K0, CC78K0, and ID78K0-QB. Download the DF780495 from the download site for development tools (http://www.necel.com/micro/ods/eng/index.html).

2. The CC78K0-L is not included in the software package (SP78K0).