Renesas Electronics America Inc - UPD78F0472GK-GAK-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0472gk-gak-ax

[MEMO]

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-2 shows the types of pin I/O circuits and the recommended connections of unused pins.
See **Figure 2-1** for the configuration of the I/O circuit of each type.

Table 2-2. Pin I/O Circuit Types (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P10/PCL	5-AG	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P11/$\overline{SCK10}$	5-AH		
P12/SI10/RxD0			
P13/SO10/TxD0			
P14/$\overline{SCKA0}$/INTP4			
P15/SIA0/<RxD6>			
P16/SOA0/<TxD6>	5-AG		
P17			
P20/SEG39/ANI0/DS0- to P27/SEG32/ANI7/REF+ Notes 1, 2, 3, 4	17-R		<Analog setting> Connect to AV_{REF} or AV_{SS}. <Digital setting> Input: Independently connect to AV_{REF} or AV_{SS} via a resistor.[Note 5] Output: Leave open. <Segment setting> Leave open.
P30/INTP5	5-AH		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P31/TOH1/INTP3			
P32/TOH0/MCGO	5-AG		
P33/TI000/RTCDIV/ RTCCL/BUZ/INTP2	5-AH		
P34/TI52/TI010/TO00/ RTC1HZ/INTP1			
P40/V_{LC3}/KR0	5-AO		
P41/RIN/KR1	5-AH		
P42/KR2			
P43/TO51/TI51/KR3			
P44/TO50/TI50/KR4			
P45/KR5 to P47/KR7			
P80/SEG4 to P83/SEG7	17-P		<Port setting> Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open. <Segment setting> Leave open.
P90/SEG8 to P93/SEG11			
P100/SEG12 to P103/SEG15			

Notes 1. SEGx is provided to the μPD78F047x and 78F048x only.

2. ANIx is provided to the μPD78F048x and 78F049x only.

3. DSx and REFx are provided to the 78F049x only.

4. P20/SEG39/ANI0/DS0- to P27/SEG32/ANI7/REF+ are set in the digital input mode after release of reset.

5. With μPD78F047x, independently connect to V_{DD} or V_{SS} via a resistor.

Remark The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

(3) Internal low-speed oscillation clock (clock for watchdog timer)

- **Internal low-speed oscillator**

  This circuit oscillates a clock of f_{RL} = 240 kHz (TYP.). After a reset release, the internal low-speed oscillation clock always starts operating.

  Oscillation can be stopped by using the internal oscillation mode register (RCM) when "internal low-speed oscillator can be stopped by software" is set by option byte.

  The internal low-speed oscillation clock cannot be used as the CPU clock. The following hardware operates with the internal low-speed oscillation clock.

  - Watchdog timer
  - 8-bit timer H1 (if f_{RL}, $f_{RL}/2^7$ or $f_{RL}/2^9$ is selected as the count clock)
  - LCD controller/driver (if $f_{RL}/2^3$ is selected as the LCD source clock)

Remark f_{RL}: Internal low-speed oscillation clock frequency

5.2 Configuration of Clock Generator

The clock generator includes the following hardware.

Table 5-1. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode select register (OSCCTL) Processor clock control register (PCC) Internal oscillation mode register (RCM) Main OSC control register (MOC) Main clock mode register (MCM) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) Internal high-speed oscillation trimming register (HIOTRM)
Oscillators	X1 oscillator XT1 oscillator Internal high-speed oscillator Internal low-speed oscillator

(6) Main clock mode register (MCM)

This register selects the main system clock supplied to CPU clock and clock supplied to peripheral hardware clock.

MCM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 5-6. Format of Main Clock Mode Register (MCM)

Address: FFA1H After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	<2>	<1>	<0>
MCM	0	0	0	0	0	XSEL	MCS	MCM0

XSEL	MCM0	Selection of clock supplied to main system clock and peripheral hardware	
		Main system clock (f_{XP})	Peripheral hardware clock (f_{PRS})
0	0	Internal high-speed oscillation clock (f_{RH})	Internal high-speed oscillation clock (f_{RH})
0	1		
1	0		High-speed system clock (f_{XH})
1	1	High-speed system clock (f_{XH})	

MCS	Main system clock status
0	Operates with internal high-speed oscillation clock
1	Operates with high-speed system clock

Note Bit 1 is read-only.

Cautions 1. XSEL can be changed only once after a reset release.

2. A clock other than f_{PRS} is supplied to the following peripheral functions regardless of the setting of XSEL and MCM0.

- **Watchdog timer (operates with internal low-speed oscillation clock)**
- **When "f_{RL}", "$f_{RL}/2^7$", or "$f_{RL}/2^9$" is selected as the count clock for 8-bit timer H1 (operates with internal low-speed oscillation clock)**
- **When "$f_{RL}/2^3$" is selected as the LCD source clock for LCD controller/driver (operates with internal low-speed oscillation clock)**
- **Peripheral hardware selects the external clock as the clock source (Except when the external count clock of TM00 is selected (TI000 pin valid edge))**

Figure 6-8. Format of 16-Bit Timer Output Control Register 00 (TOC00)

Address: FFBDH After reset: 00H R/W

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

OSPT00	One-shot pulse output trigger via software
0	–
1	One-shot pulse output
The value of this bit is always “0” when it is read. Do not set this bit to 1 in a mode other than the one-shot pulse output mode. If it is set to 1, TM00 is cleared and started.	

OSPE00	One-shot pulse output operation control
0	Successive pulse output
1	One-shot pulse output
One-shot pulse output operates correctly in the free-running timer mode or clear & start mode entered by TI000 pin valid edge input. The one-shot pulse cannot be output in the clear & start mode entered upon a match between TM00 and CR000.	

TOC004	TO00 output control on match between CR010 and TM00
0	Disables inversion operation
1	Enables inversion operation
The interrupt signal (INTTM010) is generated even when TOC004 = 0.	

LVS00	LVR00	Setting of TO00 pin output status
0	0	No change
0	1	Initial value of TO00 output is low level (TO00 output is cleared to 0).
1	0	Initial value of TO00 output is high level (TO00 output is set to 1).
1	1	Setting prohibited

- LVS00 and LVR00 can be used to set the initial value of the TO00 output level. If the initial value does not have to be set, leave LVS00 and LVR00 as 00.
- Be sure to set LVS00 and LVR00 when TOE00 = 1.
  LVS00, LVR00, and TOE00 being simultaneously set to 1 is prohibited.
- LVS00 and LVR00 are trigger bits. By setting these bits to 1, the initial value of the TO00 output level can be set. Even if these bits are cleared to 0, TO00 output is not affected.
- The values of LVS00 and LVR00 are always 0 when they are read.
- For how to set LVS00 and LVR00, see **6.5.2 Setting LVS00 and LVR00**.
- The actual TO00/TI010/P34/TI52/RTC1HZ/INTP1 pin output is determined depending on PM34 and P34, besides TO00 output.

TOC001	TO00 output control on match between CR000 and TM00
0	Disables inversion operation
1	Enables inversion operation
The interrupt signal (INTTM000) is generated even when TOC001 = 0.	

TOE00	TO00 output control
0	Disables output (TO00 output fixed to low level)
1	Enables output

6.4.4 Operation in clear & start mode entered by TI000 pin valid edge input

When bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 10 (clear & start mode entered by the TI000 pin valid edge input) and the count clock (set by PRM00) is supplied to the timer/event counter, TM00 starts counting up. When the valid edge of the TI000 pin is detected during the counting operation, TM00 is cleared to 0000H and starts counting up again. If the valid edge of the TI000 pin is not detected, TM00 overflows and continues counting.

The valid edge of the TI000 pin is a cause to clear TM00. Starting the counter is not controlled immediately after the start of the operation.

CR000 and CR010 are used as compare registers and capture registers.

(a) When CR000 and CR010 are used as compare registers

Signals INTTM000 and INTTM010 are generated when the value of TM00 matches the value of CR000 and CR010.

(b) When CR000 and CR010 are used as capture registers

The count value of TM00 is captured to CR000 and the INTTM000 signal is generated when the valid edge is input to the TI010 pin (or when the phase reverse to that of the valid edge is input to the TI000 pin).

When the valid edge is input to the TI000 pin, the count value of TM00 is captured to CR010 and the INTTM010 signal is generated. As soon as the count value has been captured, the counter is cleared to 0000H.

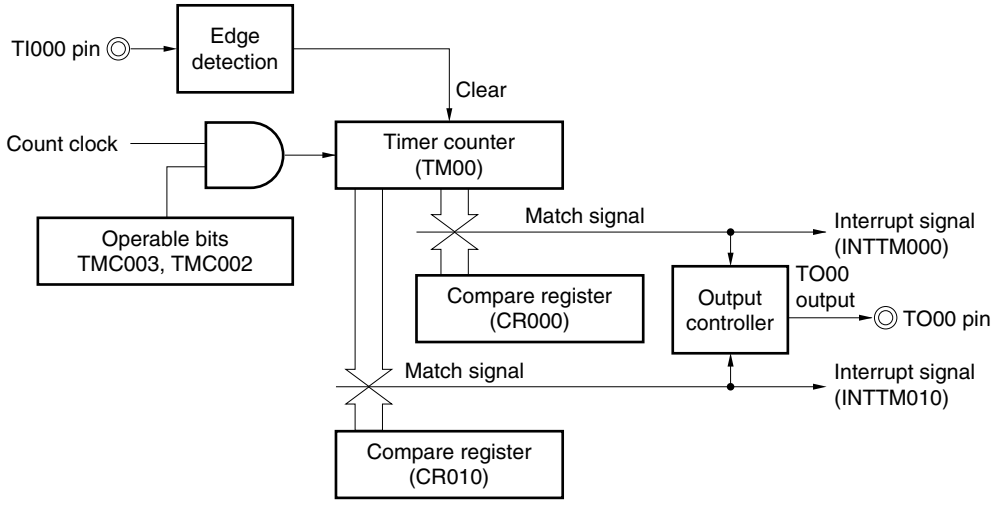
Caution Do not set the count clock as the valid edge of the TI000 pin (PRM002, PRM001, and PRM000 = 110). When PRM002, PRM001, and PRM000 = 110, TM00 is cleared.

Remarks 1. For the setting of the I/O pins, see **6.3 (6) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

(1) Operation in clear & start mode entered by TI000 pin valid edge input (CR000: compare register, CR010: compare register)

Figure 6-23. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Compare Register)



6.4.9 External 24-bit event counter operation

16-bit timer/event counter 00 can be operated to function as an external 24-bit event counter, by connecting 16-bit timer/event counter 00 and 8-bit timer/event counter 52 in cascade, and using the external event counter function of 8-bit timer/event counter 52.

It operates as an external 24-bit event counter, by counting the number of external clock pulses input to the TI52 pin via 8-bit timer counter 52 (TM52), and counting the signal which has been output upon a match between the TM52 count value and 8-bit timer compare register 52 (CR52 = FFH[Note]) via 16-bit timer counter 00 (TM00).

When using 16-bit timer/event counter 00 as an external 24-bit event counter, external event input enable can be controlled via 8-bit timer counter H2 output.

The valid edge of the input to the TI52 pin can be specified by timer clock selection register 52 (TCL52) of 8-bit timer counter 52 (TM52). Also, input enable for TM52 external event input can be controlled via 8-bit timer counter H2 output, by setting bit 2 (ISC2) of the input switch control register (ISC) to “1”.

Count operation using 8-bit timer 52 output as the count clock is started, by setting bits 2, 1, and 0 (PRM002, PRM001, and PRM000) of prescaler mode register 00 (PRM00) of 16-bit timer/event counter 00 to “1”, “1”, and “1” (TM52 output is selected as a count clock), and bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) to “1” and “1” (count clear & start mode entered upon a match between TM00 and CR000). TM00 is cleared to “0” and an interrupt request signal (INTTM000) is generated upon a match between the TM00 count value and 16-bit timer compare register 000 (CR000) value.

Subsequently, INTTM000 is generated upon every match between the TM00 and CR000 values.

Note When operating 16-bit timer/event counter 00 as an external 24-bit event counter, the 8-bit timer compare register 52 (CR52) value must be set to FFH. Also, the TM52 interrupt request signal (INTTM52) must be masked (TMMK52 = 1).

Figure 6-54. Configuration Diagram of External 24-bit Event Counter

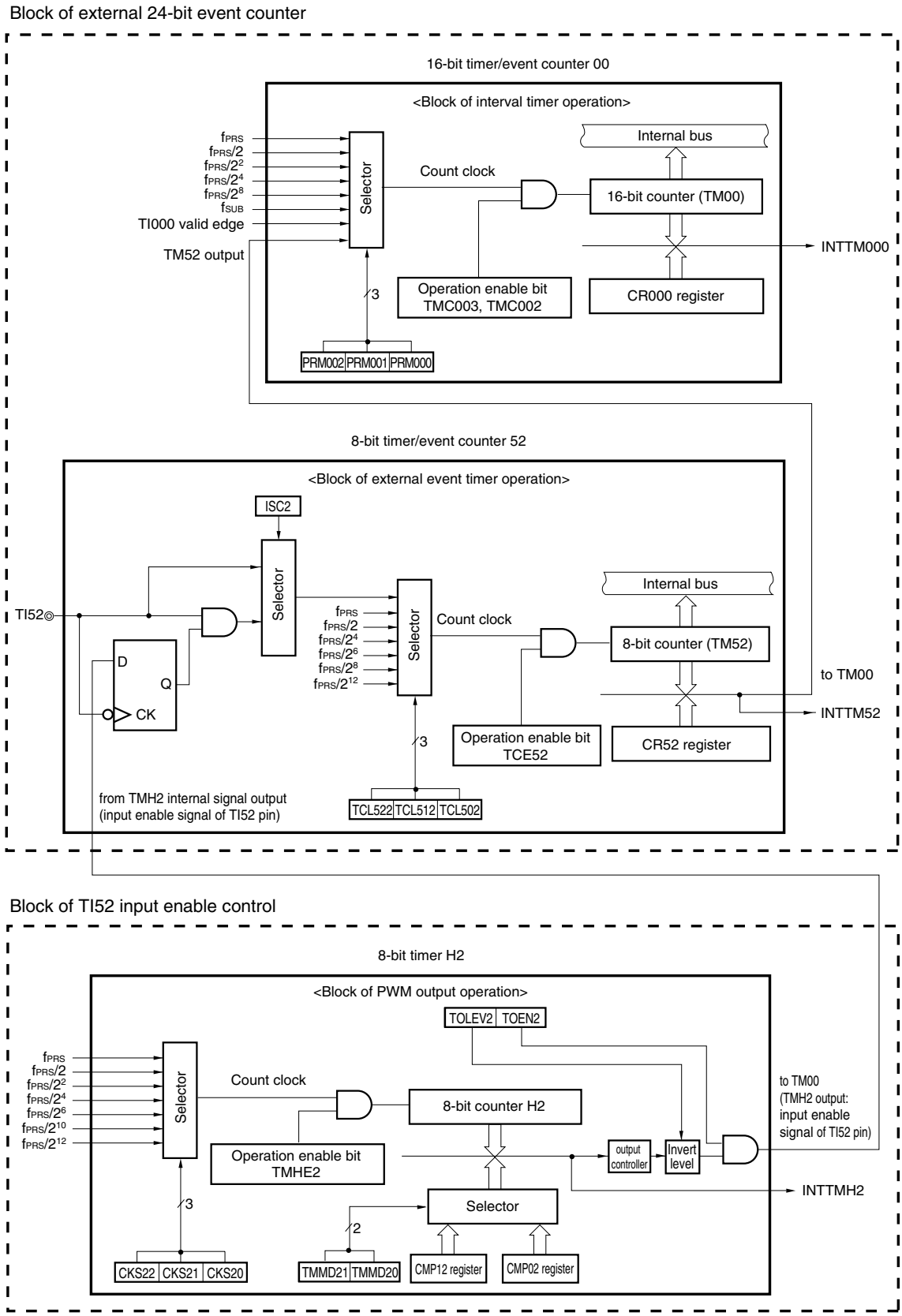
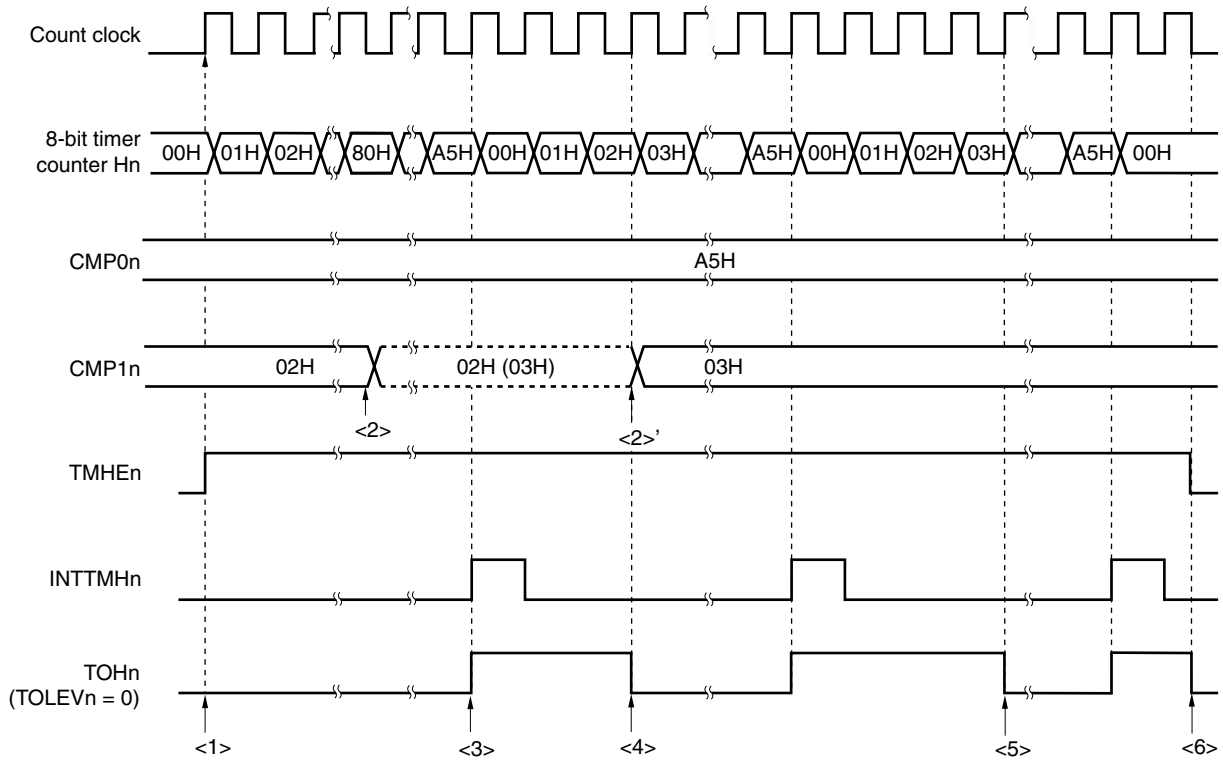


Figure 8-14. Operation Timing in PWM Output Mode (4/4)

(e) Operation by changing CMP1n (CMP1n = 02H → 03H, CMP0n = A5H)



<1> The count operation is enabled by setting TMHEn = 1. Start 8-bit timer counter Hn by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> The CMP1n register value can be changed during timer counter operation. This operation is asynchronous to the count clock.

<3> When the values of 8-bit timer counter Hn and the CMP0n register match, the value of 8-bit timer counter Hn is cleared, an active level is output, and the INTTMHn signal is output.

<4> If the CMP1n register value is changed, the value is latched and not transferred to the register. When the values of the 8-bit timer counter Hn and the CMP1n register before the change match, the value is transferred to the CMP1n register and the CMP1n register value is changed (<2>').

However, three count clocks or more are required from when the CMP1n register value is changed to when the value is transferred to the register. If a match signal is generated within three count clocks, the changed value cannot be transferred to the register.

<5> When the values of 8-bit timer counter Hn and the CMP1n register after the change match, an inactive level is output. 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<6> Clearing the TMHEn bit to 0 during timer Hn operation sets the INTTMHn signal to the default and PWM output to an inactive level.

Remark n = 0 to 2, however, TOH0 and TOH1 only for TOHn

Figure 9-4. Format of Real-Time Counter Control Register 1 (RTCC1) (2/2)

RWAIT	Wait control of real-time counter
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.
Be sure to write "1" to it to read or write the counter value.
Because RSUBC continues operation, complete reading or writing of it in 1 second, and clear this bit back to 0.
When RWAIT = 1, it takes up to 1 clock (32.768 kHz) until the counter value can be read or written.
If RSUBC overflows when RWAIT = 1, it counts up after RWAIT = 0. If the second count register is written, however, it does not count up because RSUBC is cleared.

<R> **Caution The RIFG and WAFG flags may be cleared when the RTCC1 register is written by using a 1-bit manipulation instruction. Use, therefore, an 8-bit manipulation instruction in order to write to the RTCC1 register. To prevent the RIFG and WAFG flags from being cleared during writing, disable writing by setting "1" to the corresponding bit. When the value may be rewritten because the RIFG and WAFG flags are not being used, the RTCC1 register may be written by using a 1-bit manipulation instruction.**

Remark Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

(3) 16-bit ΔΣ type A/D conversion result register (ADDCR)

This register is a 16-bit register that stores the A/D conversion result. Each time A/D conversion ends, the conversion result is loaded from the ΔΣ A/D circuit. The higher 8 bits of the conversion result are stored in FF7FH and the lower 8 bits are stored in FF7EH.

ADDCR can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 13-4. Format of 16-Bit ΔΣ type A/D Conversion Result Register (ADDCR)

Address: FF7EH, FF7FH After reset: 0000H R

Symbol	FF7FH								FF7EH							
ADDCR																

Cautions 1. When N-bit resolution is set, conversion results are stored starting from the higher bits and the remaining 16-N bits are fixed to "0".

2. If the conversion completion interrupt and conversion result read operation conflict, the conversion result may be undefined. Read the conversion result after the generation of the conversion result completion interrupt, and before the next conversion completion.

(4) 8-bit ΔΣ type A/D conversion result register (ADDCRH)

This register is an 8-bit register that stores the A/D conversion result. The higher 8 bits of 16-bit resolution are stored.

ADDCRH can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-5. Format of 8-Bit ΔΣ type A/D Conversion Result Register (ADDCRH)

Address: FF7FH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ADDCRH								

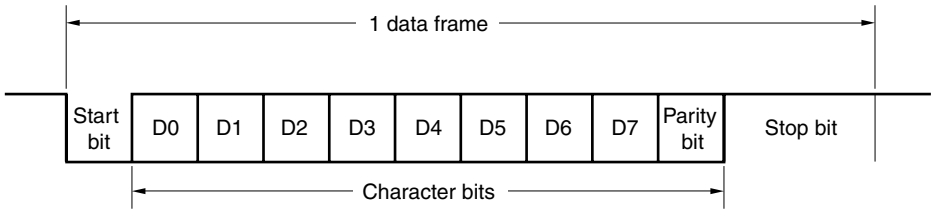
Caution If the conversion completion interrupt and conversion result read operation conflict, the read value of the conversion result may be undefined. Read the conversion result after the generation of the conversion result completion interrupt, and before the next conversion completion.

(2) Communication operation

(a) Format and waveform example of normal transmit/receive data

Figures 14-7 and 14-8 show the format and waveform example of the normal transmit/receive data.

Figure 14-7. Format of Normal UART Transmit/Receive Data



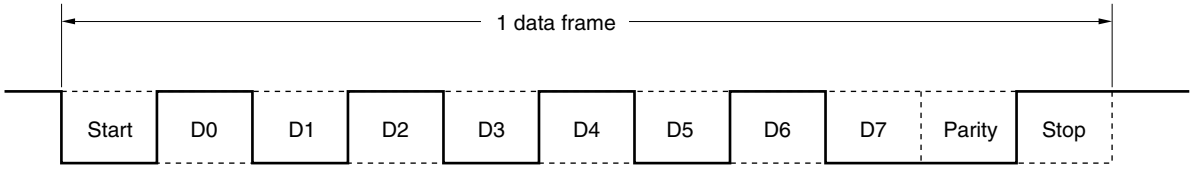
One data frame consists of the following bits.

- Start bit ... 1 bit
- Character bits ... 7 or 8 bits (LSB first)
- Parity bit ... Even parity, odd parity, 0 parity, or no parity
- Stop bit ... 1 or 2 bits

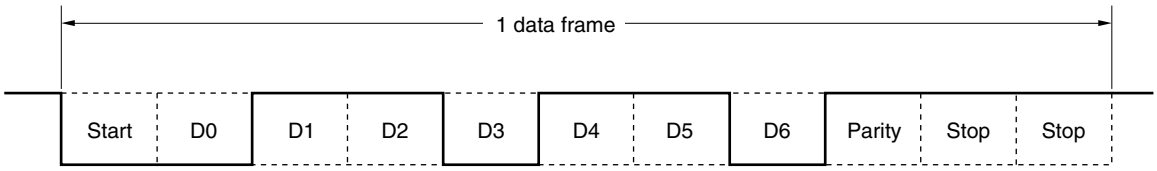
The character bit length, parity, and stop bit length in one data frame are specified by asynchronous serial interface operation mode register 0 (ASIM0).

Figure 14-8. Example of Normal UART Transmit/Receive Data Waveform

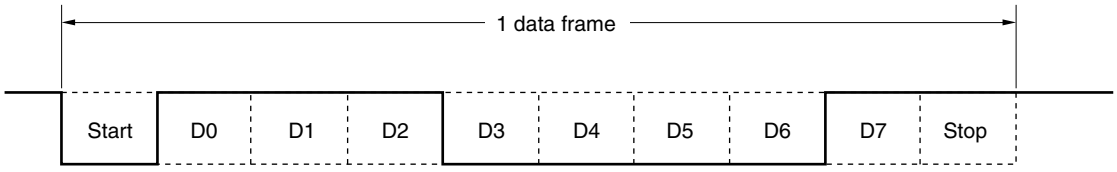
1. Data length: 8 bits, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H



2. Data length: 7 bits, Parity: Odd parity, Stop bit: 2 bits, Communication data: 36H



3. Data length: 8 bits, Parity: None, Stop bit: 1 bit, Communication data: 87H



(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- $\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1 \right) \times 100 \text{ [\%]}$

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

Example: Frequency of base clock = 10 MHz = 10,000,000 Hz
Set value of MDL67 to MDL60 bits of BRGC6 register = 00100001B (k = 33)
Target baud rate = 153600 bps

Baud rate = 10 M / (2 × 33)
= 10000000 / (2 × 33) = 151,515 [bps]

Error = (151515/153600 − 1) × 100
= −1.357 [%]

(b) μPD78F049x

The segment signals correspond to 32 bytes of the LCD display data memory (FA40H to FA5FH) during an LCD display period, bits 0, 1, 2, and 3 of each byte are read in synchronization with COM0, COM1, COM2, and COM3, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (SEG0 to SEG31).

Furthermore, segment signals correspond to the setting values of port registers 14 and 15 during a segment key scan output period. Bits 0 to 3 and bits 4 to 7 of each port register will be read in synchronization with the first half and latter half of the segment key scan output period, respectively, and if the content of each bit is 1 or 0, high levels or low levels will be output to the segment pins (SEG24 to SEG31), respectively.

Check, with the information given above, what combination of front-surface electrodes (corresponding to the segment signals) and rear-surface electrodes (corresponding to the common signals) forms display patterns in the LCD display data memory, and write the bit data that corresponds to the desired display pattern on a one-to-one basis.

LCD display data memory bits 1 to 3, bits 2 and 3, and bit 3 are not used for LCD display in the static display, two-time slot, and three-time slot modes, respectively. So these bits can be used for purposes other than display.

The higher 4 bits of FA40H to FA43H are fixed to 0.

(3) Output waveforms of common signals and segment signals during LCD display signal output period

The voltages shown in Table 18-4 are output to the common signals and segment signals during the LCD display signal output period.

When both common and segment signals are at the select voltage, a display on-voltage of $\pm V_{LCD}$ is obtained. The other combinations of the signals correspond to the display off-voltage.

Table 18-4. LCD Drive Voltage

(a) Static display mode (during LCD display signal output period)

Common Signal \ Segment Signal	Select Signal Level	Deselect Signal Level
	V_{SS}/V_{LC0}	V_{LC0}/V_{SS}
V_{LC0}/V_{SS}	$-V_{LCD}/+V_{LCD}$	0 V/0 V

(b) 1/2 bias method (during LCD display signal output period)

Common Signal \ Segment Signal		Select Signal Level	Deselect Signal Level
		V_{SS}/V_{LC0}	V_{LC0}/V_{SS}
Select signal level	V_{LC0}/V_{SS}	$-V_{LCD}/+V_{LCD}$	0 V/0 V
Deselect signal level	$V_{LC1} = V_{LC2}$	$-\frac{1}{2}V_{LCD}/+\frac{1}{2}V_{LCD}$	$+\frac{1}{2}V_{LCD}/-\frac{1}{2}V_{LCD}$

(c) 1/3 bias method (during LCD display signal output period)

Common Signal \ Segment Signal		Select Signal Level	Deselect Signal Level
		V_{SS}/V_{LC0}	V_{LC1}/V_{LC2}
Select signal level	V_{LC0}/V_{SS}	$-V_{LCD}/+V_{LCD}$	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$
Deselect signal level	V_{LC2}/V_{LC1}	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$	$+\frac{1}{3}V_{LCD}/-\frac{1}{3}V_{LCD}$

(d) 1/4 bias method (during LCD display signal output period)

Common Signal \ Segment Signal		Select Signal Level	Deselect Signal Level
		V_{LC0}/V_{SS}	V_{LC1}/V_{LC2}
Select signal level	V_{SS}/V_{LC0}	$+V_{LCD}/-V_{LCD}$	$+\frac{1}{2}V_{LCD}/-\frac{1}{2}V_{LCD}$
Deselect signal level	V_{LC1}/V_{LC3}	$+\frac{1}{4}V_{LCD}/-\frac{1}{4}V_{LCD}$	$-\frac{1}{4}V_{LCD}/+\frac{1}{4}V_{LCD}$

18.7.2 Two-time-slice display example

Figure 18-21 shows how the 6-digit LCD panel having the display pattern shown in Figure 18-20 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 and COM1) of the 78K0/LF3 chip. This example displays data "12345.6" in the LCD panel. The contents of the display data memory (FA40H to FA57H) correspond to this display.

The following description focuses on numeral "3" (∃) displayed in the fourth digit. To display "3" in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 to SEG15 pins according to Table 18-7 at the timing of the common signals COM0 and COM1; see Figure 18-20 for the relationship between the segment signals and LCD segments.

Table 18-7. Select and Deselect Voltages (COM0 and COM1)

Segment / Common	SEG12	SEG13	SEG14	SEG15
COM0	Select	Select	Deselect	Deselect
COM1	Deselect	Select	Select	Select

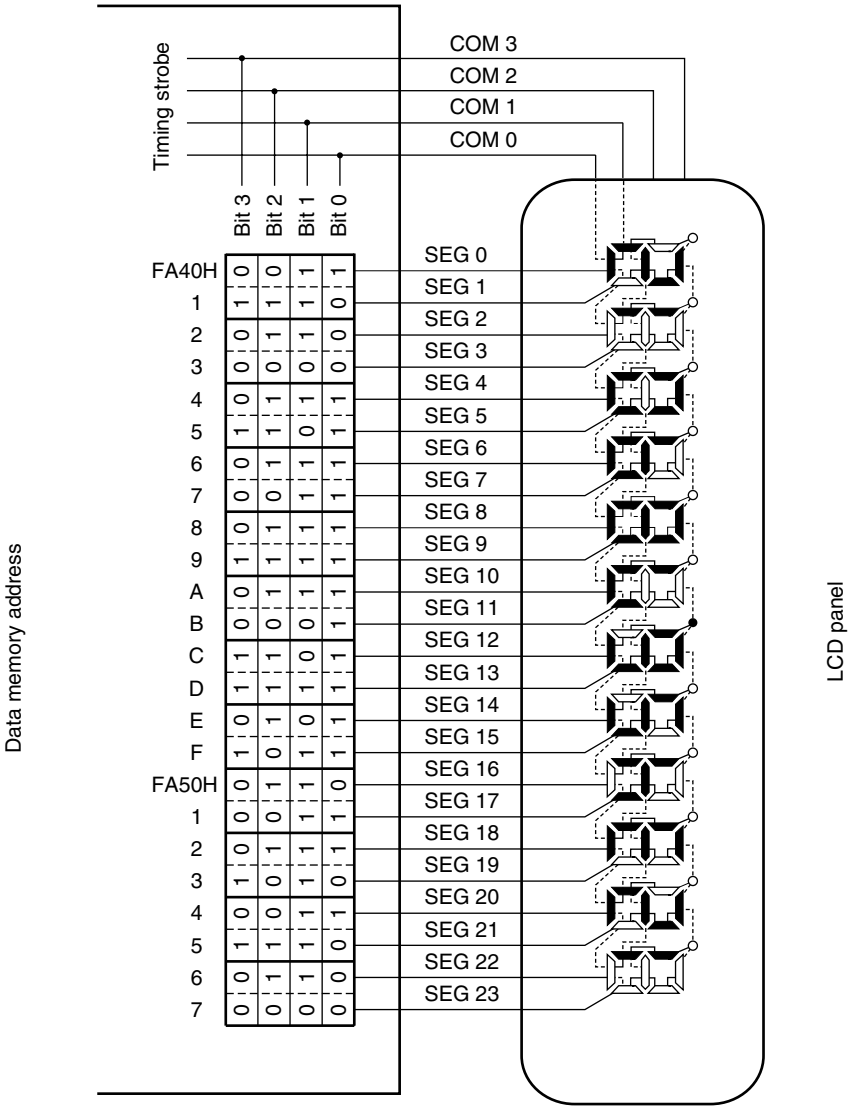
According to Table 18-7, it is determined that the display data memory location (FA4FH) that corresponds to SEG15 must contain xx10.

Figure 18-22 shows examples of LCD drive waveforms between the SEG15 signal and each common signal. When the select voltage is applied to SEG15 at the timing of COM1, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 18-20. Two-Time-Slice LCD Display Pattern and Electrode Connections

Remark n = 0 to 5

Figure 18-28. Example of Connecting Four-Time-Slice LCD Panel



19.4.2 Manchester code generator mode

This mode is used to transmit data in Manchester code format using the MCGO pin.

(1) Register description

MCG control register 0 (MC0CTL0), MCG control register 1 (MC0CTL1), and MCG control register 2 (MC0CTL2) are used to set the Manchester code generator mode.

(a) MCG control register 0 (MC0CTL0)

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Address: FF4CH After reset: 10H R/W

Symbol	<7>	6	5	<4>	3	2	<1>	<0>
MC0CTL0	MC0PWR	0	0	MC0DIR	0	0	MC0OSL	MC0OLV

MC0PWR	Operation control
0	Operation stopped
1	Operation enabled

MC0DIR	First bit specification
0	MSB
1	LSB

MC0OSL	Data format
0	Manchester code
1	Bit sequential data

MC0OLV	Output level when transmission suspended
0	Low level
1	High level

Caution Clear (0) the MC0PWR bit before rewriting the MC0DIR, MC0OSL, and MC0OLV bits (it is possible to rewrite these bits by an 8-bit memory manipulation instruction at the same time when the MC0PWR bit is set (1)).

19.4.3 Bit sequential buffer mode

The bit sequential buffer mode is used to output sequential signals using the MCGO pin.

(1) Register description

The MCG control register 0 (MC0CTL0), MCG control register 1 (MC0CTL1), and MCG control register 2 (MC0CTL2) are used to set the bit sequential buffer mode.

(a) MCG control register 0 (MC0CTL0)

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Address: FF4CH After reset: 10H R/W

Symbol	<7>	6	5	<4>	3	2	<1>	<0>
MC0CTL0	MC0PWR	0	0	MC0DIR	0	0	MC0OSL	MC0OLV

MC0PWR	Operation control
0	Operation stopped
1	Operation enabled

MC0DIR	First bit specification
0	MSB
1	LSB

MC0OSL	Data format
0	Manchester code
1	Bit sequential data

MC0OLV	Output level when transmission suspended
0	Low level
1	High level

Caution Clear (0) the MC0PWR bit before rewriting the MC0DIR, MC0OSL, and MC0OLV bits (it is possible to rewrite these bits by an 8-bit memory manipulation instruction at the same time when the MC0PWR bit is set (1)).

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second Operand / First Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP