Renesas Electronics America Inc - UPD78F0473GC-GAD-AX Datasheet

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Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0473gc-gad-ax

RENESAS

User's Manual

78K0/LF3

8-Bit Single-Chip Microcontrollers

μPD78F0471	μPD78F0481	μPD78F0491
μPD78F0472	μPD78F0482	μPD78F0492
μPD78F0473	μPD78F0483	μPD78F0493
μPD78F0474	μPD78F0484	μPD78F0494
μPD78F0475	μPD78F0485	μPD78F0495

Document No. U18329EJ4V0UD00 (4th edition)
Date Published August 2008 NS

Pin Identification

ANI0 to ANI7[Note 1]: Analog input
AV_{REF}[Note 1]: Analog reference voltage
AV_{SS}[Note 1]: Analog ground
BUZ: Buzzer output
COM0 to COM7: Common output
DS0+ to DS2+[Note 2]: ΔΣ Analog input (+)
DS0− to DS2−[Note 2]: ΔΣ Analog input (−)
EXCLK: External clock input (main system clock)
EXLVI: External potential input for low-voltage detector
FLMD0: Flash programming mode
INTP0 to INTP5: External interrupt input
KR0 to KR7: Key return
MCGO: Manchester code generator output
OCD0A, OCD0B: On chip debug input/output
P10 to P17: Port 1
P20 to P27: Port 2
P30 to P34: Port 3
P40 to P47: Port 4
P80 to P83: Port 8
P90 to P93: Port 9
P100 to P103: Port 10
P110 to P113: Port 11
P120 to P124: Port 12
P130 to P133: Port 13
P140 to P143: Port 14
P150 to P153: Port 15
PCL: Programmable clock output
REGC Regulator capacitance
$\overline{RESET}$: Reset
RxD0, RxD6: Receive data
REF+[Note 2]: ΔΣ Analog reference voltage (+)
REF−[Note 2]: ΔΣ Analog reference voltage (−)
RIN: Remote control input
RTC1HZ: Real-time counter correction clock (1 Hz) output
RTCCL: Real-time counter clock (32.768 kHz original oscillation) output
RTCDIV: Real-time counter clock (32.768 kHz divided frequency) output
SEG0 to SEG31: Segment output
SEG32 to SEG39[Note 3]: Segment output
SEG24 (KS0) to SEG31 (KS7): Segment key scan
$\overline{SCK10}$: Serial clock input/output
$\overline{SCKA0}$: Serial clock input/output
SI10: Serial data input
SIA0: Serial data input
SO10: Serial data output
SOA0: Serial data output
TI000, TI010: Timer input
TI50, TI51, TI52: Timer input
TO00: Timer output
TO50, TO51: Timer output
TOH0, TOH1: Timer output
TxD0, TxD6: Transmit data
V_{DD}: Power supply
V_{SS}: Ground
V_{LC0} to V_{LC3}: LCD power supply
X1, X2: Crystal oscillator (main system clock)
XT1, XT2: Crystal oscillator (subsystem clock)

Notes 1. μPD78F048x and 78F049x only.
2. μPD78F049x only.
3. μPD78F047x and 78F048x only.

3.1.1 Internal program memory space

The internal program memory space stores the program and table data. Normally, it is addressed with the program counter (PC).

78K0/LF3 products incorporate internal ROM (flash memory), as shown below.

Table 3-3. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
μPD78F0471, 78F0481, 78F0491	Flash memory	16384 × 8 bits (0000H to 3FFFH)
μPD78F0472, 78F0482, 78F0492		24576 × 8 bits (0000H to 5FFFH)
μPD78F0473, 78F0483, 78F0493		32768 × 8 bits (0000H to 7FFFH)
μPD78F0474, 78F0484, 78F0494		49152 × 8 bits (0000H to BFFFH)
μPD78F0475, 78F0485, 78F0495		61440 × 8 bits (0000H to EFFFH)

The internal program memory space is divided into the following areas.

(1) Vector table area

The 64-byte area 0000H to 003FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

Table 3-4. Vector Table

Vector Table Address	Interrupt Source	Vector Table Address	Interrupt Source
0000H	$\overline{\text{RESET}}$ input, POC, LVI, WDT	0022H	INTTM010
0004H	INTLVI	0024H[Note 1]	INTAD[Note 1]
0006H	INTP0	0026H	INTSR0
0008H	INTP1	0028H	INTRTC
000AH	INTP2	002AH	INTTM51
000CH	INTP3	002CH	INTKR
000EH	INTP4	002EH	INTRTCI
0010H	INTP5	0030H[Note 2]	INTDSAD[Note 2]
0012H	INTSRE6	0032H	INTTM52
0014H	INTSR6	0034H	INTTMH2
0016H	INTST6	0036H	INTMCG
0018H	INTCSI10/INTST0	0038H	INTRIN
001AH	INTTMH1	003AH	INTRERR/INTGP/INTREND /INTDFULL
001CH	INTTMH0	003CH	INTACSI
001EH	INTTM50	003EH	BRK
0020H	INTTM000		

Notes 1. μPD78F048x and 78F049x only.

2. μPD78F049x only.

Cautions 2. If clearing of bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) to 00 and input of the capture trigger conflict, then the captured data is undefined.

3. To change the mode from the capture mode to the comparison mode, first clear the TMC003 and TMC002 bits to 00, and then change the setting.

A value that has been once captured remains stored in CR000 unless the device is reset. If the mode has been changed to the comparison mode, be sure to set a comparison value.

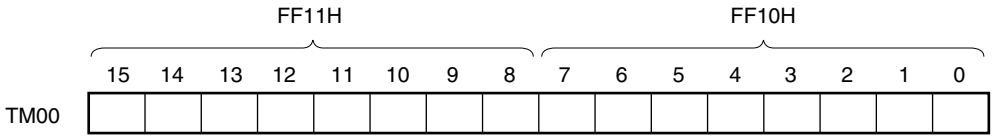
(1) 16-bit timer counter 00 (TM00)

TM00 is a 16-bit read-only register that counts count pulses.

The counter is incremented in synchronization with the rising edge of the count clock.

Figure 6-2. Format of 16-Bit Timer Counter 00 (TM00)

Address: FF10H, FF11H After reset: 0000H R



The count value of TM00 can be read by reading TM00 when the value of bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) is other than 00. The value of TM00 is 0000H if it is read when TMC003 and TMC002 = 00.

The count value is reset to 0000H in the following cases.

- At reset signal generation
- If TMC003 and TMC002 are cleared to 00
- If the valid edge of the TI000 pin is input in the mode in which the clear & start occurs when inputting the valid edge to the TI000 pin
- If TM00 and CR000 match in the mode in which the clear & start occurs when TM00 and CR000 match
- OSPT00 is set to 1 in one-shot pulse output mode or the valid edge is input to the TI000 pin

Caution Even if TM00 is read, the value is not captured by CR010.

(2) 16-bit timer capture/compare register 000 (CR000), 16-bit timer capture/compare register 010 (CR010)

CR000 and CR010 are 16-bit registers that are used with a capture function or comparison function selected by using CRC00.

Change the value of CR000 while the timer is stopped (TMC003 and TMC002 = 00).

The value of CR010 can be changed during operation if the value has been set in a specific way. For details, see **6.5.1 Rewriting CR010 during TM00 operation**.

These registers can be read or written in 16-bit units.

Reset signal generation sets these registers to 0000H.

Figure 6-5. Format of 16-Bit Timer Mode Control Register 00 (TMC00)

Address: FFBAH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
TMC00	0	0	0	0	TMC003	TMC002	TMC001	OVF00

TMC003	TMC002	Operation enable of 16-bit timer/event counter 00
0	0	Disables 16-bit timer/event counter 00 operation. Stops supplying operating clock. Clears 16-bit timer counter 00 (TM00).
0	1	Free-running timer mode
1	0	Clear & start mode entered by TI000 pin valid edge input[Note]
1	1	Clear & start mode entered upon a match between TM00 and CR000

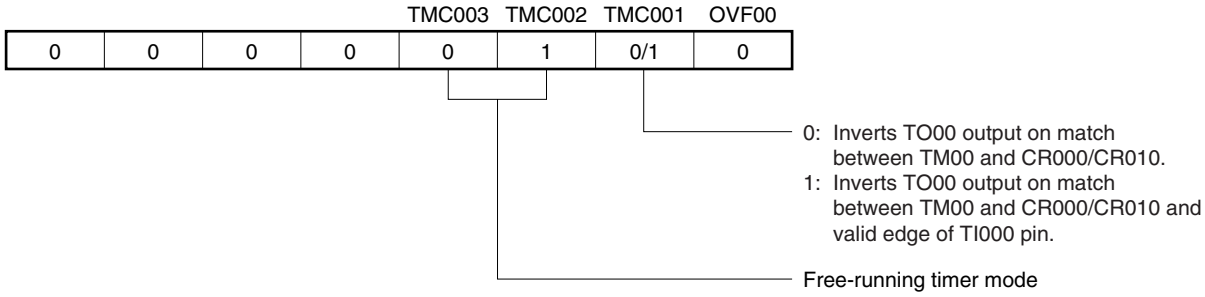
TMC001	Condition to reverse timer output (TO00)
0	• Match between TM00 and CR000 or match between TM00 and CR010
1	• Match between TM00 and CR000 or match between TM00 and CR010 • Trigger input of TI000 pin valid edge

OVF00	TM00 overflow flag
Clear (0)	Clears OVF00 to 0 or TMC003 and TMC002 = 00
Set (1)	Overflow occurs.
OVF00 is set to 1 when the value of TM00 changes from FFFFH to 0000H in all the operation modes (free-running timer mode, clear & start mode entered by TI000 pin valid edge input, and clear & start mode entered upon a match between TM00 and CR000). It can also be set to 1 by writing 1 to OVF00.	

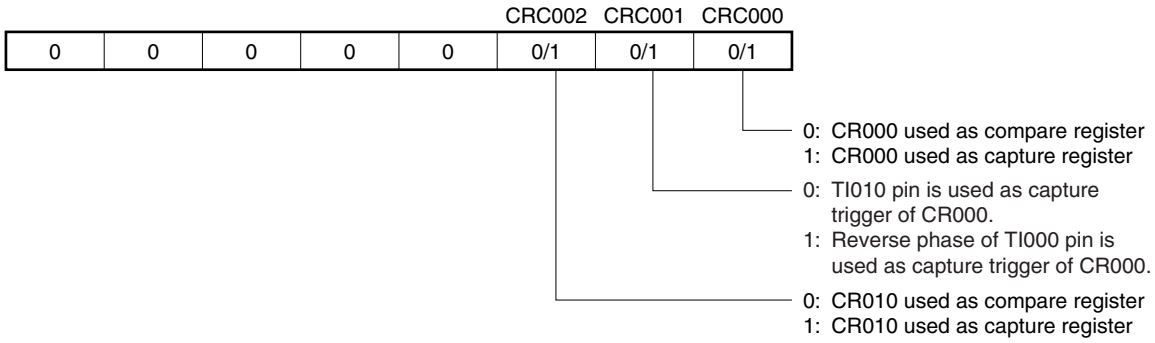
Note The TI000 pin valid edge is set by bits 5 and 4 (ES001, ES000) of prescaler mode register 00 (PRM00).

Figure 6-39. Example of Register Settings in Free-Running Timer Mode (1/2)

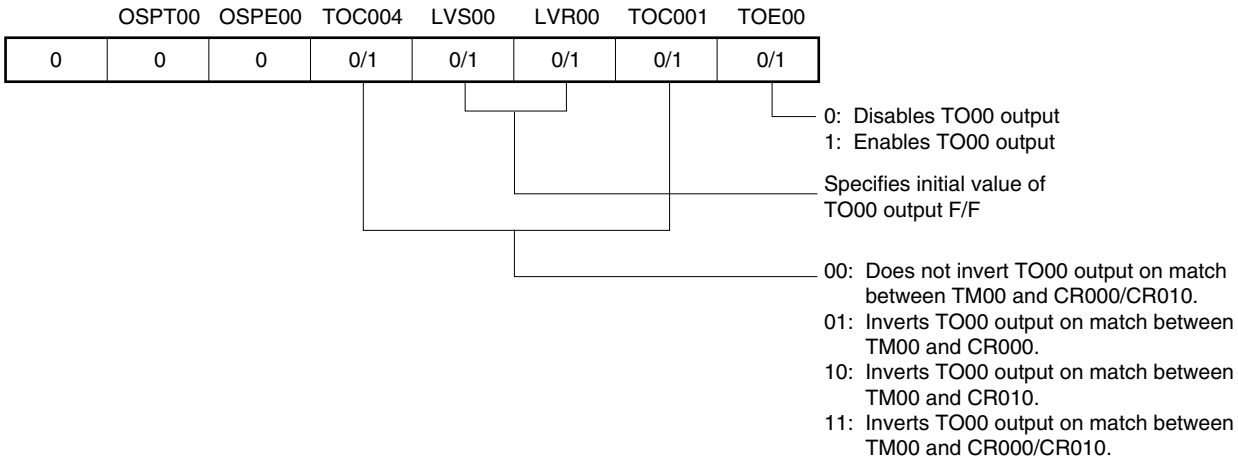
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



8.4.2 Operation as PWM output

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

The 8-bit timer compare register 0n (CMP0n) controls the cycle of timer output (TOHn). Rewriting the CMP0n register during timer operation is prohibited.

The 8-bit timer compare register 1n (CMP1n) controls the duty of timer output (TOHn). Rewriting the CMP1n register during timer operation is possible.

The operation in PWM output mode is as follows.

PWM output (TOHn output) outputs an active level and 8-bit timer counter Hn is cleared to 0 when 8-bit timer counter Hn and the CMP0n register match after the timer count is started. PWM output (TOHn output) outputs an inactive level when 8-bit timer counter Hn and the CMP1n register match.

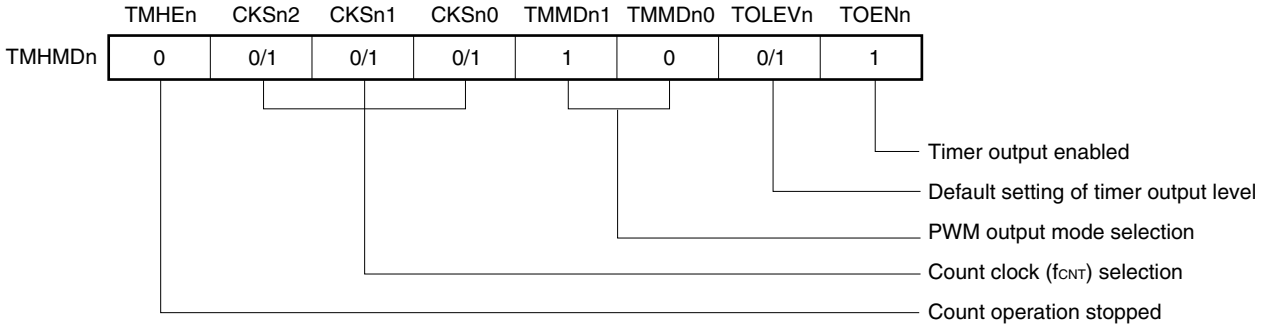
The timer output of TMH2 (PWM output) can only be used as an external event input enable signal of TM52. Note, no pins for external output are available.

Setting

<1> Set each register.

Figure 8-13. Register Setting in PWM Output Mode

(i) Setting timer H mode register n (TMHMDn)



(ii) Setting CMP0n register

- Compare value (N): Cycle setting

(iii) Setting CMP1n register

- Compare value (M): Duty setting

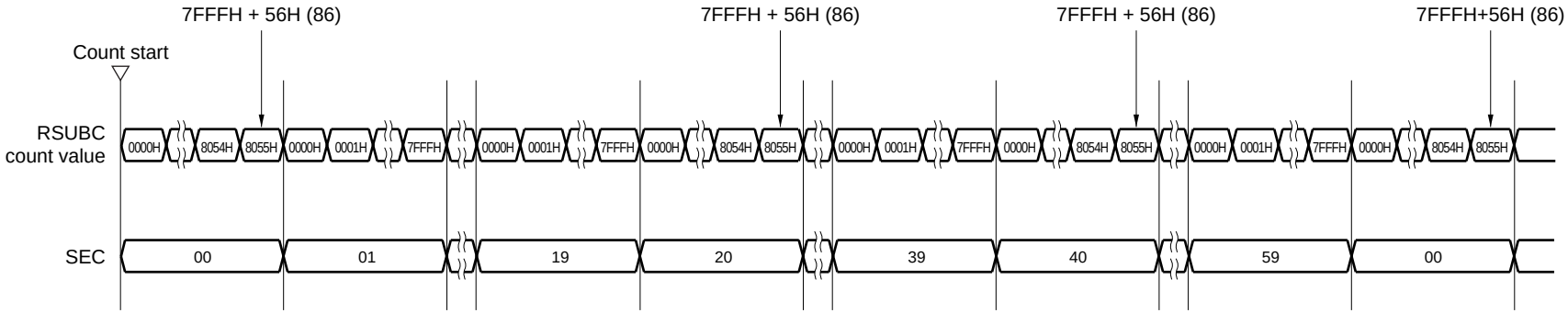
Remarks 1. n = 0 to 2, however, TOH0 and TOH1 only for TOHn

2. 00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

<2> The count operation starts when TMHEn = 1.

<3> The CMP0n register is the compare register that is to be compared first after counter operation is enabled. When the values of the 8-bit timer counter Hn and the CMP0n register match, the 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, an active level is output. At the same time, the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP0n register to the CMP1n register.

Figure 9-26. Operation when (DEV, F6, F5, F4, F3, F2, F1, F0) = (0, 0, 1, 0, 1, 1, 0, 0)



(3) Baud rate generator control register 0 (BRGC0)

This register selects the base clock of serial interface UART0 and the division value of the 5-bit counter.

BRGC0 can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 1FH.

Figure 14-4. Format of Baud Rate Generator Control Register 0 (BRGC0)

Address: FF71H After reset: 1FH R/W

Symbol	7	6	5	4	3	2	1	0
BRGC0	TPS01	TPS00	0	MDL04	MDL03	MDL02	MDL01	MDL00

TPS01	TPS00	Base clock (f_{XCLK0}) selection[Note 1]				
			f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz
0	0	TM50 output[Note 2]				
0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	4 MHz	5 MHz
1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1 MHz	1.25 MHz
1	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	250 kHz	312.5 kHz

MDL04	MDL03	MDL02	MDL01	MDL00	k	Selection of 5-bit counter output clock
0	0	×	×	×	×	Setting prohibited
0	1	0	0	0	8	$f_{XCLK0}/8$
0	1	0	0	1	9	$f_{XCLK0}/9$
0	1	0	1	0	10	$f_{XCLK0}/10$
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	1	0	1	0	26	$f_{XCLK0}/26$
1	1	0	1	1	27	$f_{XCLK0}/27$
1	1	1	0	0	28	$f_{XCLK0}/28$
1	1	1	0	1	29	$f_{XCLK0}/29$
1	1	1	1	0	30	$f_{XCLK0}/30$
1	1	1	1	1	31	$f_{XCLK0}/31$

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. Note the following points when selecting the TM50 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

The peripheral functions used in the LIN communication operation are shown below.

<Peripheral functions used>

- External interrupt (INTP0); wakeup signal detection
  Use: Detects the wakeup signal edges and detects start of communication.
- 16-bit timer/event counter 00 (TI000); baud rate error detection
  Use: Detects the baud rate error (measures the TI000 input edge interval in the capture mode) by detecting the sync field (SF) length and divides it by the number of bits.
- Serial interface UART6

15.2 Configuration of Serial Interface UART6

Serial interface UART6 includes the following hardware.

Table 15-1. Configuration of Serial Interface UART6

Item	Configuration
Registers	Receive buffer register 6 (RXB6) Receive shift register 6 (RXS6) Transmit buffer register 6 (TXB6) Transmit shift register 6 (TXS6)
Control registers	Asynchronous serial interface operation mode register 6 (ASIM6) Asynchronous serial interface reception error status register 6 (ASIS6) Asynchronous serial interface transmission status register 6 (ASIF6) Clock selection register 6 (CKSR6) Baud rate generator control register 6 (BRGC6) Asynchronous serial interface control register 6 (ASICL6) Input switch control register (ISC) Port function register 1 (PF1) Port mode register 1 (PM1) Port register 1 (P1) Port mode register 11 (PM11) Port register 11 (P11)

(1) Receive buffer register 6 (RXB6)

This 8-bit register stores parallel data converted by receive shift register 6 (RXS6).

Each time 1 byte of data has been received, new receive data is transferred to this register from RXS6. If the data length is set to 7 bits, data is transferred as follows.

- In LSB-first reception, the receive data is transferred to bits 0 to 6 of RXB6 and the MSB of RXB6 is always 0.
- In MSB-first reception, the receive data is transferred to bits 1 to 7 of RXB6 and the LSB of RXB6 is always 0.

If an overrun error (OVE6) occurs, the receive data is not transferred to RXB6.

RXB6 can be read by an 8-bit memory manipulation instruction. No data can be written to this register.

Reset signal generation sets this register to FFH.

(2) Receive shift register 6 (RXS6)

This register converts the serial data input to the RxD6 pin into parallel data.

RXS6 cannot be directly manipulated by a program.

(3) Transmit buffer register 6 (TXB6)

This buffer register is used to set transmit data. Transmission is started when data is written to TXB6.

This register can be read or written by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Cautions 1. Do not write data to TXB6 when bit 1 (TXBF6) of asynchronous serial interface transmission status register 6 (ASIF6) is 1.

2. Do not refresh (write the same value to) TXB6 by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of asynchronous serial interface operation mode register 6 (ASIM6) are 1 or when bits 7 and 5 (POWER6, RXE6) of ASIM6 are 1).

3. Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.

(4) Transmit shift register 6 (TXS6)

This register transmits the data transferred from TXB6 from the TxD6 pin as serial data. Data is transferred from TXB6 immediately after TXB6 is written for the first transmission, or immediately before INTST6 occurs after one frame was transmitted for continuous transmission. Data is transferred from TXB6 and transmitted from the TxD6 pin at the falling edge of the base clock.

TXS6 cannot be directly manipulated by a program.

(8) Port function register 1 (PF1)

This register sets the pin functions of P16/SOA0/TxD6 pin.

PF1 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF1 to 00H.

Figure 15-12. Format of Port Function Register 1 (PF1)

Address: FF20H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF1	0	PF16	0	0	PF13	0	0	0

PF16	Port (P16), CSIA0, and UART6 output specification
0	Used as P16 or SOA0
1	Used as TxD6

PF13	Port (P13), CSI10, and UART0 output specification
0	Used as P13 or SO10
1	Used as TxD0

(9) Port mode register 1 (PM1)

This register sets port 1 input/output in 1-bit units.

When using the P16/SOA0/TxD6 pin for serial interface data output, clear PM16 to 0. The output latch of P16 at this time may be 0 or 1.

When using the P15/SIA0/RxD6 pin for serial interface data input, set PM15 to 1. The output latch of P15 at this time may be 0 or 1.

PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 15-13. Format of Port Mode Register 1 (PM1)

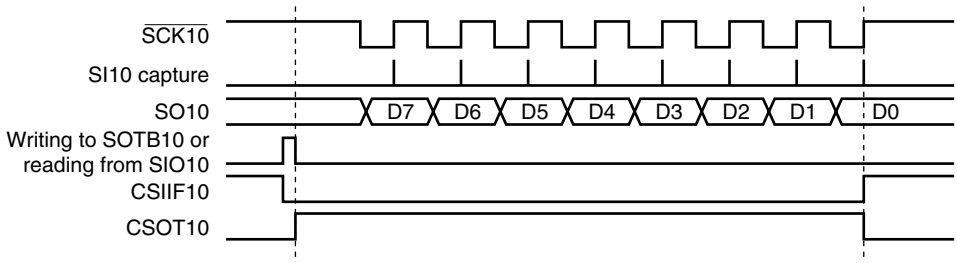
Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

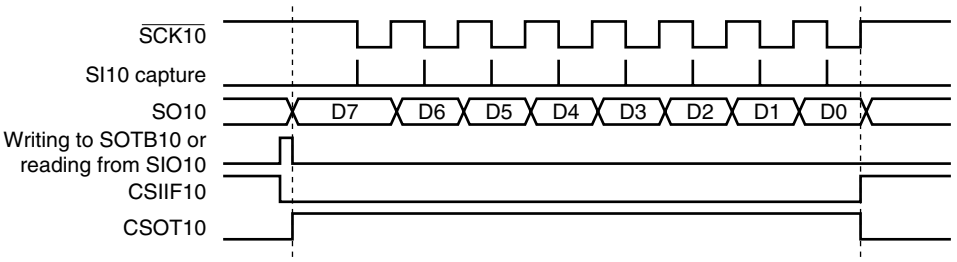
PM1n	P1n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 16-7. Timing of Clock/Data Phase

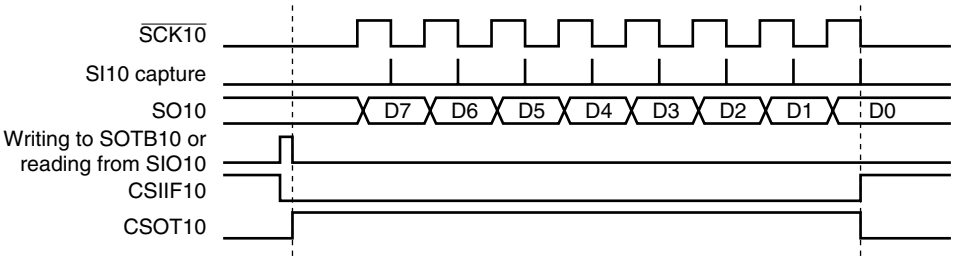
(a) Type 1: CKP10 = 0, DAP10 = 0, DIR10 = 0



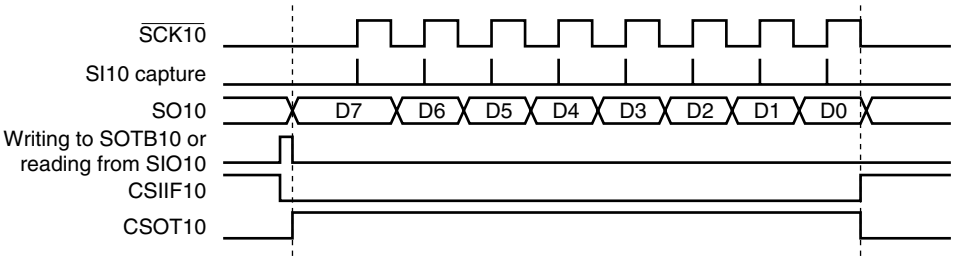
(b) Type 2: CKP10 = 0, DAP10 = 1, DIR10 = 0



(c) Type 3: CKP10 = 1, DAP10 = 0, DIR10 = 0



(d) Type 4: CKP10 = 1, DAP10 = 1, DIR10 = 0



Remark The above figure illustrates a communication operation where data is transmitted with the MSB first.

(6) Automatic data transfer interval specification register 0 (ADTI0)

This is an 8-bit register used to specify the interval time for byte data transfer during automatic data transfer (bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) = 1).

Set this register when in master mode (bit 4 (MASTER0) of CSIMA0 = 1) (setting is unnecessary in slave mode). Setting in 1-byte communication mode (bit 6 (ATE0) of CSIMA0 = 0) is also valid. When the interval time specified by ADTI0 after the end of 1-byte communication has elapsed, an interrupt request signal (INTACSI) is output. The number of clocks for the interval can be set to between 0 and 63 clocks.

This register can be set by an 8-bit memory manipulation instruction. However, when bit 0 (TSF0) of serial status register 0 (CSIS0) is 1, rewriting ADTI0 is prohibited.

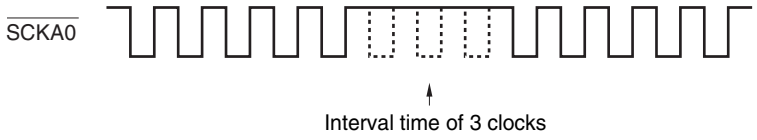
Figure 17-7. Format of Automatic Data Transfer Interval Specification Register 0 (ADTI0)

Address: FF95H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTI0	0	0	ADTI05	ADTI04	ADTI03	ADTI02	ADTI01	ADTI00

The specified interval time is the serial clock (specified by divisor selection register 0 (BRGCA0)) multiplied by an integer value.

Example When ADTI0 = 03H



(7) Automatic data transfer address count register 0 (ADTC0)

This is a register used to indicate buffer RAM addresses during automatic transfer. When automatic transfer is stopped, the data position when transfer stopped can be ascertained by reading ADTC0 register value.

This register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H. However, reading from ADTC0 is prohibited when bit 0 (TSF0) of serial status register 0 (CSIS0) = 1.

Figure 17-8. Format of Automatic Data Transfer Address Count Register 0 (ADTC0)

Address: FF97H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ADTC0	0	0	0	ADTC04	ADTC03	ADTC02	ADTC01	ADTP00

(8) Port function register 1 (PF1)

This register sets the pin functions of P16/SOA0/TxD6 pin.

PF1 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF1 to 00H.

Figure 17-9. Format of Port Function Register 1 (PF1)

Address: FF20H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF1	0	PF16	0	0	PF13	0	0	0

PF16	Port (P16), CSIA0, and UART6 output specification
0	Used as P16 or SOA0
1	Used as TxD6

PF13	Port (P13), CSI10, and UART0 output specification
0	Used as P13 or SO10
1	Used as TxD0

18.4.2 Setting method when using segment key scan function (KSON = 1)

When using the segment key scan function (KSON = 1), set the LCD controller/driver as follows. Set the LCD controller/driver using the following procedure.

<1> Set (VAON = 1) internal gate voltage boosting (bit 4 of the LCD display mode register (LCDM)).[Note 1]

<2> Set the resistance division method via MDSET0 and MDSET1 (bits 4 and 5 of the LCD mode register (LCDMD)) (MDSET0 = 0: external resistance division method, MDSET0 = 1: internal resistance division method).
Set (KSON = 1) KSON (bit 0 of the LCD mode register (LCDMD)).

<3> Set the pins to be used as segment outputs to the port function registers (PF2m, PFnALL).

<4> Use port mode register 4 (PM4) to set the pin to be used as a key scan input pin[Note 2] to PM4m = 1 (input mode).

<5> Use pull-up resistor option register 4 (PU4) to set the pin to be used as a key scan input pin[Note 2] to PU4m = 0 (connects an on-chip pull-up resistor only during the segment key scan output period).

<6> Use the key return mode register (KRM) to set the pin to be used as a segment key scan input pin to KRMm = 1[Note 3].

<7> Set an initial value to the RAM for LCD display.

<8> Set an initial value of segment key scan output to P14, P15.

<9> Set the number of time slices via LCDM0 to LCDM2 (bits 0 to 2 of the LCD display mode register (LCDM)).

<10> Set the LCD source clock and LCD clock via LCD clock control register 0 (LCDC0).

<11> Set (SCOC = 1) SCOC (bit 6 of the LCD display mode register (LCDM)).
Deselect signals are output from all the segment and common pins, and the non-display status is entered.

<12> Start output corresponding to each data memory by setting (LCDON = 1) LCDON (bit 7 of LCDM).

Hereinafter, set data to the data memory according to the contents displayed, and perform segment key scan output settings for the port registers (P14, P15) according to the contents of the segment key scan output.

Notes 1. Set VAON based on the following conditions.

<When set to the 1/3 bias method>

- When 2.5 V ≤ V_{LCD} = V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/2 bias method or 1/4 bias method >

- When 2.7 V ≤ V_{LCD} = V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 1

2. When using the segment key scan function, be sure to set port 4 as a segment key scan input pin and the pull-up resistor option register of the port to be used to PU4m = 0 (connects an on-chip pull-up resistor only during the segment key scan output period).
An external pull-up resistor cannot be used, because it affects the LCD display output.

3. An interrupt request flag may be set when KRM has been changed. Consequently, change the KRM register after having disabled interrupts, and enable interrupts after having cleared the interrupt request flag.

Table 24-1. Operation Statuses During Reset Period

Item			During Reset Period
System clock			Clock supply to the CPU is stopped.
	Main system clock	f_{RH}	Operation stopped
		f_X	Operation stopped (pin is I/O port mode)
		f_{EXCLK}	Clock input invalid (pin is I/O port mode)
	Subsystem clock	f_{XT}	Operation stopped (pin is I/O port mode)
	f_{RL}		Operation stopped
CPU			
Flash memory			
RAM			
Port (latch)			
16-bit timer/event counter		00	
8-bit timer/event counter		50	
		51	
		52	
8-bit timer		H0	
		H1	
		H2	
Real-time counter			
Watchdog timer			
Clock output			
Buzzer output			
10-bit successive approximation type A/D converter			
16-bit $\Delta\Sigma$ type A/D converter			
Serial interface		UART0	
		UART6	
		CSI10	
		CSIA0	
LCD controller/driver			
Manchester code generator			
Remote controller receiver			
Power-on-clear function			Operable
Low-voltage detection function			Operation stopped
External interrupt			

Remark f_{RH}: Internal high-speed oscillation clock
f_X: X1 oscillation clock
f_{EXCLK}: External main system clock
f_{XT}: XT1 oscillation clock
f_{RL}: Internal low-speed oscillation clock

28.6 Connection of Pins on Board

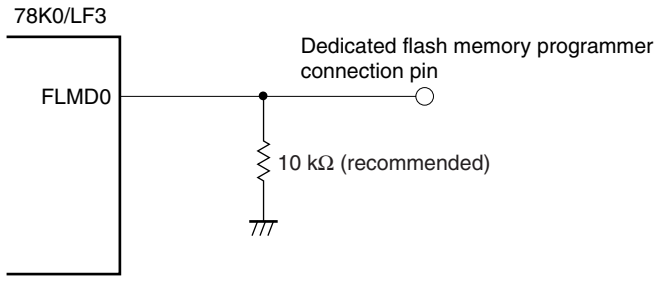
To write the flash memory on-board, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

28.6.1 FLMD0 pin

In the normal operation mode, 0 V is input to the FLMD0 pin. In the flash memory programming mode, the V_{DD} write voltage is supplied to the FLMD0 pin. An FLMD0 pin connection example is shown below.

Figure 28-8. FLMD0 Pin Connection Example



28.6.2 Serial interface pins

The pins used by each serial interface are listed below.

Table 28-5. Pins Used by Each Serial Interface

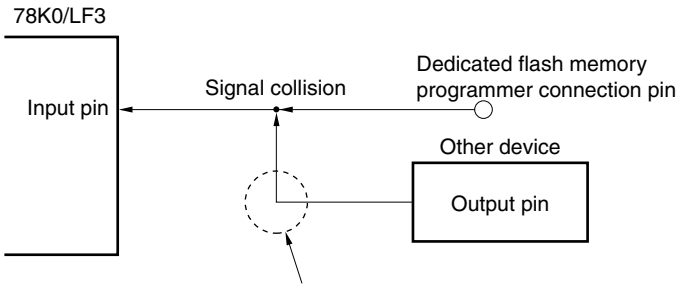
Serial Interface	Pins Used
CSI10	SO10, SI10, $\overline{SCK10}$
UART6	TxD6, RxD6

To connect the dedicated flash memory programmer to the pins of a serial interface that is connected to another device on the board, care must be exercised so that signals do not collide or that the other device does not malfunction.

(1) Signal collision

If the dedicated flash memory programmer (output) is connected to a pin (input) of a serial interface connected to another device (output), signal collision takes place. To avoid this collision, either isolate the connection with the other device, or make the other device go into an output high-impedance state.

Figure 28-9. Signal Collision (Input Pin of Serial Interface)

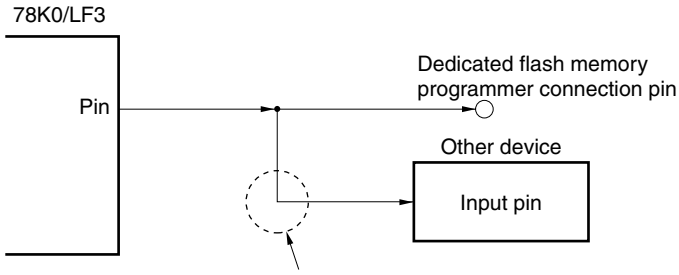


In the flash memory programming mode, the signal output by the device collides with the signal sent from the dedicated flash programmer. Therefore, isolate the signal of the other device.

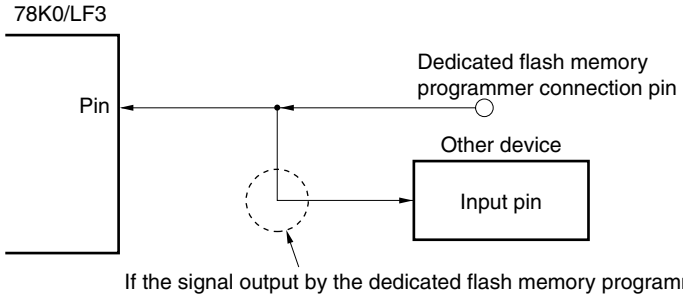
(2) Malfunction of other device

If the dedicated flash memory programmer (output or input) is connected to a pin (input or output) of a serial interface connected to another device (input), a signal may be output to the other device, causing the device to malfunction. To avoid this malfunction, isolate the connection with the other device.

Figure 28-10. Malfunction of Other Device



If the signal output by the 78K0/LF3 in the flash memory programming mode affects the other device, isolate the signal of the other device.



If the signal output by the dedicated flash memory programmer in the flash memory programming mode affects the other device, isolate the signal of the other device.

(3/3)

Page	Description	Classification
CHAPTER 24 RESET FUNCTION		
p. 666	Change of **Figure 24-2. Timing of Reset by $\overline{\text{RESET}}$ Input**	(c)
p. 666	Change of **Figure 24-3. Timing of Reset Due to Watchdog Timer Overflow**	(c)
p. 667	Change of **Figure 24-4. Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input**	(c)
CHAPTER 25 POWER-ON-CLEAR CIRCUIT		
p. 676	Change of **Figure 25-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1)**	(b)
p. 677	Change of **Caution 2** in **Figure 25-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2)**	(b, c)
CHAPTER 26 LOW-VOLTAGE DETECTOR		
p. 697	Change of **Figure 26-9. Example of Software Processing After Reset Release (2/2)**	(c)
CHAPTER 28 FLASH MEMORY		
p. 705	Change of **Note 2** in and addition of **Caution** to **Table 28-3. Wiring Between 78K0/LF3 and Dedicated Flash memory programmer**	(c)
p. 709	Change of **Note 1** in **Table 28-4. Pin Connection**	(c)
p. 712	Change of **Caution 2** in **28.6.6 Other signal pins**	(c)
p. 713	Change of **Figure 28-12. Flash Memory Manipulation Procedure**	(b)
p. 714	Change of **Table 28-7. Communication Modes**	(b)
pp. 718 to 720	Addition of **28.9 Processing Time for Each Command When PG-FP5 Is Used (Reference)**	(b, c)
pp. 721 to 730	Revision of **28.10 Flash Memory Programming by Self-Programming**	(b, c)
CHAPTER 29 ON-CHIP DEBUG FUNCTION		
pp. 731, 732	Full-scale revision of chapter	(c)
CHAPTER 31 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)		
p. 746	Addition of **Caution**	(c)
p. 750	Addition of **Recommended Oscillator Constants**	(b)
p. 754	Change of **Supply current value** and **Notes 1**, **6** in and addition of **Note 5** to **DC Characteristics**	(b)
p. 755	Change of $\Delta\Sigma$ type A/D converter operating current value in **DC Characteristics**	(b)
p. 765	Change of **16-bit $\Delta\Sigma$ type A/D Converter Characteristics**	(b)
p. 766	Change of **Note 3** in **LCD Characteristics**	(b)
p. 769	Change of **Basic characteristics** in **Flash Memory Programming Characteristics** and addition of **Notes 1**, **4**	(b, c)
CHAPTER 33 RECOMMENDED SOLDERING CONDITIONS		
p. 772	Addition of chapter	(b, c)
APPENDIX A DEVELOPMENT TOOLS		
pp. 775 to 782	Addition of appendix A	(c)

Remark “Classification” in the above table classifies revisions as follows.

(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents