Renesas Electronics America Inc - UPD78F0473GK-GAK-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0473gk-gak-ax

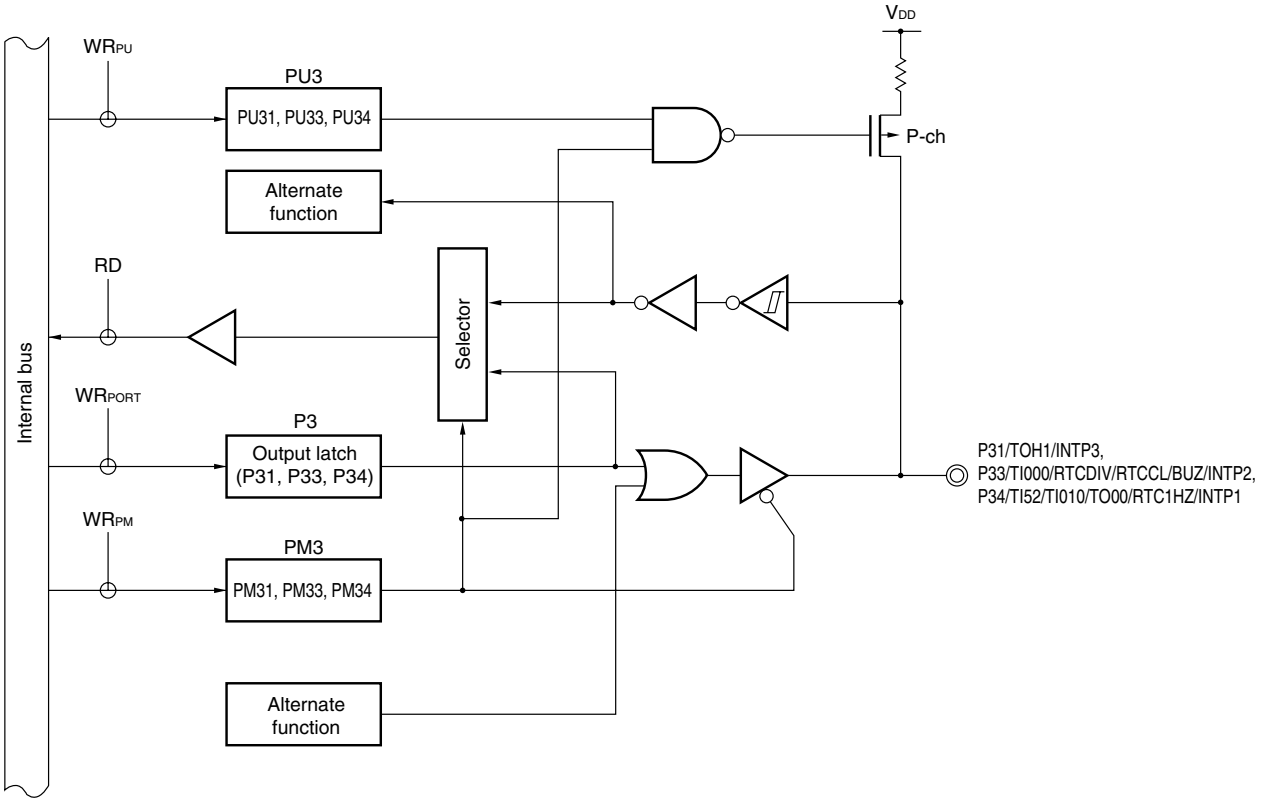
(2) Non-port pins **(2/4)**

Function Name	I/O	Function	After Reset	Alternate Function
SEG0 to SEG3	Output	LCD controller/driver segment signal outputs	Output	COM4 to COM7
SEG4 to SEG7			Input port	P80 to P83
SEG8 to SEG11				P90 to P93
SEG12 to SEG15				P100 to P103
SEG16, SEG17				P110, P111
SEG18				P112/TxD6
SEG19				P113/RxD6
SEG20 to SEG23				P130 to P133
<R> SEG24 (KS0) to SEG27 (KS3)		LCD controller/driver segment signal outputs. Segment key source signal can be simultaneously output.		P140 to P143
<R> SEG28 (KS4) to SEG31 (KS7)				P150 to P153
SEG32[Note 1]		LCD controller/driver segment signal outputs	Digital input port	P27/ANI7[Note 2]
SEG33[Note 1]				P26/ANI6[Note 2]
SEG34[Note 1]				P25/ANI5[Note 2]
SEG35[Note 1]				P24/ANI4[Note 2]
SEG36[Note 1]				P23/ANI3[Note 2]
SEG37[Note 1]				P22/ANI2[Note 2]
SEG38[Note 1]				P21/ANI1[Note 2]
SEG39[Note 1]				P20/ANI0[Note 2]
COM0 to COM3	Output	LCD controller/driver common signal outputs	Output	–
COM4 to COM7				SEG0 to SEG3
V_{LC0} to V_{LC2}	–	LCD drive voltage	–	–
V_{LC3}			Input port	P40/KR0

Notes 1. μPD78F047x and 78F048x only.

2. μPD78F048x and 78F049x only.

Figure 4-10. Block Diagram of P31, P33, P34



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

4.2.4 Port 4

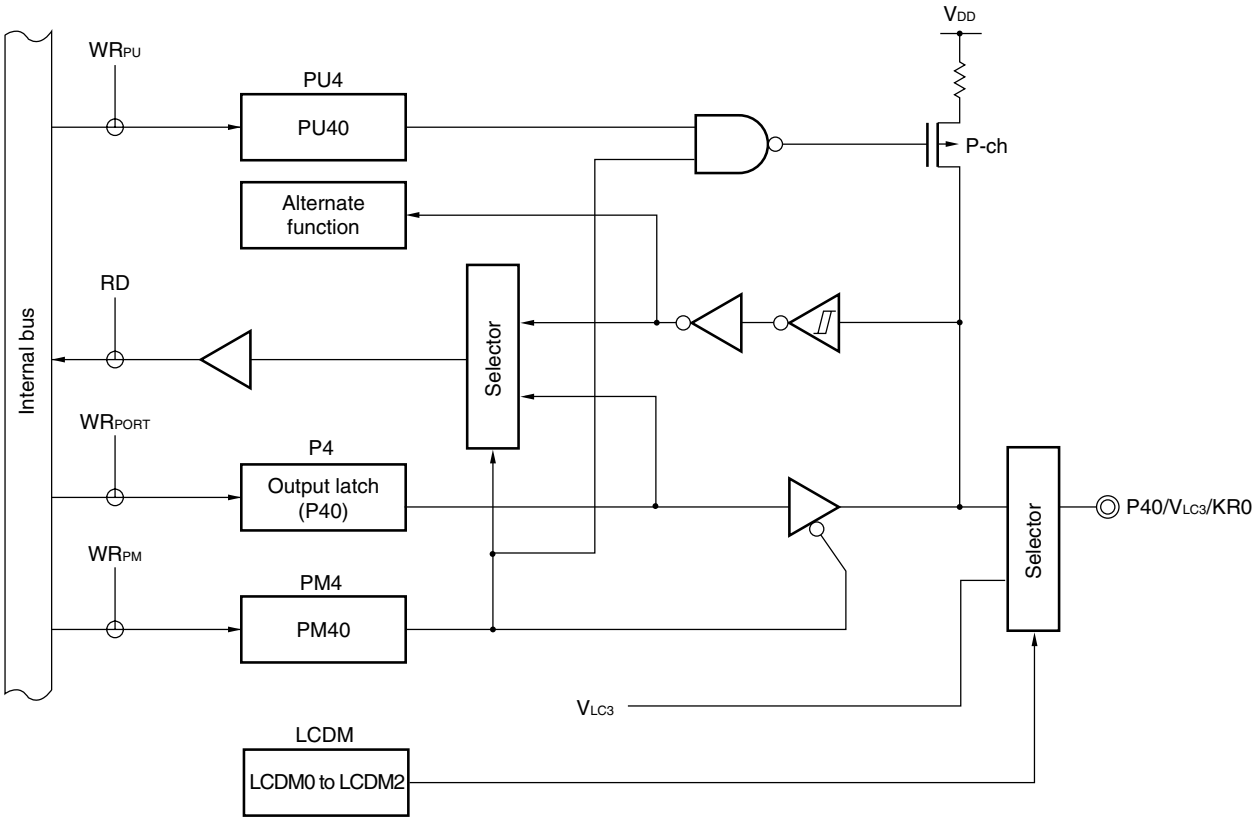
Port 4 is an 8-bit I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P47 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 4 (PU4).

This port can also be used for key interrupt input, segment key scan input, timer I/O, remote control receive data input, and power supply voltage for driving the LCD.

Reset signal generation sets port 4 to input mode.

Figures 4-12 to 4-14 show a block diagram of port 4.

Figure 4-12. Block Diagram of P40



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
LCDM: LCD display mode register
RD: Read signal
WR××: Write signal

CHAPTER 5 CLOCK GENERATOR

5.1 Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.
The following three kinds of system clocks and clock oscillators are selectable.

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 2 to 10 MHz by connecting a resonator to X1 and X2.
Oscillation can be stopped by executing the STOP instruction or using the main OSC control register (MOC).

<2> Internal high-speed oscillator

This circuit oscillates a clock of f_{RH} = 8 MHz (TYP.). After a reset release, the CPU always starts operating with this internal high-speed oscillation clock. Oscillation can be stopped by executing the STOP instruction or using the internal oscillation mode register (RCM).

An external main system clock (f_{EXCLK} = 2 to 10 MHz) can also be supplied from the OCD0B/EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or using RCM.
As the main system clock, a high-speed system clock (X1 clock or external main system clock) or internal high-speed oscillation clock can be selected by using the main clock mode register (MCM).

(2) Subsystem clock

- **Subsystem clock oscillator**

  This circuit oscillates at a frequency of f_{XT} = 32.768 kHz by connecting a 32.768 kHz resonator across XT1 and XT2. Oscillation can be stopped by using the processor clock control register (PCC) and clock operation mode select register (OSCCTL).

Remarks 1. f_X: X1 clock oscillation frequency
2. f_{RH}: Internal high-speed oscillation clock frequency
3. f_{EXCLK}: External main system clock frequency
4. f_{XT}: XT1 clock oscillation frequency

(5) Input switch control register (ISC)

The input source to TI000 becomes the input signal from the P33/TI000 pin, by setting ISC1 to 0.

ISC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets ISC to 00H.

Figure 6-10. Format of Input Switch Control Register (ISC)

Address: FF4FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	ICS5	ICS4	ICS3	ICS2	ICS1	ICS0

ICS5	ICS4	TxD6, RxD6 input source selection
0	0	TxD6:P112, RxD6: P113
0	1	TxD6:P16, RxD6: P15
Other than above		Setting prohibited

ISC3	RxD6/P113 input enabled/disabled
0	RxD6/P113 input disabled
1	RxD6/P113 input enabled

ISC2	TI52 input source control
0	No enable control of TI52 input (P34)
1	Enable controlled of TI52 input (P34)[Note 1]

ISC1	TI000 input source selection
0	TI000 (P33)
1	RxD6 (P15 or P113[Note 2])

ISC0	INTP0 input source selection
0	INTP0 (P120)
1	RxD6 (P15 or P113[Note 2])

Notes 1. TI52 input is controlled by TOH2 output signal.

2. This is selected by ISC5 and ISC4.

<R>

(6) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P34/TI52/TI010/TO00/RTC1HZ/INTP1 pin for timer output, set PM34 and the output latches of P34 to 0.

When using the P33/TI000/RTCDIV/RTCCL/BUZ/INTP2 and P34/TI52/TI010/TO00/RTC1HZ/INTP1 pins for timer input, set PM33 and PM34 to 1. At this time, the output latches of P33 and P34 may be 0 or 1.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM3 to FFH.

Figure 6-11. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

6.4 Operation of 16-Bit Timer/Event Counter 00

6.4.1 Interval timer operation

If bits 3 and 2 (TMC003 and TMC002) of the 16-bit timer mode control register (TMC00) are set to 11 (clear & start mode entered upon a match between TM00 and CR000), the count operation is started in synchronization with the count clock.

When the value of TM00 later matches the value of CR000, TM00 is cleared to 0000H and a match interrupt signal (INTTM000) is generated. This INTTM000 signal enables TM00 to operate as an interval timer.

Remarks 1. For the setting of I/O pins, see **6.3 (6) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 interrupt, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

Figure 6-12. Block Diagram of Interval Timer Operation

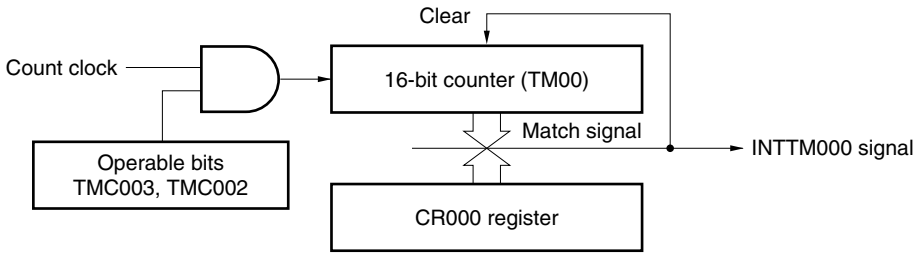


Figure 6-13. Basic Timing Example of Interval Timer Operation

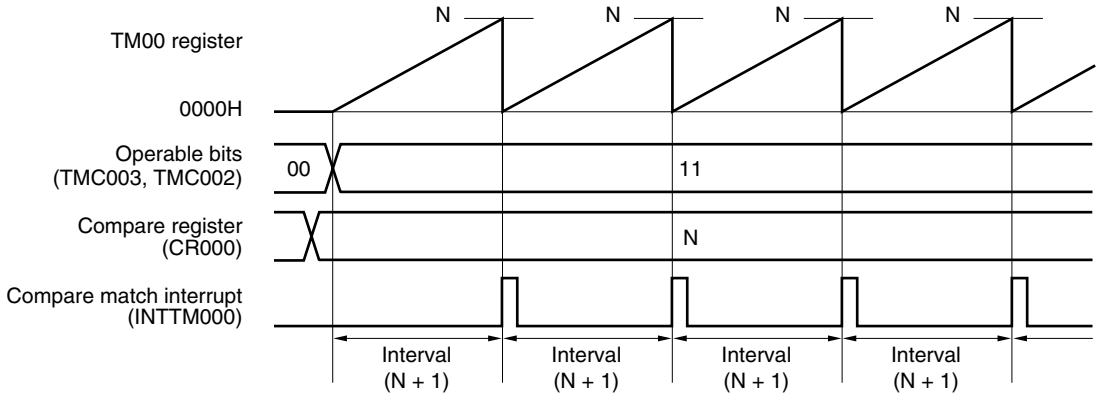
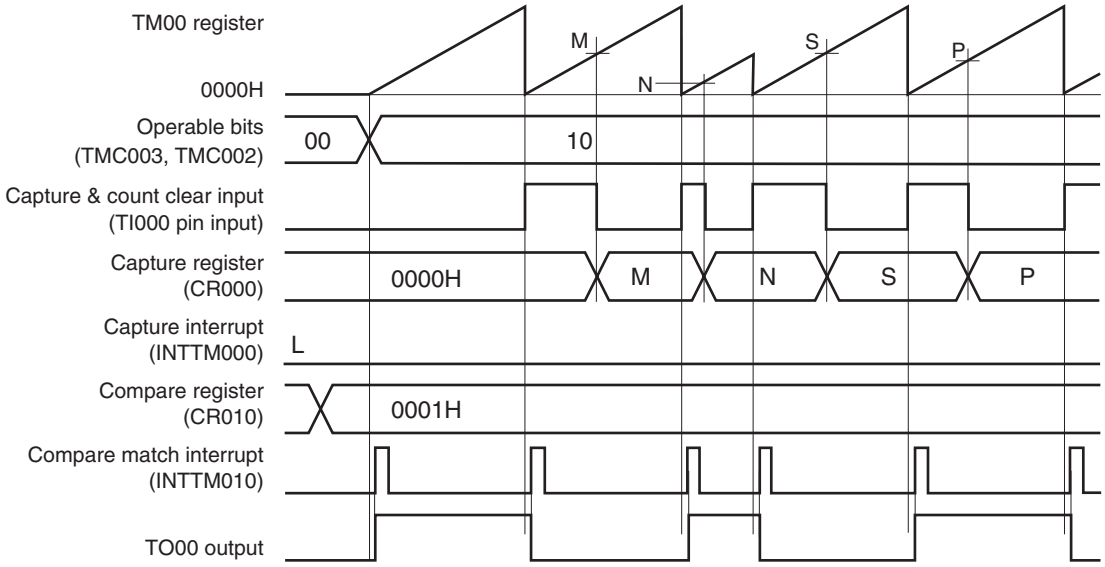


Figure 6-28. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00, = 03H, TMC00 = 08H, CR010 = 0001H



This is an application example where the TO00 output level is to be inverted when the count value has been captured & cleared.

TM00 is cleared at the rising edge detection of the TI000 pin and it is captured to CR000 at the falling edge detection of the TI000 pin.

When bit 1 (CRC001) of capture/compare control register 00 (CRC00) is set to 1, the count value of TM00 is captured to CR000 in the phase reverse to that of the signal input to the TI000 pin, but the capture interrupt signal (INTTM000) is not generated. However, the INTTM000 signal is generated when the valid edge of the TI010 pin is detected. Mask the INTTM000 signal when it is not used.

Figure 13-2. Format of 16-bit ΔΣ type A/D Converter Control Register 0 (ADDCTL0)

Address: FF7CH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
ADDCTL0	ADPON	ADDCE	HAC	AINMCD	0	0	ADDS1	ADDS0

ADDPON	16-bit ΔΣ type A/D circuit power supply control
0	Power supply OFF
1	Power supply ON

ADDCE	16-bit ΔΣ type A/D conversion operation control
0	Stops conversion operation
1	Starts conversion operation

HAC	Setting 16-bit ΔΣ type A/D conversion high-accuracy mode
0	High-accuracy mode OFF
1	High-accuracy mode ON

AINMOD	16-bit ΔΣ type A/D conversion input mode control
0	Single input
1	Differential input

ADDS1	ADDS0	16-bit ΔΣ type analog input specification
0	0	DS0+/DS0-
0	1	DS1+/DS1-
1	0	DS2+/DS2-
1	1	Setting prohibited

Cautions 1. Do not set the ADDPON and ADDCE bits to 1 at the same time. ADDCE must be set to 1, at least 1.2 μs after ADDPON has been set to 1.

2. Setting the ΔΣ analog input channel to be set by ADDS1 and ADDS0 to a pin which has been selected to be used in the analog input mode by the ADPC0 register is prohibited.

3. Operating 16-bit ΔΣ type A/D conversion and 10-bit successive approximation type A/D conversions at the same time (ADDCE = 1 and ADCS = 1) is prohibited.

4. If ADDCTL0 is rewritten (including identical data), A/D conversion operation is resumed after it has been initialized.

5. Set the input voltage in accordance with Table 13-4 Input Voltage Range.

6. When executing a STOP instruction, power to the 16-bit ΔΣ type A/D converter must be turned off (ADDPON = 0).

Figure 15-5. Format of Asynchronous Serial Interface Operation Mode Register 6 (ASIM6) (2/2)

PS61	PS60	Transmission operation	Reception operation
0	0	Does not output parity bit.	Reception without parity
0	1	Outputs 0 parity.	Reception as 0 parity[Note]
1	0	Outputs odd parity.	Judges as odd parity.
1	1	Outputs even parity.	Judges as even parity.

CL6	Specifies character length of transmit/receive data
0	Character length of data = 7 bits
1	Character length of data = 8 bits

SL6	Specifies number of stop bits of transmit data
0	Number of stop bits = 1
1	Number of stop bits = 2

ISRM6	Enables/disables occurrence of reception completion interrupt in case of error
0	“INTSRE6” occurs in case of error (at this time, INTSR6 does not occur).
1	“INTSR6” occurs in case of error (at this time, INTSRE6 does not occur).

Note If “reception as 0 parity” is selected, the parity is not judged. Therefore, bit 2 (PE6) of asynchronous serial interface reception error status register 6 (ASIS6) is not set and the error interrupt does not occur.

Cautions 1. To start the transmission, set POWER6 to 1 and then set TXE6 to 1. To stop the transmission, clear TXE6 to 0, and then clear POWER6 to 0.

2. To start the reception, set POWER6 to 1 and then set RXE6 to 1. To stop the reception, clear RXE6 to 0, and then clear POWER6 to 0.

3. Set POWER6 to 1 and then set RXE6 to 1 while a high level is input to the RxD6 pin. If POWER6 is set to 1 and RXE6 is set to 1 while a low level is input, reception is started.

4. TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.

5. Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.

6. Clear the TXE6 and RXE6 bits to 0 before rewriting the PS61, PS60, and CL6 bits.

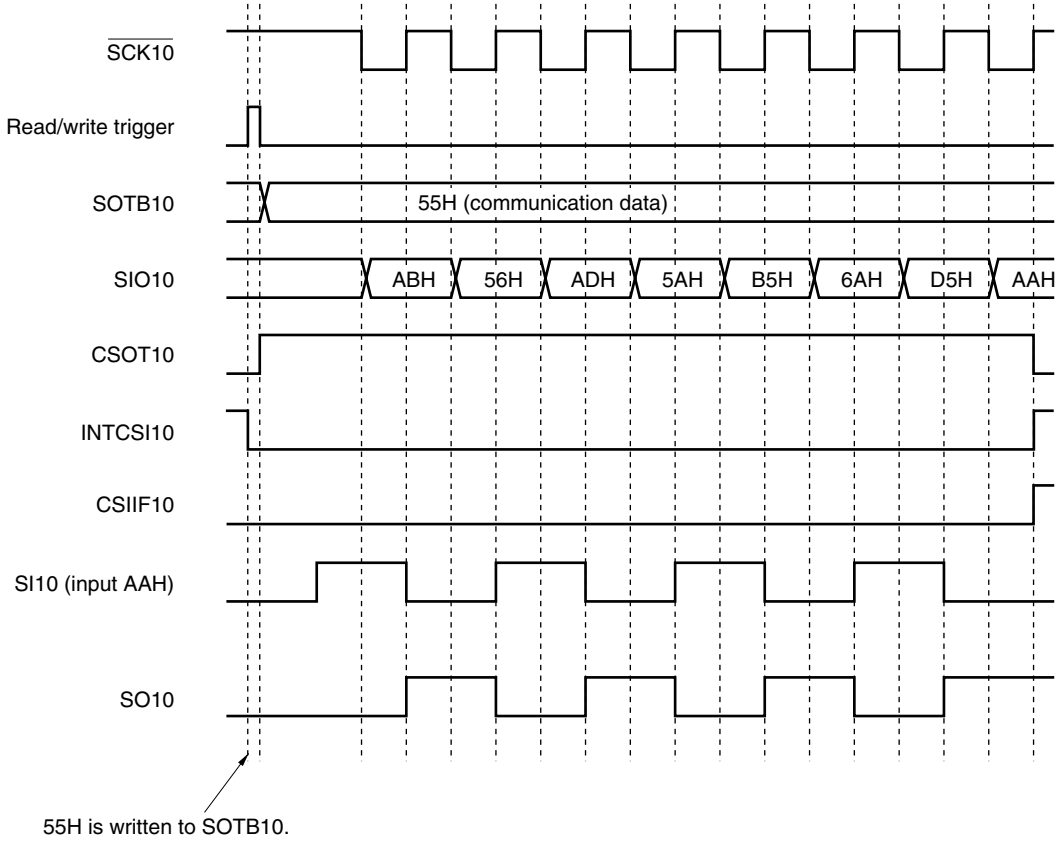
7. Fix the PS61 and PS60 bits to 0 when used in LIN communication operation.

8. Clear TXE6 to 0 before rewriting the SL6 bit. Reception is always performed with “the number of stop bits = 1”, and therefore, is not affected by the set value of the SL6 bit.

9. Make sure that RXE6 = 0 when rewriting the ISRM6 bit.

Figure 16-6. Timing in 3-Wire Serial I/O Mode (2/2)

(b) Transmission/reception timing (Type 2: TRMD10 = 1, DIR10 = 0, CKP10 = 0, DAP10 = 1)



(3) Serial trigger register 0 (CSIT0)

This is an 8-bit register used to control execution/stop of automatic data transfer between buffer RAM and serial I/O shift register 0 (SIOA0).

This register can be set by a 1-bit or 8-bit memory manipulation instruction. This register can be set when bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) is 1.

Reset signal generation clears this register to 00H.

Figure 17-4. Format of Serial Trigger Register 0 (CSIT0)

Address: FF92H After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	<0>
CSIT0	0	0	0	0	0	0	ATSTP0	ATSTA0

ATSTP0	Automatic data transfer stop
0	–
1	Automatic data transfer stopped

ATSTA0	Automatic data transfer start
0	–
1	Automatic data transfer started

Cautions 1. Even if ATSTP0 or ATSTA0 is set to 1, automatic transfer cannot be started/stopped until 1-byte transfer is complete.

2. ATSTP0 and ATSTA0 change to 0 automatically after the interrupt signal INTACSI is generated.

3. After automatic data transfer is stopped, the data address when the transfer stopped is stored in automatic data transfer address count register 0 (ADTC0). However, since no function to restart automatic data transfer is incorporated, when transfer is stopped by setting ATSTP0 = 1, start automatic data transfer by setting ATSTA0 to 1 after re-setting the registers.

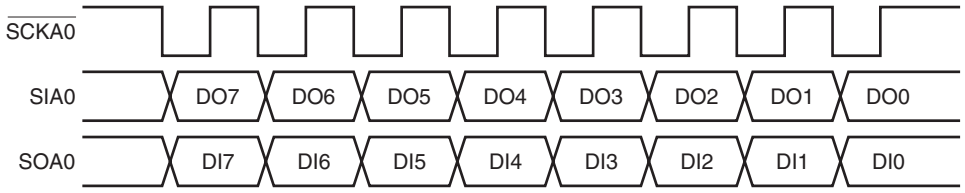
(b) Data format

In the data format, data is changed in synchronization with the $\overline{\text{SCKA0}}$ falling edge as shown below.

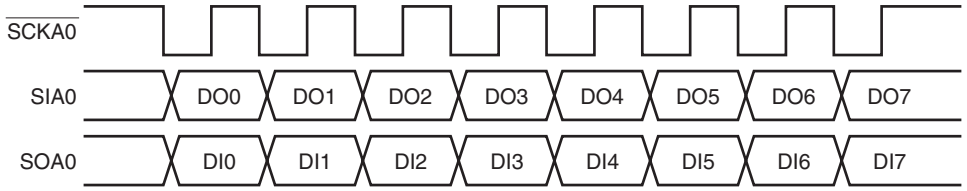
The data length is fixed to 8 bits and the data communication direction can be switched by the specification of bit 1 (DIR0) of serial operation mode specification register 0 (CSIMA0).

Figure 17-12. Format of Transmit/Receive Data

(a) MSB-first (DIR0 bit = 0)



(b) LSB-first (DIR0 bit = 1)



<R>

CHAPTER 18 LCD CONTROLLER/DRIVER

18.1 Functions of LCD Controller/Driver

The functions of the LCD controller/driver in the 78K0/LF3 are as follows.

(1) The LCD driver voltage generator can switch external resistance division and internal resistance division.
(2) Automatic output of segment and common signals based on automatic display data memory read
(3) Six different display modes:
- Static
- 1/2 duty (1/2 bias)
- 1/3 duty (1/2 bias)
- 1/3 duty (1/3 bias)
- 1/4 duty (1/3 bias)
- 1/8 duty (1/4 bias)

(4) Six different frame frequencies, selectable in each display mode
(5) μPD78F047x: Segment signal outputs: 40[Note] (SEG0 to SEG39),
Common signal outputs: 8[Note] (COM0 to COM7)
μPD78F048x: Segment signal outputs: 40[Note] (SEG0 to SEG39),
Common signal outputs: 8[Note] (COM0 to COM7)
μPD78F049x: Segment signal outputs: 32[Note] (SEG0 to SEG31),
Common signal outputs: 8[Note] (COM0 to COM7)
(6) Output of LCD segment signals and time division output of segment key source signals in each display mode (except static mode)
Segment key source signal outputs: Max. 8 (SEG24 (KS0) to SEG31 (KS7))

Note The four segment signal outputs (SEG0 to SEG3) and four common signal outputs (COM4 to COM7) are alternate-function pins. COM4 to COM7 can be used only when eight-time-slice mode is selected by the setting of the LCD display mode register (LCDM).

CHAPTER 23 STANDBY FUNCTION

23.1 Standby Function and Configuration

23.1.1 Standby function

The standby function is designed to reduce the operating current of the system. The following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, internal high-speed oscillator, internal low-speed oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions 1. The STOP mode can be used only when the CPU is operating on the main system clock. The subsystem clock oscillation cannot be stopped. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.

2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.

3. The following sequence is recommended for operating current reduction of the 10-bit successive approximation type A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

The following sequence is recommended for operating current reduction of the 16-bit ΔΣ type A/D converter when the standby function is used: First clear bit 7 (ADDPON) and bit 6 (ADDCE) of the 16-bit ΔΣ type A/D converter mode register (ADDCTL0) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

CHAPTER 24 RESET FUNCTION

The following four operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
(4) Internal reset by comparison of supply voltage and detection voltage of low-power-supply detector (LVI)

External and internal resets have no functional differences. In both cases, program execution starts at the address at 0000H and 0001H when the reset signal is generated.

A reset is applied when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection, and each item of hardware is set to the status shown in Tables 24-1 and 24-2. Each pin is high impedance during reset signal generation or during the oscillation stabilization time just after a reset release.

When a low level is input to the $\overline{\text{RESET}}$ pin, the device is reset. It is released from the reset status when a high level is input to the $\overline{\text{RESET}}$ pin and program execution is started with the internal high-speed oscillation clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the internal high-speed oscillation clock (see **Figures 24-2** to **24-4**) after reset processing. Reset by POC and LVI circuit power supply detection is automatically released when $V_{DD} \geq V_{POC}$ or $V_{DD} \geq V_{LVI}$ after the reset, and program execution starts using the internal high-speed oscillation clock (see **CHAPTER 25 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 26 LOW-VOLTAGE DETECTOR**) after reset processing.

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.
2. During reset input, the X1 clock, XT1 clock, internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input becomes invalid.
3. When the STOP mode is released by a reset, the STOP mode contents are held during reset input. However, the port pins become high-impedance.

25.4 Cautions for Power-on-Clear Circuit

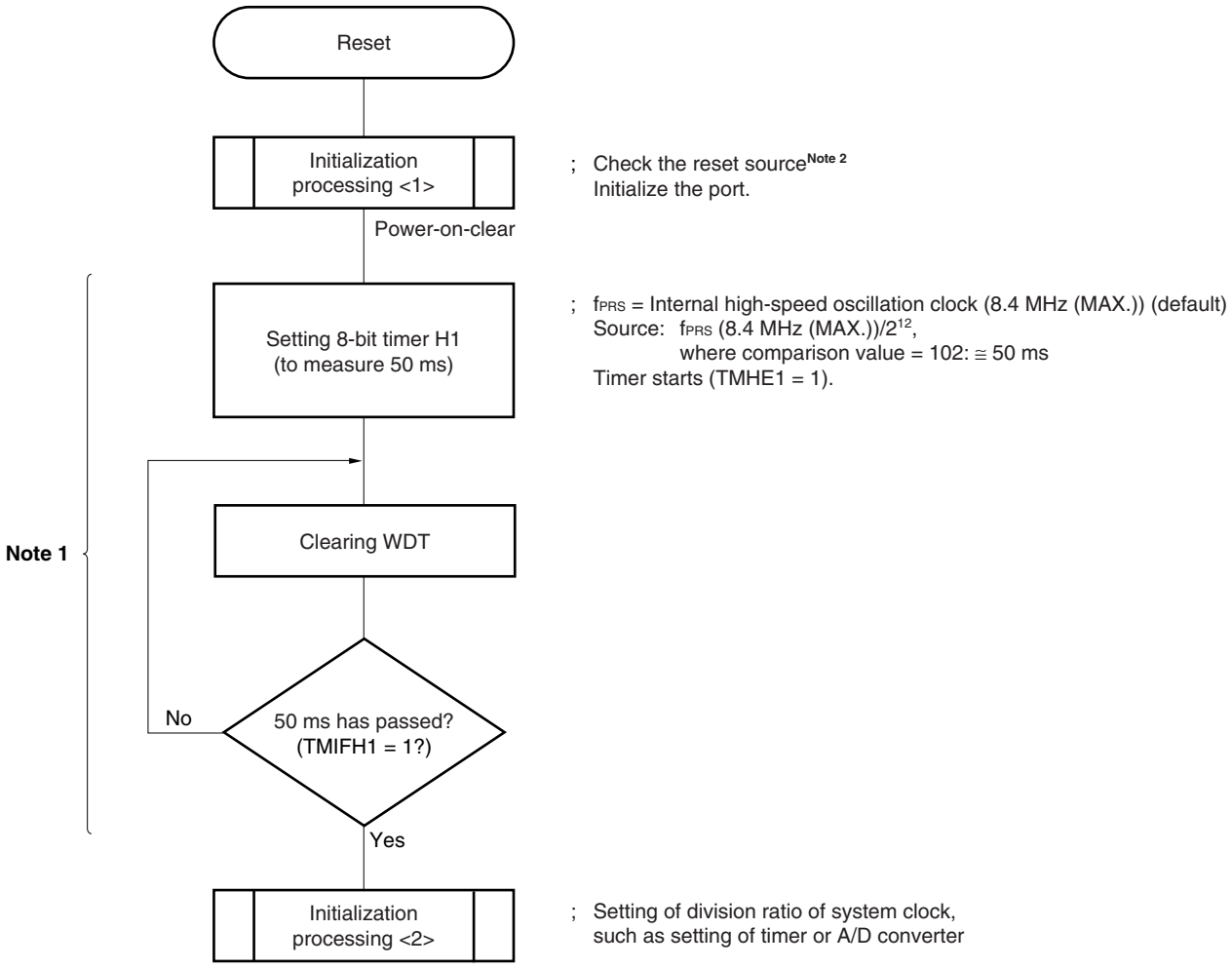
In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POC detection voltage (V_{POC}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

Figure 25-3. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of POC detection voltage



Notes 1. If reset is generated again during this period, initialization processing <2> is not started.

2. A flowchart is shown on the next page.

CHAPTER 27 OPTION BYTE

27.1 Functions of Option Bytes

The flash memory at 0080H to 0084H of the 78K0/LF3 is an option byte area. When power is turned on or when the device is restarted from the reset status, the device automatically references the option bytes and sets specified functions. When using the product, be sure to set the following functions by using the option bytes.

When the boot swap operation is used during self-programming, 0080H to 0084H are switched to 1080H to 1084H. Therefore, set values that are the same as those of 0080H to 0084H to 1080H to 1084H in advance.

Caution Be sure to set 00H to 0082H and 0083H (0082H/1082H and 0083H/1083H when the boot swap function is used).

(1) 0080H/1080H

- ○ Internal low-speed oscillator operation
  - Can be stopped by software
  - Cannot be stopped
- ○ Watchdog timer interval time setting
- ○ Watchdog timer counter operation
  - Enabled counter operation
  - Disabled counter operation
- ○ Watchdog timer window open period setting

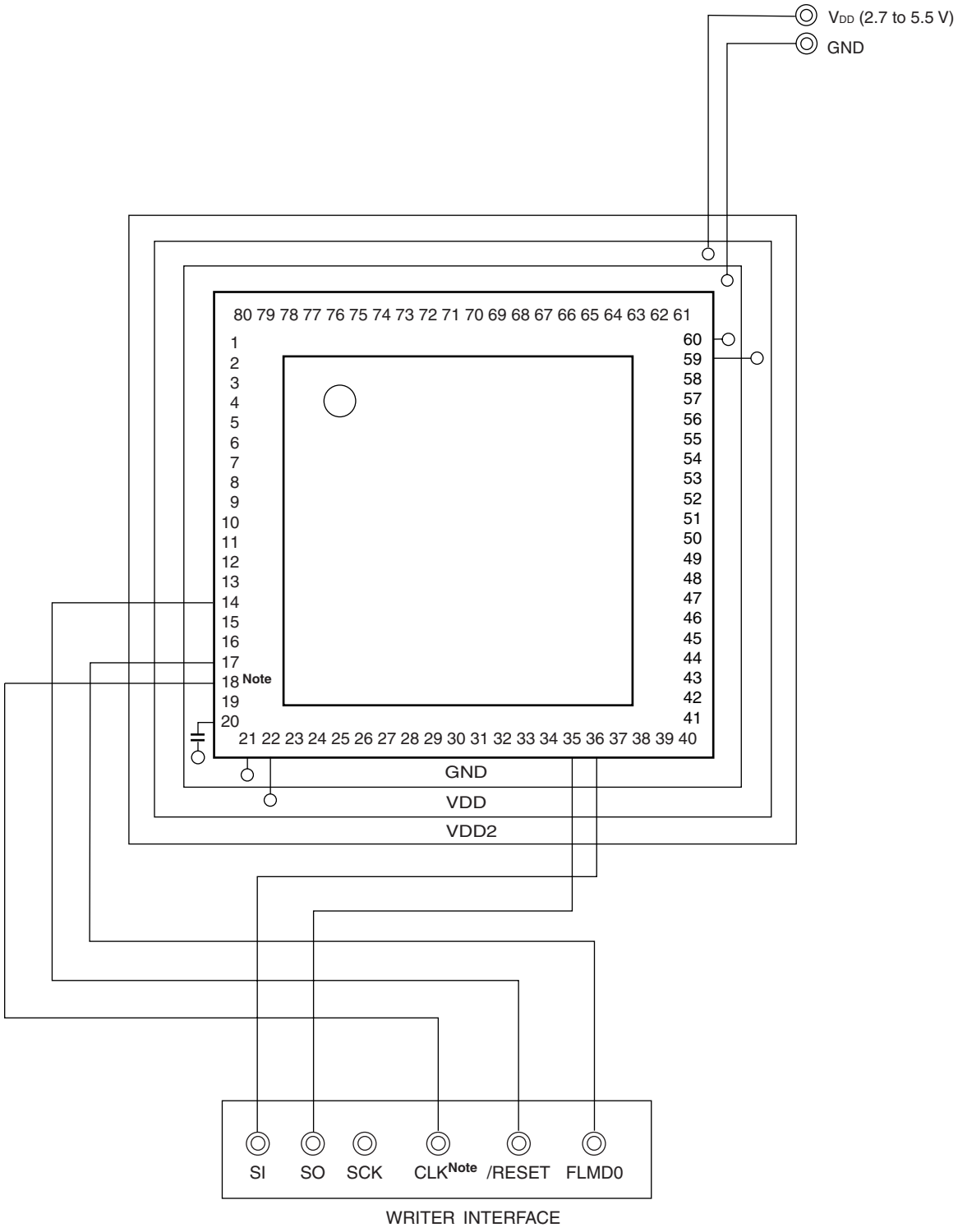
Caution Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.

(2) 0081H/1081H

- ○ Selecting POC mode
  - During 2.7 V/1.59 V POC mode operation (POCMODE = 1)
    The device is in the reset state upon power application and until the supply voltage reaches 2.7 V (TYP.). It is released from the reset state when the voltage exceeds 2.7 V (TYP.). After that, POC is not detected at 2.7 V but is detected at 1.59 V (TYP.).
    If the supply voltage rises to 1.8 V after power application at a pace slower than 0.5 V/ms (MIN.), use of the 2.7 V/1.59 V POC mode is recommended.
  - During 1.59 V POC mode operation (POCMODE = 0)
    The device is in the reset state upon power application and until the supply voltage reaches 1.59 V (TYP.). It is released from the reset state when the voltage exceeds 1.59 V (TYP.). After that, POC is detected at 1.59 V (TYP.), in the same manner as on power application.

Caution POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming (at this time, 1.59 V POC mode (default) is set). However, because the value of 1081H is copied to 0081H during the boot swap operation, it is recommended to set a value that is the same as that of 0081H to 1081H when the boot swap function is used.

Figure 28-4. Example of Wiring Adapter for Flash Memory Writing in UART (UART6) Mode



Note The above figure illustrates an example of wiring when using the clock output from the PG-FP5 or FL-PR5.

CHAPTER 30 INSTRUCTION SET

This chapter lists each instruction set of the 78K0/LF3 in table form. For details of each operation and operation code, refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

30.1 Conventions Used in Operation List

30.1.1 Operand identifiers and specification methods

Operands are written in the "Operand" column of each instruction in accordance with the specification method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more methods, select one of them. Uppercase letters and the symbols #, !, $ and [ ] are keywords and must be written as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to write the #, !, $, and [ ] symbols.

For operand register identifiers r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for specification.

Table 30-1. Operand Identifiers and Specification Methods

Identifier	Specification Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol[Note]
sfrp	Special function register symbol (16-bit manipulatable register even addresses only)[Note]
saddr	FE20H to FF1FH Immediate data or labels
saddrp	FE20H to FF1FH Immediate data or labels (even address only)
addr16	0000H to FFFFH Immediate data or labels (Only even addresses for 16-bit data transfer instructions)
addr11	0800H to 0FFFH Immediate data or labels
addr5	0040H to 007FH Immediate data or labels (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
RBn	RB0 to RB3

Note Addresses from FFD0H to FFDFH cannot be accessed with these operands.

Remark For special function register symbols, see **Table 3-6 Special Function Register List**.