Renesas Electronics America Inc - UPD78F0481GK-GAK-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0481gk-gak-ax

Table 4-2. Port Functions (1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCL
P11				$\overline{\text{SCK10}}$
P12				SI10/RxD0
P13				SO10/TxD0
P14				$\overline{\text{SCKA0}}$/INTP4
P15				SIA0/<RxD6>
P16				SOA0/<TxD6>
P17				–
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	SEG39[Note1]/ANI0[Note2]/DS0–[Note3]
P21				SEG38[Note1]/ANI1[Note2]/DS0+[Note3]
P22				SEG37[Note1]/ANI2[Note2]/DS1–[Note3]
P23				SEG36[Note1]/ANI3[Note2]/DS1+[Note3]
P24				SEG35[Note1]/ANI4[Note2]/DS2–[Note3]
P25				SEG34[Note1]/ANI5[Note2]/DS2+[Note3]
P26				SEG33[Note1]/ANI6[Note2]/REF–[Note3]
P27				SEG32[Note1]/ANI7[Note2]/REF+[Note3]
P30	I/O	Port 3. 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP5
P31				TOH1/INTP3
P32				TOH0/MCGO
P33				TI000/RTCDIV/RTCCL/BUZ/INTP2
P34				TI52/TI010/TO00/RTC1HZ/INTP1
P40	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	V_{LC3}/KR0
P41				RIN/KR1
P42				KR2
P43				TO51/TI51/KR3
P44				TO50/TI50/KR4
P45 to P47				KR5 to KR7

Notes **1.** μPD78F047x and 78F048x only.

2. μPD78F048x and 78F049x only.

3. μPD78F049x only.

Remark The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

4.2.1 Port 1

Port 1 is an 8-bit I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P17 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

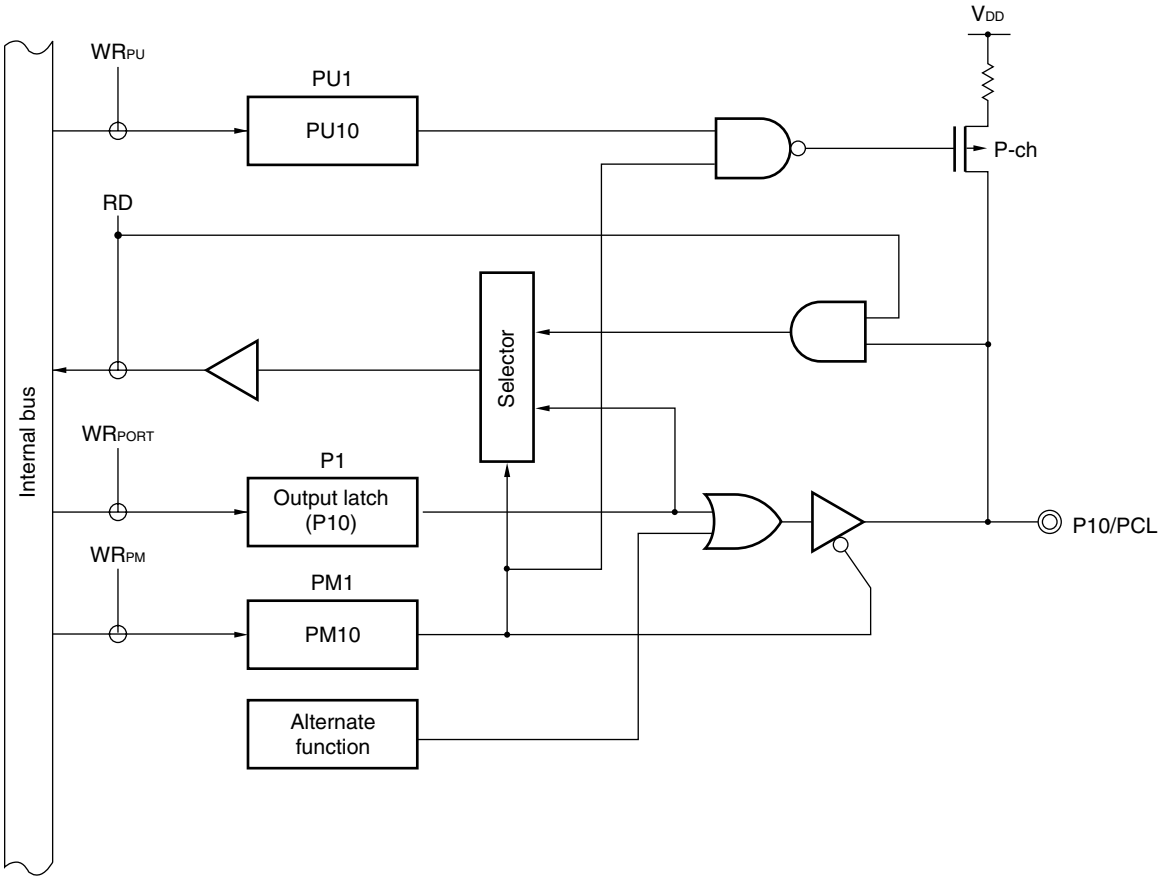
This port can also be used for serial clock I/O, serial interface data I/O, and maskable external interrupt input.

Reset signal generation sets port 1 to input mode.

Figures 4-2 to 4-7 show block diagrams of port 1.

Caution To use P11/$\overline{\text{SCK10}}$, P12/SI10/RxD0, and P13/SO10/TxD0 as general-purpose ports, set serial operation mode register 10 (CSIM10) and serial clock selection register 10 (CSIC10) to the default status (00H).

Figure 4-2. Block Diagram of P10



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

4.2.6 Port 9

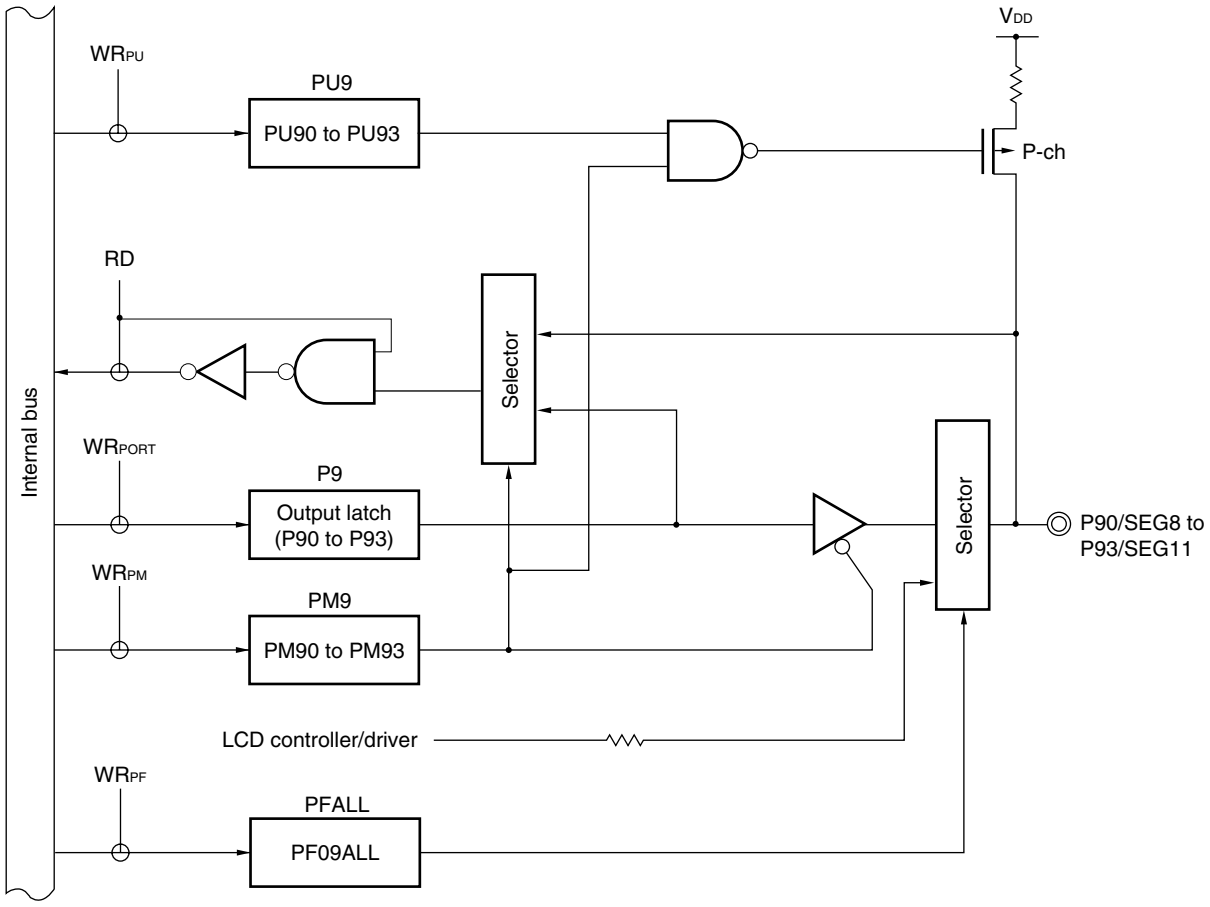
Port 9 is a 4-bit I/O port with an output latch. Port 9 can be set to the input mode or output mode in 1-bit units using port mode register 9 (PM9). When the P90 to P93 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 9 (PU9).

This port can also be used for segment output.

Reset signal generation sets port 9 to input mode.

Figure 4-16 shows block diagrams of port 9.

Figure 4-16. Block Diagram of P90 to P93



P9: Port register 9
PU9: Pull-up resistor option register 9
PM9: Port mode register 9
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

5.4 System Clock Oscillator

5.4.1 X1 oscillator

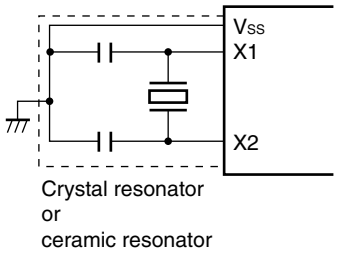
The X1 oscillator oscillates with a crystal resonator or ceramic resonator (2 to 10 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

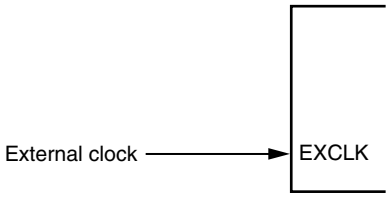
Figure 5-10 shows an example of the external circuit of the X1 oscillator.

Figure 5-10. Example of External Circuit of X1 Oscillator

(a) Crystal or ceramic oscillation



(b) External clock



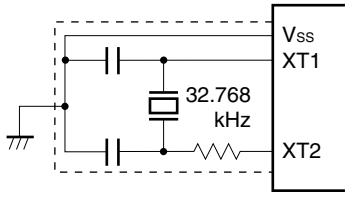
5.4.2 XT1 oscillator

The XT1 oscillator oscillates with a crystal resonator (standard: 32.768 kHz) connected to the XT1 and XT2 pins.

Figure 5-11 shows an example of the external circuit of the XT1 oscillator.

Figure 5-11. Example of External Circuit of XT1 Oscillator

(a) Crystal oscillation

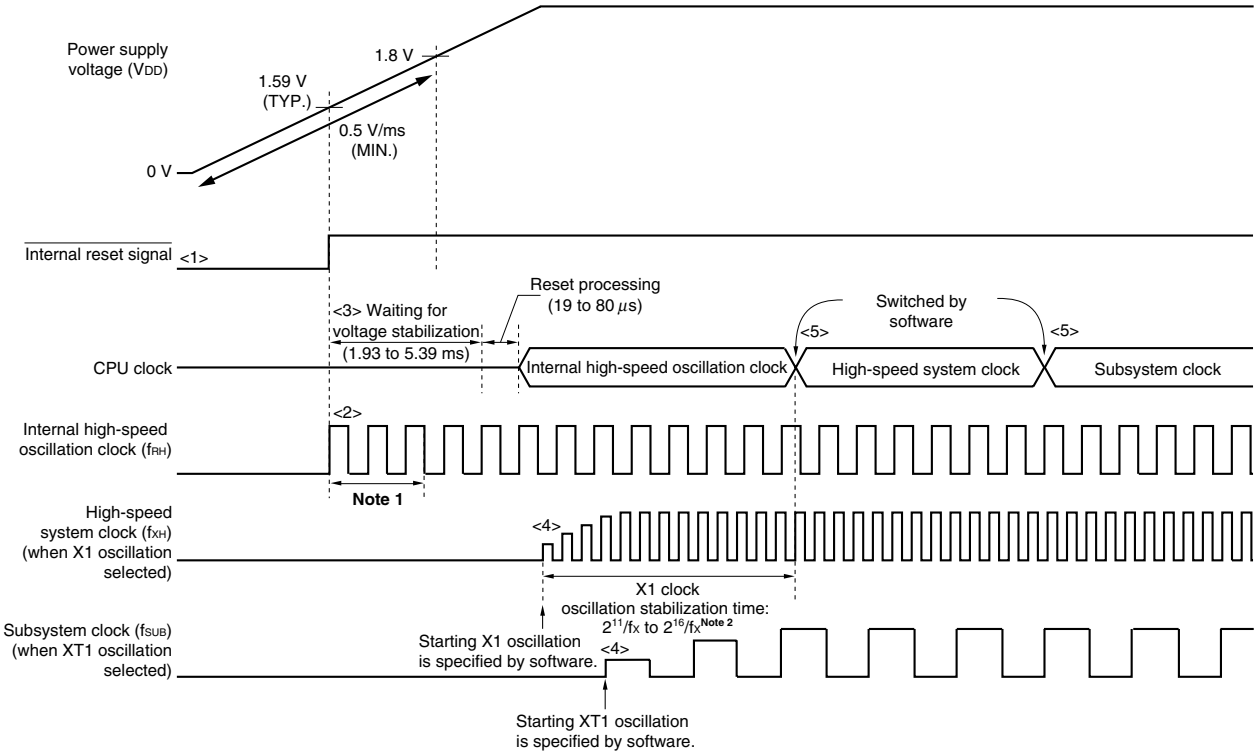


Caution 1. When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in the Figures 5-10 and 5-11 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Note that the XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption.

<R> **Figure 5-13. Clock Generator Operation When Power Supply Voltage Is Turned On (When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0))**



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 1.59 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> When the power supply voltage rises with a slope of 0.5 V/ms (MIN.), the CPU starts operation on the internal high-speed oscillation clock after the reset is released and after the stabilization times for the voltage of the power supply and regulator have elapsed, and then reset processing is performed.

<4> Set the start of oscillation of the X1 or XT1 clock via software (see **(1)** in **5.6.1 Example of controlling high-speed system clock** and **(1)** in **5.6.3 Example of controlling subsystem clock)**.

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see **(3)** in **5.6.1 Example of controlling high-speed system clock** and **(3)** in **5.6.3 Example of controlling subsystem clock**).

Notes 1. The internal voltage stabilization time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

2. When releasing a reset (above figure) or releasing STOP mode while the CPU is operating on the internal high-speed oscillation clock, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC). If the CPU operates on the high-speed system clock (X1 oscillation), set the oscillation stabilization time when releasing STOP mode using the oscillation stabilization time select register (OSTS).

Cautions 1. If the voltage rises with a slope of less than 0.5 V/ms (MIN.) from power application until the voltage reaches 1.8 V, input a low level to the $\overline{\text{RESET}}$ pin from power application until the voltage reaches 1.8 V, or set the 2.7 V/1.59 V POC mode by using the option byte (POCMODE = 1) (see Figure 5-14). By doing so, the CPU operates with the same timing as <2> and thereafter in Figure 5-13 after reset release by the $\overline{\text{RESET}}$ pin.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

Figure 6-9. Format of Prescaler Mode Register 00 (PRM00)

Address: FFBBH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PRM00	ES101	ES100	ES001	ES000	0	PRM002	PRM001	PRM000

ES101	ES100	TI010 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES001	ES000	TI000 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

PRM002	PRM001	PRM000	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}[Note 2]	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	1	$f_{PRS}/2^4$	1.25 MHz	2.5 MHz	625 kHz
1	0	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	0	1	f_{SUB}	32.768 kHz		
1	1	0	TI000 valid edge[Note 3]			
1	1	1	TM52 output			

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.
- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of PRM002 = PRM001 = PRM000 = 0 (count clock: f_{PRS}) is prohibited.

3. The external clock from the TI000 pin requires a pulse longer than twice the cycle of the peripheral hardware clock (f_{PRS}).

Caution Do not select the valid edge of TI000 as the count clock during the pulse width measurement.

Remarks 1. 8-bit timer/event counter 52 (TM52) output can be selected as the TM00 count clock by setting PRM002, PRM001, PRM000 = 1, 1, 1. Any frequency can be set as the 16-bit timer (TM00) count clock, depending on the TM52 count clock and compare register setting values.

2. f_{PRS}: Peripheral hardware clock frequency
f_{SUB}: Subsystem clock frequency

6.4.3 External event counter operation

When bits 1 and 0 (PRM001 and PRM000) of the prescaler mode register 00 (PRM00) are set to 11 (for counting up with the valid edge of the TI000 pin) and bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 11, the valid edge of an external event input is counted, and a match interrupt signal indicating matching between TM00 and CR000 (INTTM000) is generated.

To input the external event, the TI000 pin is used. Therefore, the timer/event counter cannot be used as an external event counter in the clear & start mode entered by the TI000 pin valid edge input (when TMC003 and TMC002 = 10).

The INTTM000 signal is generated with the following timing.

- Timing of generation of INTTM000 signal (second time or later)
  = Number of times of detection of valid edge of external event × (Set value of CR000 + 1)

However, the first match interrupt immediately after the timer/event counter has started operating is generated with the following timing.

- Timing of generation of INTTM000 signal (first time only)
  = Number of times of detection of valid edge of external event input × (Set value of CR000 + 2)

To detect the valid edge, the signal input to the TI000 pin is sampled during the clock cycle of f_{PRS}. The valid edge is not detected until it is detected two times in a row. Therefore, a noise with a short pulse width can be eliminated.

Remarks 1. For the setting of I/O pins, see **6.3 (6) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

Figure 6-20. Block Diagram of External Event Counter Operation

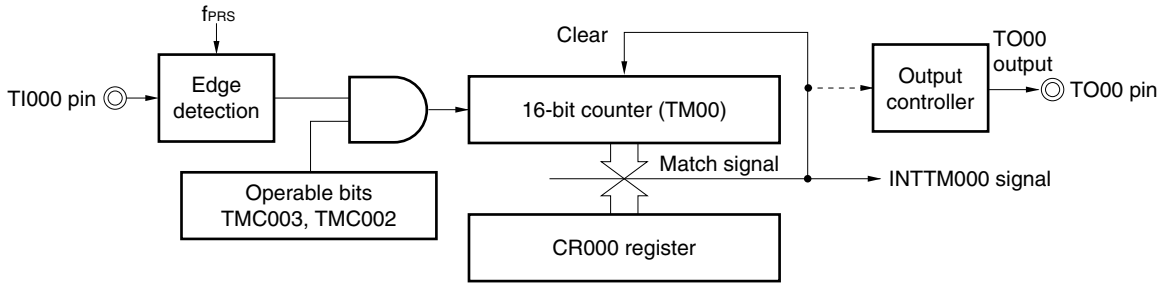
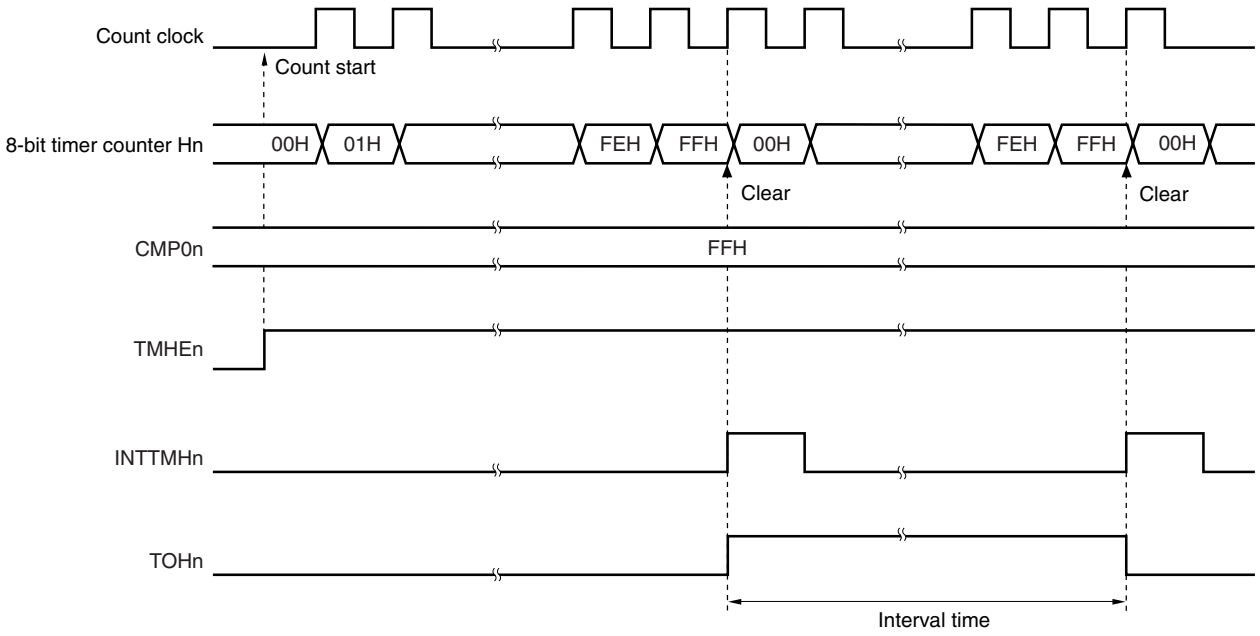
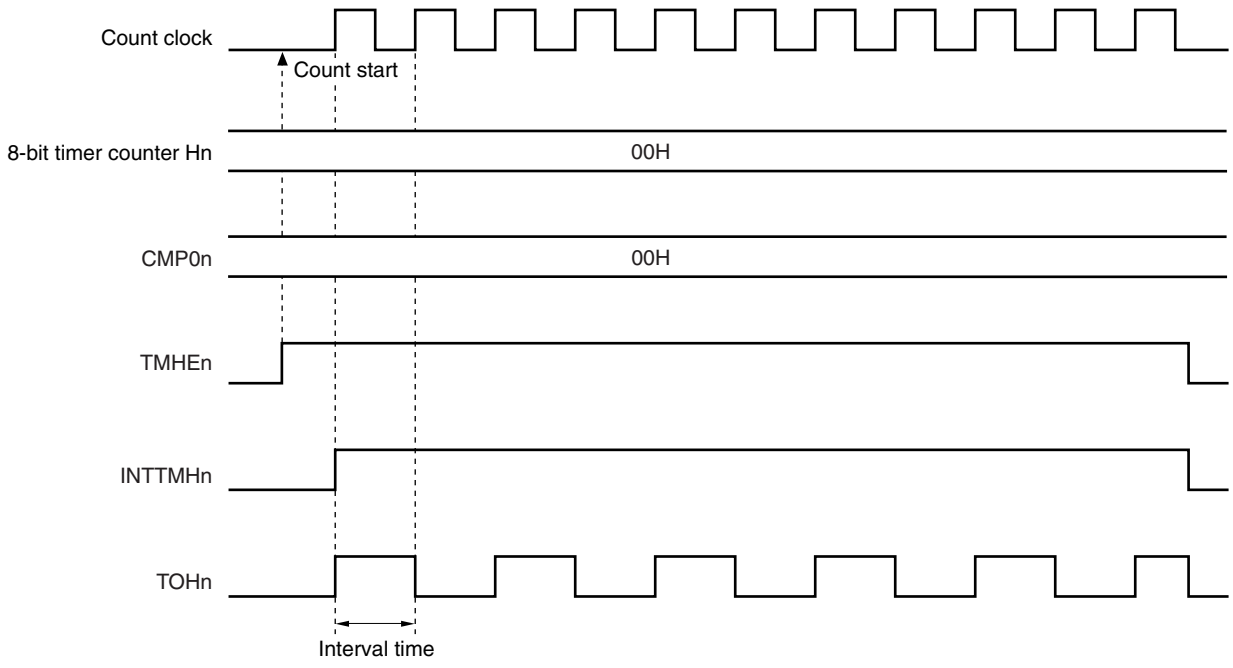


Figure 8-12. Timing of Interval Timer/Square-Wave Output Operation (2/2)

(b) Operation when CMP0n = FFH



(c) Operation when CMP0n = 00H



Remark n = 0 to 2, however, TOH0 and TOH1 only for TOHn

10.3 Register Controlling Watchdog Timer

The watchdog timer is controlled by the watchdog timer enable register (WDTE).

(1) Watchdog timer enable register (WDTE)

Writing ACH to WDTE clears the watchdog timer counter and starts counting again.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 9AH or 1AH[Note].

Figure 10-2. Format of Watchdog Timer Enable Register (WDTE)

Address: FF99H After reset: 9AH/1AH[Note] R/W

Symbol	7	6	5	4	3	2	1	0
WDTE								

Note The WDTE reset value differs depending on the WDTON setting value of the option byte (0080H). To operate watchdog timer, set WDTON to 1.

WDTON Setting Value	WDTE Reset Value
0 (watchdog timer count operation disabled)	1AH
1 (watchdog timer count operation enabled)	9AH

Cautions 1. If a value other than ACH is written to WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

2. If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

3. The value read from WDTE is 9AH/1AH (this differs from the written value (ACH)).

(5) 16-bit ΔΣ type A/D conversion status register (ADDSTR)

This register holds the channel for which A/D conversion has been completed. It also checks which channel has completed conversion.

ADDSTR can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-6. Format of 16-Bit ΔΣ type A/D Conversion Status Register (ADDSTR)

Address: FF75H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ADDSTR	0	0	0	0	0	0	ADDIT1	ADDIT0

ADDIT1	ADDIT0	Channel converted by 16-bit ΔΣ type A/D conversion	
		When differential input is selected	When single input is selected
0	0	DS0+/DS0-	DS0+
0	1	DS1+/DS1-	DS1+
1	0	DS2+/DS2-	DS2+

(d) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P32/TOH0/MCGO pin for Manchester code output, clear PM32 to 0 and clear the output latch of P32 to 0.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

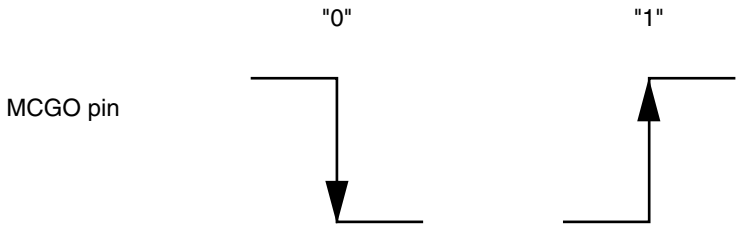
Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(2) Format of "0" and "1" of Manchester code output

The format of "0" and "1" of Manchester code output in 78K0/LF3 is as follows.



(d) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P32/TOH0/MCGO pin for bit sequential data output, clear PM32 to 0 and clear the output latch of P32 to 0.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(3) Type C reception mode

The INTRERR signal is generated under any of the following conditions.

- Counter < RMDLS at the rising edge of $\overline{\text{RIN}}$
- Register changes so that RMDLL ≤ counter while $\overline{\text{RIN}}$ is at low level
- Counter < RMDH0S at the falling edge of $\overline{\text{RIN}}$
- RMDH0L ≤ counter < RMDH1S at the falling edge of $\overline{\text{RIN}}$
- RMDH1L ≤ counter and counter after RMDH1L < RMER at the falling edge of $\overline{\text{RIN}}$

However, before the first INTDFULL interrupt is generated, INTRERR signal will not be generated.

The generation timing of the INTRERR signal is shown in Figure 20-15.

CHAPTER 25 POWER-ON-CLEAR CIRCUIT

25.1 Functions of Power-on-Clear Circuit

The power-on-clear circuit (POC) has the following functions.

- Generates internal reset signal at power on.
  In the 1.59 V POC mode (option byte: POCMODE = 0), the reset signal is released when the supply voltage (V_{DD}) exceeds 1.59 V ±0.15 V.
  In the 2.7 V/1.59 V POC mode (option byte: POCMODE = 1), the reset signal is released when the supply voltage (V_{DD}) exceeds 2.7 V ±0.2 V.

- Compares supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V), generates internal reset signal when $V_{DD} < V_{POC}$.

Caution If an internal reset signal is generated in the POC circuit, the reset control flag register (RESF) is cleared to 00H.

Remark 78K0/LF3 incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT) or low-voltage-detector (LVI). RESF is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by WDT or LVI.
For details of RESF, see **CHAPTER 24 RESET FUNCTION**.

Figure 25-3. Example of Software Processing After Reset Release (2/2)

• Checking reset source

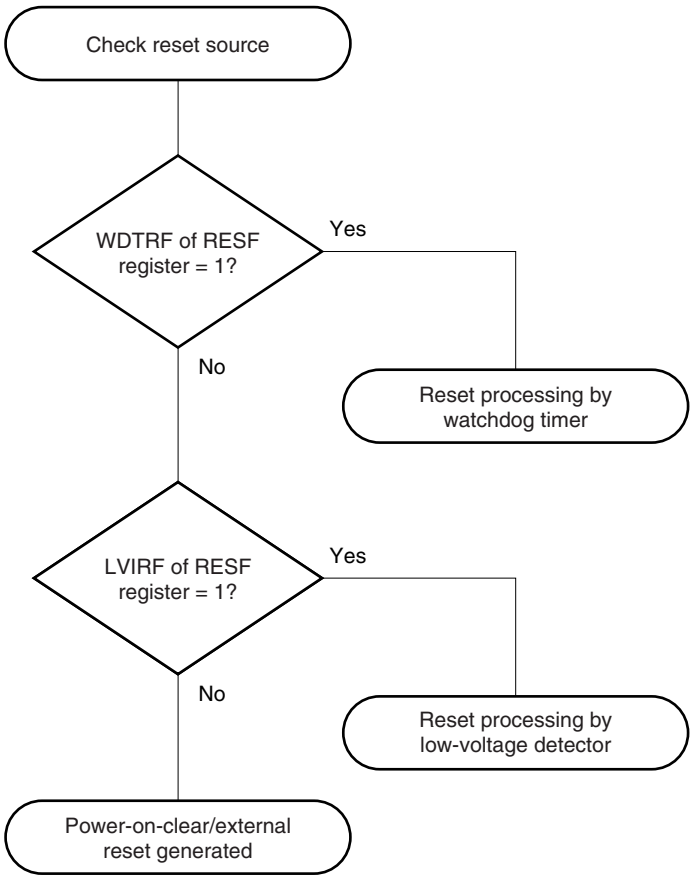
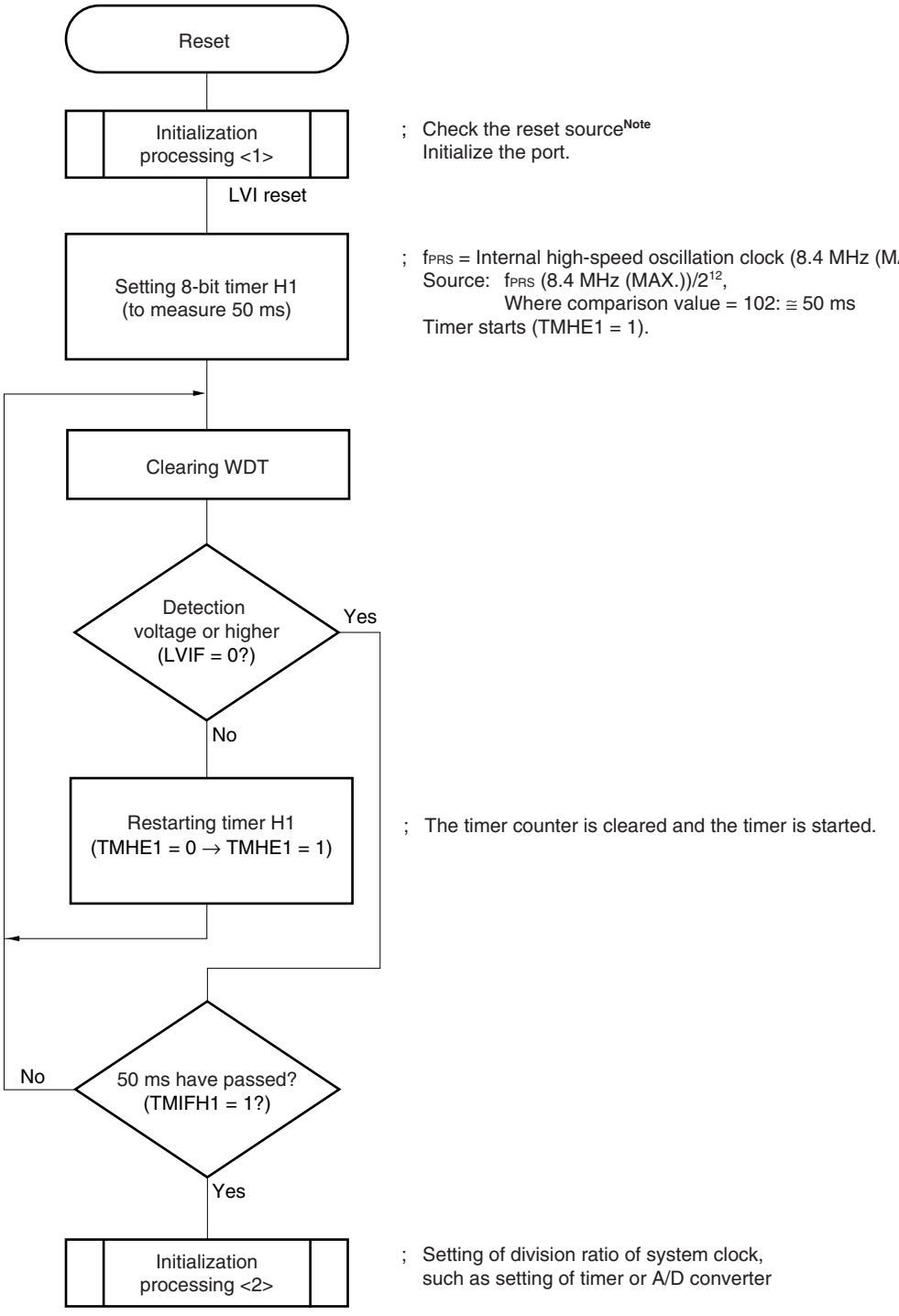


Figure 26-9. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage



Note A flowchart is shown on the next page.

Table 28-12. Processing Time for Each Command When PG-FP5 Is Used (Reference) (2/3)

(3) μPD78F0473, 78F0483, 78F0493 (Products with internal ROM: 32 KB)

Command of PG-FP5	Port: CSI-Internal-OSC (internal high-speed oscillation clock (f_{RH})) Speed: 2.5 MHz	Port: UART-Internal-OSC (internal high-speed oscillation clock (f_{RH})) Speed: 115200 bps	Port:UART-Ext-OSC (X1 clock (f_X)) Speed:115200 bps		Port:UART-Ext-FP5CLK (External main system clock (f_{EXCLK})) Speed:115200 bps	
			Frequency: 2.0 MHz	Frequency: 10 MHz	Frequency: 2.0 MHz	Frequency: 10 MHz
Signature	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Blankcheck	1.5 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Erase	1.5 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Program	4.5 s (TYP.)	6.5 s (TYP.)	6.5 s (TYP.)	6.5 s (TYP.)	6.5 s (TYP.)	6.5 s (TYP.)
Verify	2.5 s (TYP.)	5 s (TYP.)	5 s (TYP.)	5 s (TYP.)	5 s (TYP.)	5 s (TYP.)
E.P.V	5.5 s (TYP.)	7 s (TYP.)	7 s (TYP.)	7 s (TYP.)	7 s (TYP.)	7 s (TYP.)
Checksum	1.5 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Security	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)

(4) μPD78F0474, 78F0484, 78F0494 (Products with internal ROM: 48 KB)

Command of PG-FP5	Port: CSI-Internal-OSC (internal high-speed oscillation clock (f_{RH})) Speed: 2.5 MHz	Port: UART-Internal-OSC (internal high-speed oscillation clock (f_{RH})) Speed: 115200 bps	Port:UART-Ext-OSC (X1 clock (f_X)) Speed:115200 bps		Port:UART-Ext-FP5CLK (External main system clock (f_{EXCLK})) Speed:115200 bps	
			Frequency: 2.0 MHz	Frequency: 10 MHz	Frequency: 2.0 MHz	Frequency: 10 MHz
Signature	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Blankcheck	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)
Erase	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)
Program	6.5 s (TYP.)	9.5 s (TYP.)	9.5 s (TYP.)	9.5 s (TYP.)	9.5 s (TYP.)	9.5 s (TYP.)
Verify	3.5 s (TYP.)	7 s (TYP.)	7 s (TYP.)	7 s (TYP.)	7 s (TYP.)	7 s (TYP.)
E.P.V	7.5 s (TYP.)	10 s (TYP.)	10 s (TYP.)	10 s (TYP.)	10 s (TYP.)	10 s (TYP.)
Checksum	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)
Security	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)

Caution When executing boot swapping, do not use the E.P.V. command with the dedicated flash memory programmer.

Table 28-14. Interrupt Response Time (Library for Normal Model) (1/2)

Function Name	Interrupt Response Time (Unit: μs)					
	When entry RAM is allocated outside short direct addressing range			When entry RAM is allocated within short direct addressing range		
	RSTOP = 0 and RSTS = 1 (during stable operation of internal high-speed oscillator)		RSTOP = 1 (internal high-speed oscillator stopped)Note	RSTOP = 0 and RSTS = 1 (during stable operation of internal high-speed oscillator)		RSTOP = 1 (internal high-speed oscillator stopped)Note
	MCS = 0 (CPU operates with internal high-speed oscillation clock)	MCS = 1 (CPU operates with high-speed system clock)	MCS = 1 (CPU operates with high-speed system clock)	MCS = 0 (CPU operates with internal high-speed oscillation clock)	MCS = 1 (CPU operates with high-speed system clock)	MCS = 1 (CPU operates with high-speed system clock)
Block erase function	179/fCPU+1269	179/fCPU+1269	179/fCPU+1912	179/fCPU+703	179/fCPU+703	179/fCPU+713
Word write function	333/fCPU+1098	333/fCPU+1098	333/fCPU+1742	333/fCPU+533	333/fCPU+533	333/fCPU+543
Block verify function	179/fCPU+1013	179/fCPU+1013	179/fCPU+1656	179/fCPU+448	179/fCPU+448	179/fCPU+456
Block blank check function	179/fCPU+993	179/fCPU+993	179/fCPU+1637	179/fCPU+428	179/fCPU+428	179/fCPU+438
Set information function	80/fCPU+833	80/fCPU+833	80/fCPU+1477	80/fCPU+346	80/fCPU+346	80/fCPU+346
EEPROM write function	333/fCPU+1107	333/fCPU+1107	333/fCPU+1751	333/fCPU+542	333/fCPU+542	333/fCPU+552

Note This is the function processing time when the function is executed immediately after the self programming start function has been executed. The processing time after a function other than the self programming start function has been executed is the same as that of RSTOP = 0.

Remark RSTOP: Bit 0 of the internal oscillation mode register (RCM)
RSTS: Bit 7 of RCM
MCS: Bit 1 of main clock mode register (MCM)
f_{CPU}: CPU clock frequency
W: Number of words to be written (1 word = 4 bytes)

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second Operand / First Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

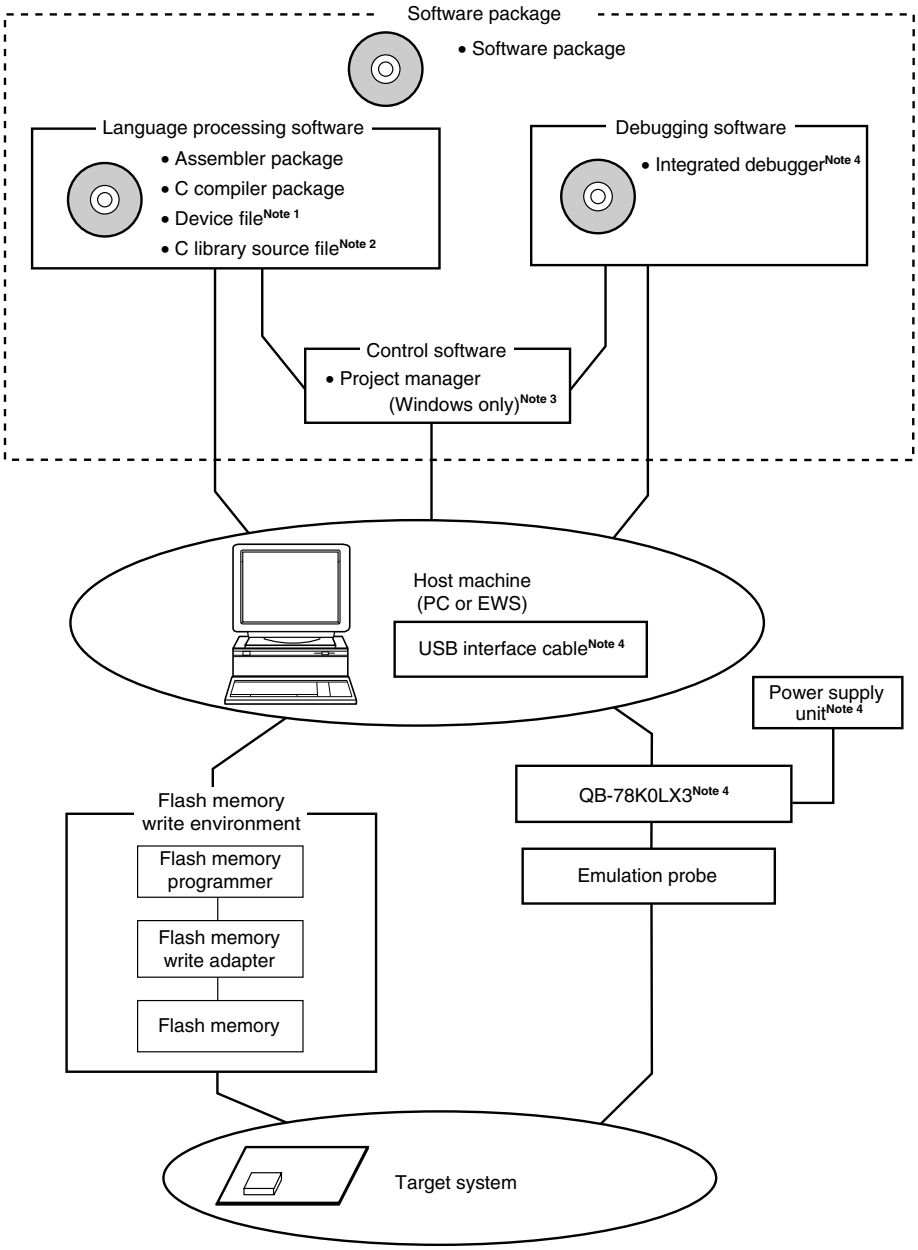
(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second Operand / First Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

Figure A-1. Development Tool Configuration (1/2)

(1) When using the in-circuit emulator QB-78K0LX3



Notes 1. Download the device file (DF780495) for the 78K0/LF3 from the download site for development tools (http://www.necel.com/micro/ods/eng/index.html).

2. The C library source file is not included in the software package.

3. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

4. The QB-78K0LX3 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, a power supply unit, the on-chip debug emulator QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board. Any other products are sold separately.
Download the software for operating the QB-MINI2 from the download site for development tools (http://www.necel.com/micro/ods/eng/index.html) when using the QB-MINI2.