Renesas Electronics America Inc - UPD78F0482GC-GAD-AX Datasheet

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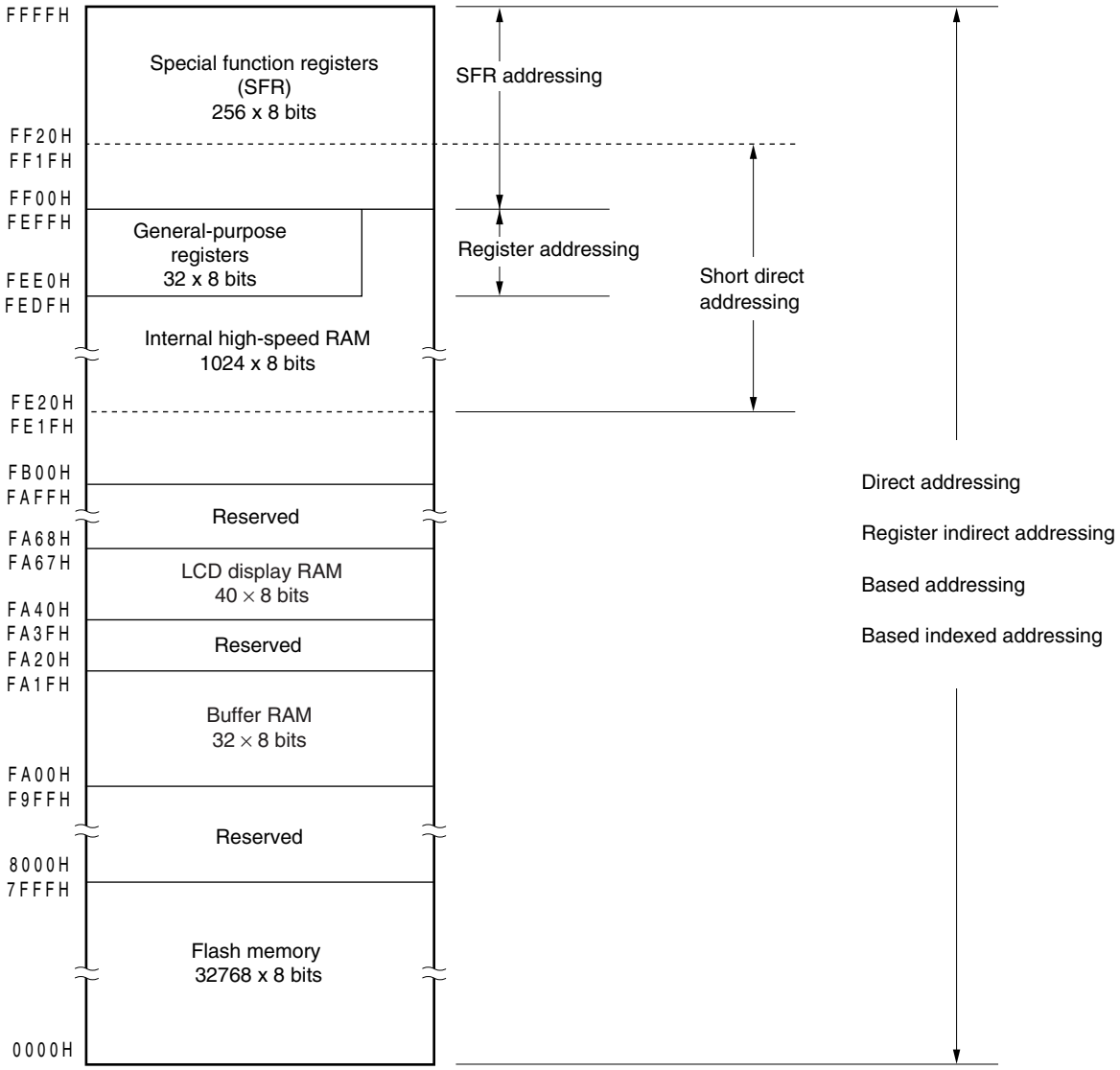
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0482gc-gad-ax

Figure 3-15. Correspondence Between Data Memory and Addressing (μPD78F0473, 78F0483)



4.2.11 Port 14

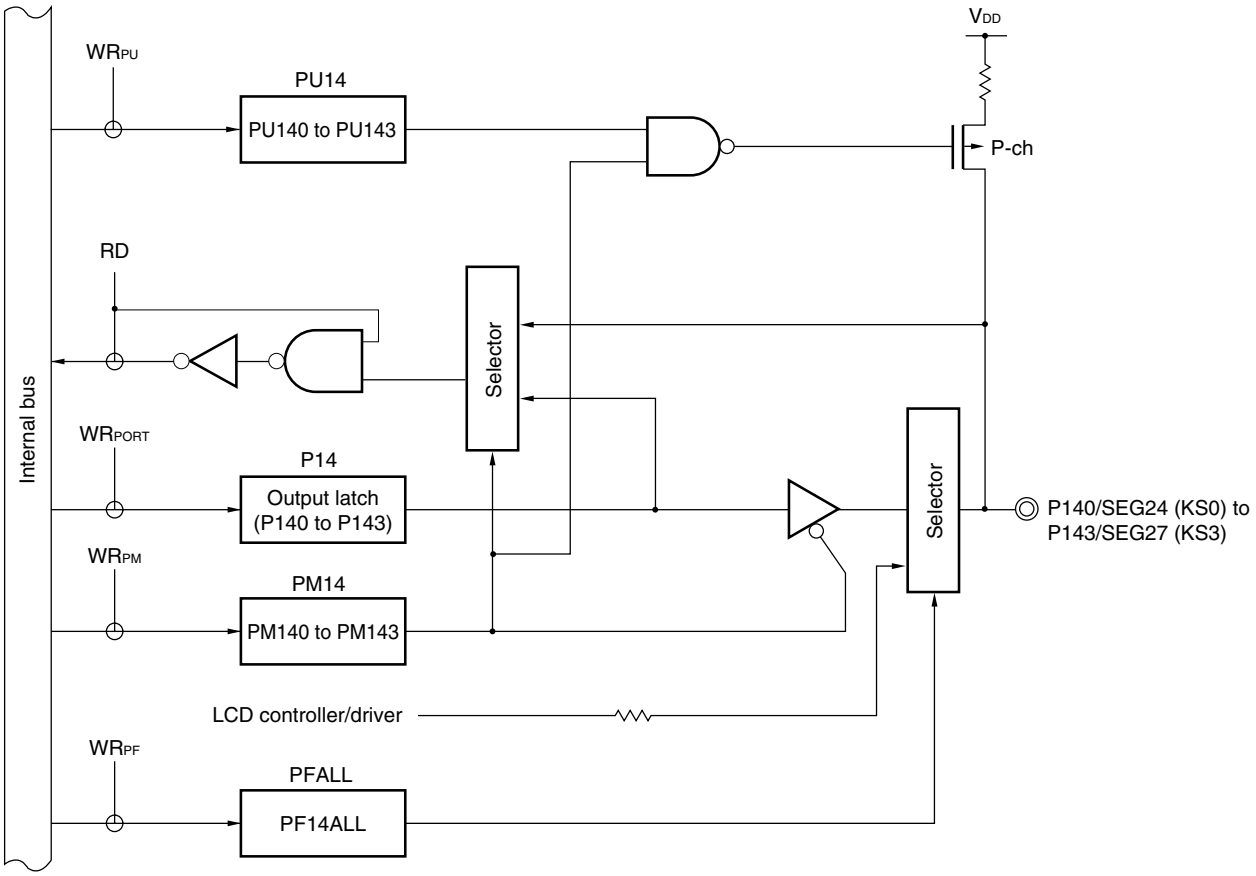
Port 14 is a 4-bit I/O port with an output latch. Port 14 can be set to the input mode or output mode in 1-bit units using port mode register 14 (PM14). When the P140 to P143 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 14 (PU14).

This port can also be used for segment output.

Reset signal generation sets port 14 to input mode.

Figure 4-25 shows a block diagram of port 14.

Figure 4-25. Block Diagram of P140 and P143



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

Notes 1. μPD78F048x and 78F049x only.

2. The functions of the P20/ANI0/DS0−, P21/ANI1/DS0+, P22/ANI2/DS1−, P23/ANI3/DS1+, P24/ANI4/DS2−, P25/ANI5/DS2+, P26/ANI6/REF−, and P27/ANI7/REF+ pins are determined according to the settings of port function register 2 (PF2), A/D port configuration register 0 (ADPC0), port mode register 2 (PM2), analog input channel specification register (ADS), and ΔΣ A/D converter mode register 0 (ADDCTL0).

Table 4-6. Setting Functions of P20/SEG39[Note 1]/ANI0[Note 2]/DS0−[Note 3] to P27/SEG32[Note 1]/ANI7[Note 2]/REF+[Note 3] Pins

PF2[Note 1]	ADPC0	PM2	ADS	ADDCTL0	P20/SEG39[Note 1]/ANI0[Note 2]/DS0−[Note 3] to P27/SEG32[Note 1]/ANI7[Note 2]/REF+[Note 3] Pins
Digital/Analog selection	Analog input selection	Input mode	Does not select ANI.	Does not select DSn±.	Analog input (not to be converted)
			Selects ANI.	Does not select DSn±.	Analog input (to be converted by successive approximation type A/D converter)
			Does not select ANI.	Selects DSn±.	Analog input (to be converted by 16-bit ΔΣ type A/D converter)
			Selects ANI.	Selects DSn±.	Setting prohibited
		Output mode	−		Setting prohibited
	Digital I/O selection	Input mode	−		Digital input
		Output mode	−		Digital output
SEG output selection[Note 1]	−	−	−		Segment output[Note 1]

Notes 1. μPD78F047x and 78F048x only.

2. μPD78F048x and 78F049x only.

3. μPD78F049x only.

Remark n = 0 to 2

3. When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **5.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 are Input port pins).

4. Targeted at registers corresponding to each port.

5. RxD6 can be set as the input source for TI000 by setting ISC1 = 1.

6. Input enable of TM52 via TMH2 can be controlled by setting ISC2 = 1.

7. RxD6 can be set as the input source for INTP0 by setting ISC0 = 1.

8. μPD78F049x only.

9. When the P40/KR0/V_{LC3} pin is set to the 1/4 bias method, it is used as V_{LC3}. When the pin is set to another bias method, it is used for the port function (P40) or the key interrupt function (KR0).

10. Set PF13 = 0 when using as port function.

11. Set PF16 = 0 when using as port function.

12. μPD78F047x and 78F048x only.

Remarks 1. ×: Don't care
−: Does not apply.
PM××: Port mode register
P××: Port output latch

2. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

3. X1, X2 pins can be used as on-chip debug mode setting pins (OCD1A, OCD1B) when the on-chip debug function is used. For detail, see **CHAPTER 29 ON-CHIP DEBUG FUNCTION.**

5.6.7 Condition before changing CPU clock and processing after changing CPU clock

Condition before changing the CPU clock and processing after changing the CPU clock are shown below.

Table 5-6. Changing CPU Clock

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Internal high-speed oscillation clock	X1 clock	Stabilization of X1 oscillation • MSTOP = 0, OSCSEL = 1, EXCLK = 0 • After elapse of oscillation stabilization time	• Internal high-speed oscillator can be stopped (RSTOP = 1).
	External main system clock	Enabling input of external clock from EXCLK pin • MSTOP = 0, OSCSEL = 1, EXCLK = 1	
X1 clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator • RSTOP = 0	X1 oscillation can be stopped (MSTOP = 1).
External main system clock			External main system clock input can be disabled (MSTOP = 1).
Internal high-speed oscillation clock	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1 • After elapse of oscillation stabilization time	Operating current can be reduced by stopping internal high-speed oscillator (RSTOP = 1).
X1 clock			X1 oscillation can be stopped (MSTOP = 1).
External main system clock			External main system clock input can be disabled (MSTOP = 1).
XT1 clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator and selection of internal high-speed oscillation clock as main system clock • RSTOP = 0, MCS = 0	XT1 oscillation can be stopped (OSCSELS = 0).
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • MSTOP = 0, OSCSEL = 1, EXCLK = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from EXCLK pin and selection of high-speed system clock as main system clock • MSTOP = 0, OSCSEL = 1, EXCLK = 1 • MCS = 1	

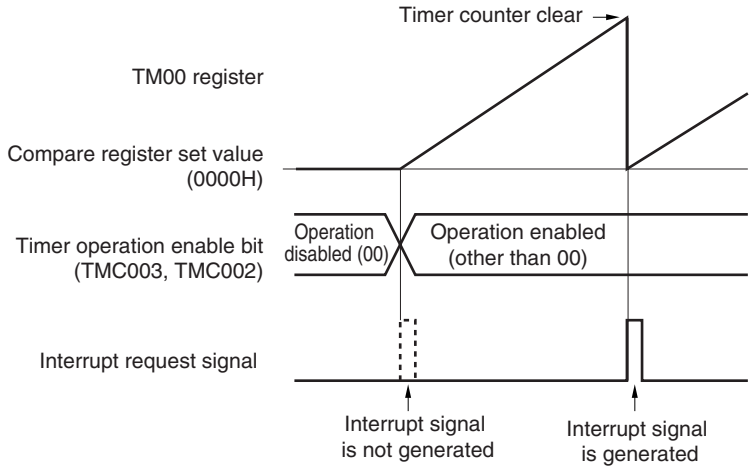
(iii) Setting range when CR000 or CR010 is used as a compare register

When CR000 or CR010 is used as a compare register, set it as shown below.

Operation	CR000 Register Setting Range	CR010 Register Setting Range
Operation as interval timer	0000H < N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH Normally, this setting is not used. Mask the match interrupt signal (INTTM010).
Operation as square-wave output		
Operation as external event counter		
Operation in the clear & start mode entered by TI000 pin valid edge input	0000H[Note] ≤ N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH
Operation as free-running timer		
Operation as PPG output	M < N ≤ FFFFH	0000H[Note] ≤ M < N
Operation as one-shot pulse output	0000H[Note] ≤ N ≤ FFFFH (N ≠ M)	0000H[Note] ≤ M ≤ FFFFH (M ≠ N)

Note When 0000H is set, a match interrupt immediately after the timer operation does not occur and timer output is not changed, and the first match timing is as follows. A match interrupt occurs at the timing when the timer counter (TM00 register) is changed from 0000H to 0001H.

- When the timer counter is cleared due to overflow
- When the timer counter is cleared due to TI000 pin valid edge (when clear & start mode is entered by TI000 pin valid edge input)
- When the timer counter is cleared due to compare match (when clear & start mode is entered by match between TM00 and CR000 (CR000 = other than 0000H, CR010 = 0000H))



Remarks 1. N: CR000 register set value, M: CR010 register set value

2. For details of TMC003 and TMC002, see **6.3 (1) 16-bit timer mode control register 00 (TMC00)**.

6.4 Operation of 16-Bit Timer/Event Counter 00

6.4.1 Interval timer operation

If bits 3 and 2 (TMC003 and TMC002) of the 16-bit timer mode control register (TMC00) are set to 11 (clear & start mode entered upon a match between TM00 and CR000), the count operation is started in synchronization with the count clock.

When the value of TM00 later matches the value of CR000, TM00 is cleared to 0000H and a match interrupt signal (INTTM000) is generated. This INTTM000 signal enables TM00 to operate as an interval timer.

Remarks 1. For the setting of I/O pins, see **6.3 (6) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 interrupt, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

Figure 6-12. Block Diagram of Interval Timer Operation

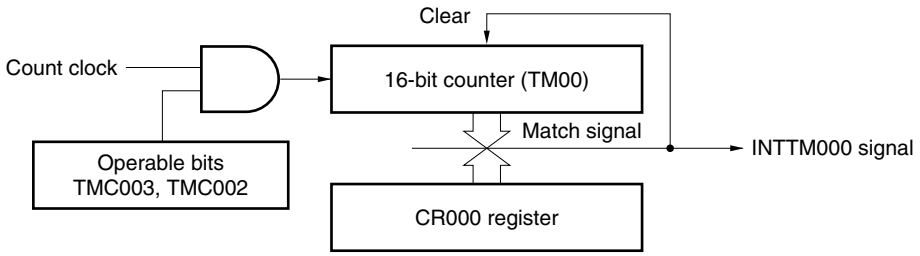


Figure 6-13. Basic Timing Example of Interval Timer Operation

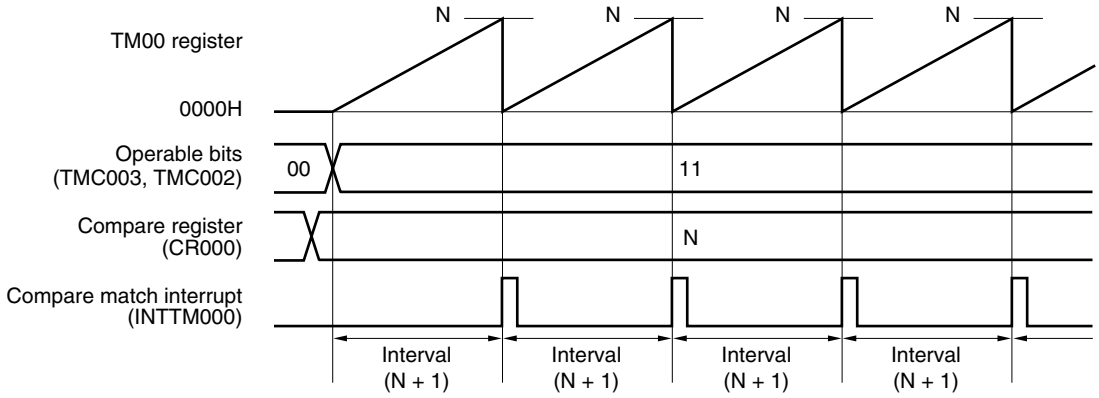
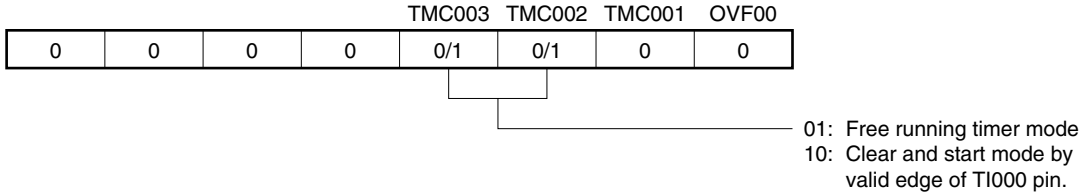
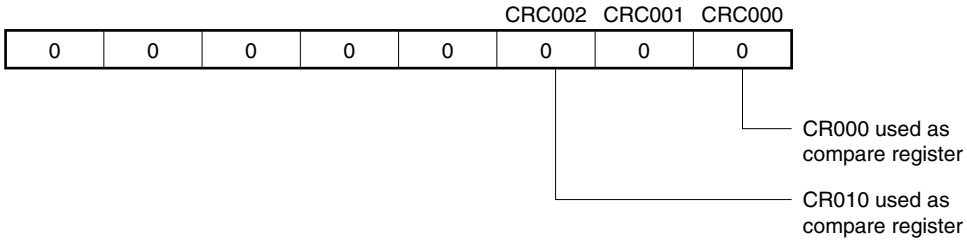


Figure 6-45. Example of Register Settings for One-Shot Pulse Output Operation (1/2)

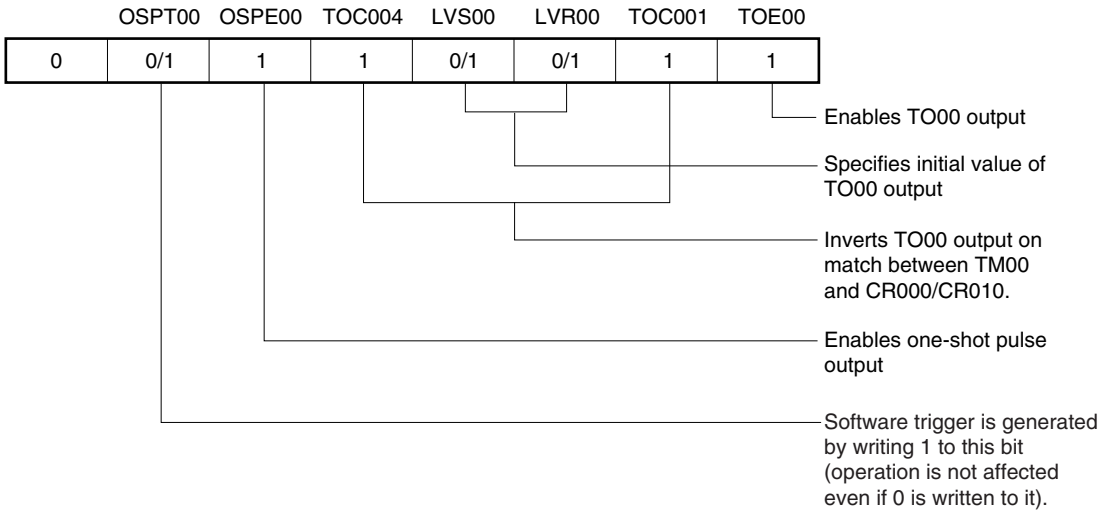
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)

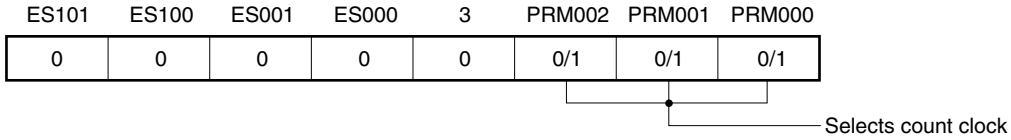
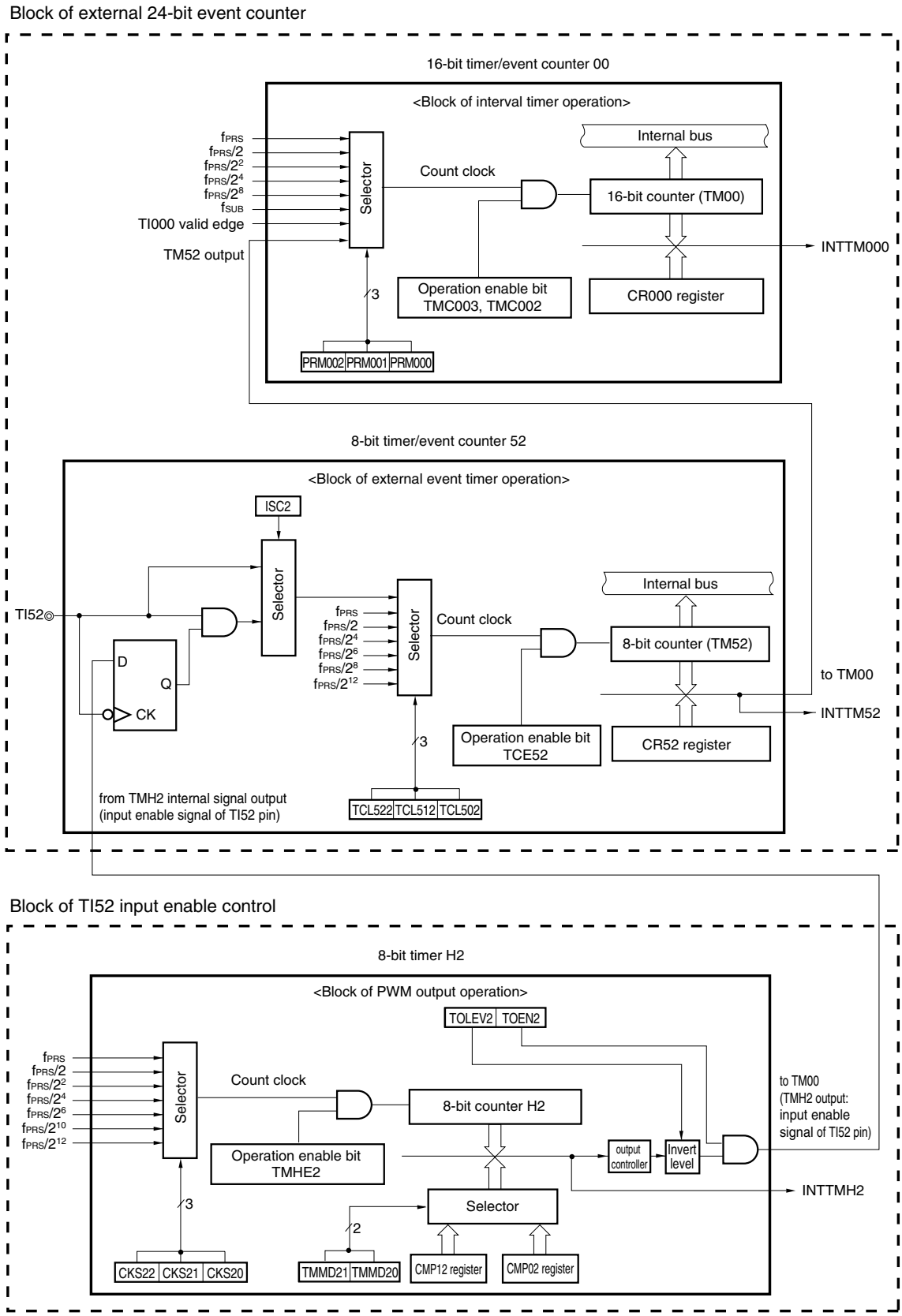


Figure 6-54. Configuration Diagram of External 24-bit Event Counter



Notes 3. Note the following points when selecting the TM50 output as the count clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)

  Start the operation of the 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)

  Start the operation of the 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

Cautions 1. When TMHE0 = 1, setting the other bits of TMHMD0 is prohibited. However, TMHMD0 can be refreshed (the same value is written).

2. In the PWM output mode, be sure to set the 8-bit timer H compare register 10 (CMP10) when starting the timer count operation (TMHE0 = 1) after the timer count operation was stopped (TMHE0 = 0) (be sure to set again even if setting the same value to CMP10).

3. The actual TOH0/P32/MCGO pin output is determined depending on PM32 and P32, besides TOH0 output.

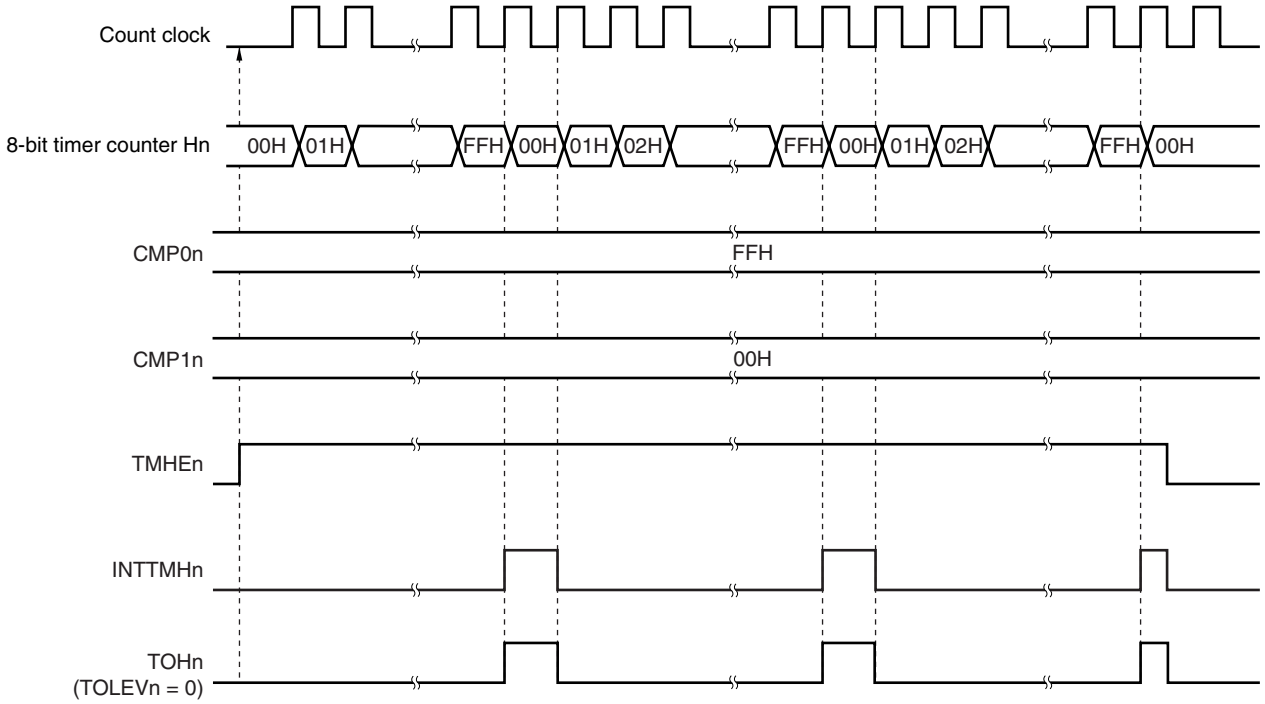
Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)

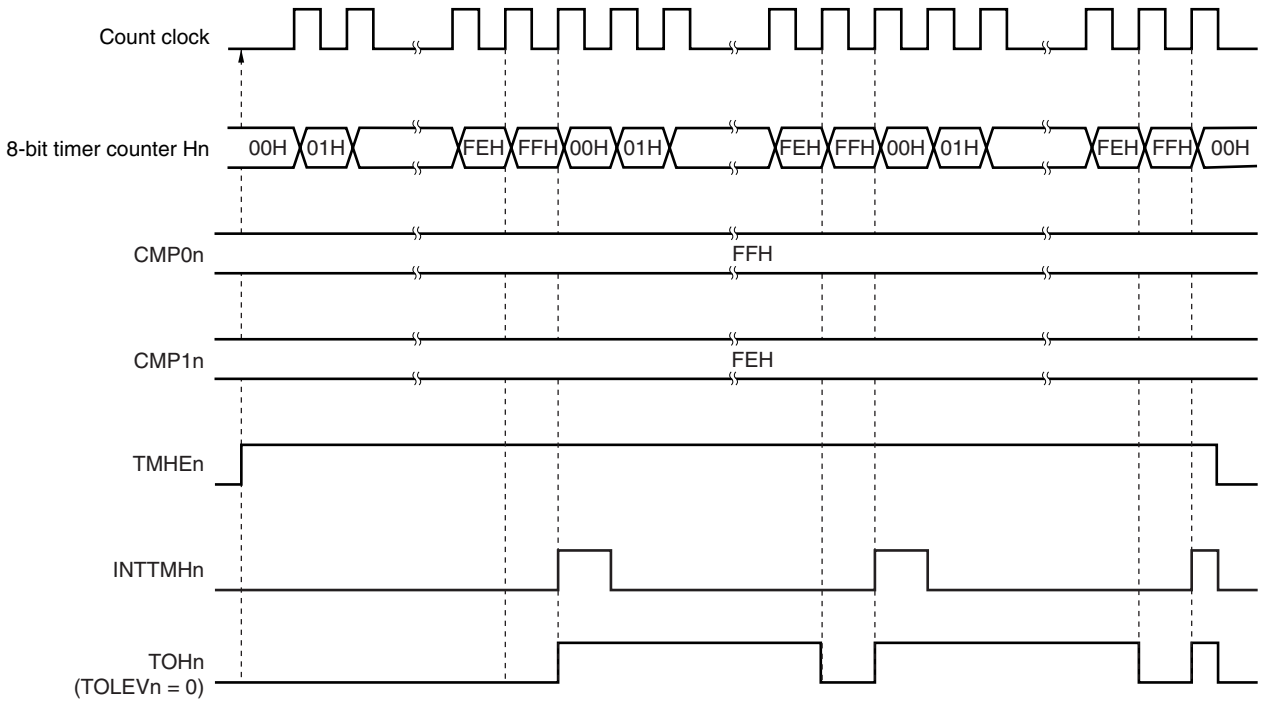
TMC501: Bit 1 of TMC50

Figure 8-14. Operation Timing in PWM Output Mode (2/4)

(b) Operation when CMP0n = FFH, CMP1n = 00H



(c) Operation when CMP0n = FFH, CMP1n = FEH



Remark n = 0 to 2, however, TOH0 and TOH1 only for TOHn

12.4.3 A/D converter operation mode

The operation mode of the A/D converter is the select mode. One channel of analog input is selected from ANI0 to ANI7 by the analog input channel specification register (ADS) and A/D conversion is executed.

(1) A/D conversion operation

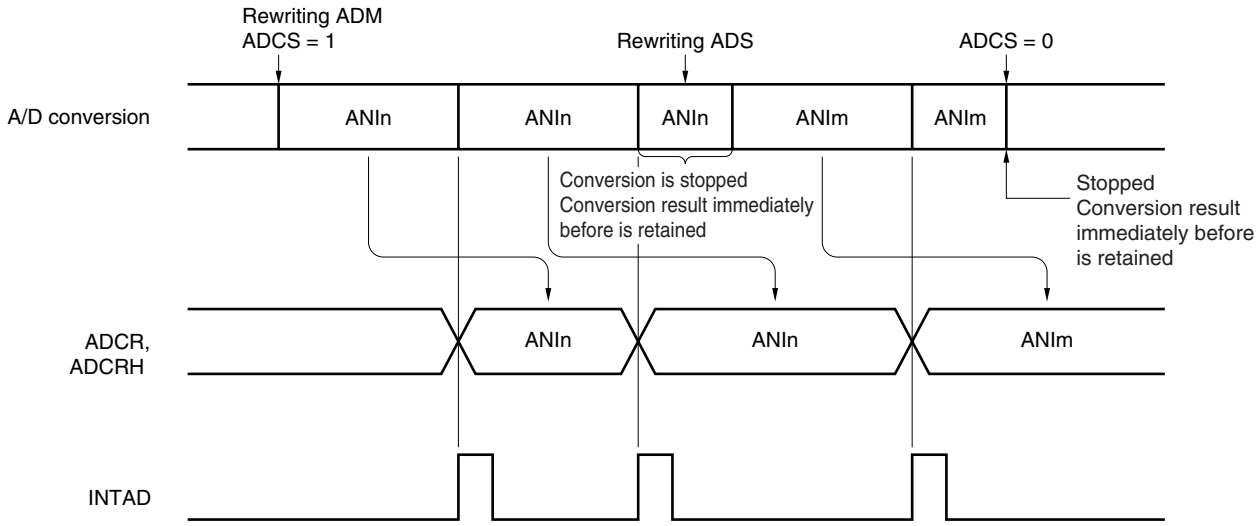
By setting bit 7 (ADCS) of the A/D converter mode register (ADM) to 1, the A/D conversion operation of the voltage, which is applied to the analog input pin specified by the analog input channel specification register (ADS), is started.

When A/D conversion has been completed, the result of the A/D conversion is stored in the A/D conversion result register (ADCR), and an interrupt request signal (INTAD) is generated. When one A/D conversion has been completed, the next A/D conversion operation is immediately started.

If ADS is rewritten during A/D conversion, the A/D conversion operation under execution is stopped and restarted from the beginning.

If 0 is written to ADCS during A/D conversion, A/D conversion is immediately stopped. At this time, the conversion result immediately before is retained.

Figure 12-13. A/D Conversion Operation



Remarks 1. n = 0 to 7

2. m = 0 to 7

13.3 Registers Used in 16-Bit ΔΣ Type A/D Converter

The 16-bit ΔΣ type A/D converter uses the following nine registers.

- 16-bit ΔΣ type A/D converter control register 0 (ADDCTL0)
- 16-bit ΔΣ type A/D converter control register 1 (ADDCTL1)
- 16-bit ΔΣ type A/D conversion result register (ADDCR)
- 8-bit ΔΣ type A/D conversion result register (ADDCRH)
- 16-bit ΔΣ type A/D conversion status register (ADDSTR)
- A/D port configuration register 0 (ADPC0)
- 16-bit ΔΣ type A/D sampling delay time setting enable register
- 16-bit ΔΣ type A/D sampling delay time setting register
- Port mode register 2 (PM2)

(1) 16-bit ΔΣ type A/D converter control register 0 (ADDCTL0)

This register sets the 16-bit ΔΣ type A/D circuit or control circuit power on/off state, conversion start/stop state, high-accuracy mode on/off state, ΔΣ input mode control, and analog input channel.

ADDCTL0 can be set by a 1-bit or 8-bit memory manipulation instruction.

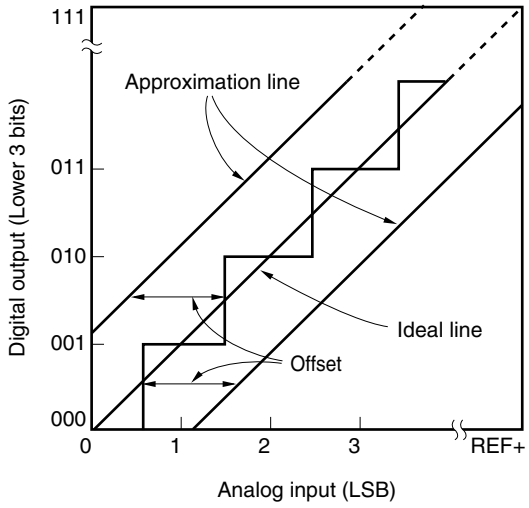
Reset signal generation clears this register to 00H.

(3) Offset (Single input)

The offset represents the difference between the approximation line of the actually measured analog input voltage values and the theoretical values (1/2 LSB).

If the approximation line is greater than the theoretical values, it shows the difference between the approximation line of the actually measured analog input voltage values and the theoretical values (3/2 LSB).

Figure 13-16. Offset (Single Input)



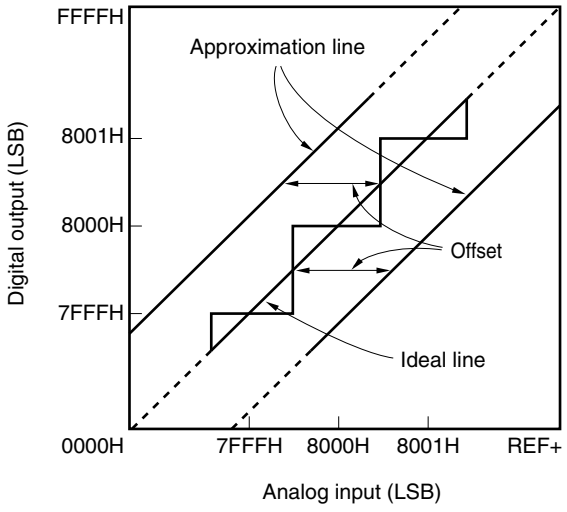
(4) Offset (Differential input)

The offset represents the difference between the approximation line of the actually measured analog input voltage values and the theoretical values (1/2 full-scale).

In the case of 16-bit resolution, the offset represents the difference between the approximation line of the actually measured analog input voltage values and the theoretical values (8000H − 1/2 LSB).

If the approximation line is greater than the theoretical values, it shows the difference between the approximation line of the actually measured analog input voltage values and the theoretical values (8000H + 1/2 LSB).

Figure 13-17. Offset (Differential Input)



(9) Conversion results just after A/D conversion start

The first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADDCE bit is set to 1 within 1.2 μs after the ADDPON bit was set to 1, or if the ADDCE bit is set to 1 with the ADDPON bit = 0. Take measures such as polling the A/D conversion end interrupt request (INTDSAD) and removing the first conversion result.

(10) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 13-22. Internal Equivalent Circuit of DSn– and DSn+ Pin

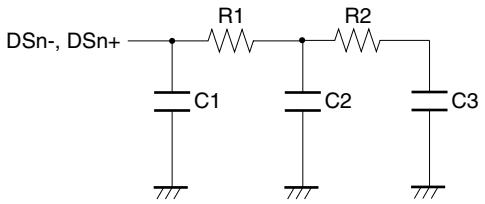


Table 13-5. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{REF}	R1	R2	C1	C2	C3
$4.0\ V \le AV_{REF} \le 5.5\ V$	8.1 kΩ	6.8 kΩ	8 pF	1.3 pF	0.22 pF
$2.7\ V \le AV_{REF} < 4.0\ V$	31 kΩ	36 kΩ	8 pF	1.3 pF	0.22 pF

Remarks 1. The resistance and capacitance values shown in Table 13-5 are not guaranteed values.

2. n = 0 to 2

(11) Simultaneous use of the 10-bit successive approximation type A/D converter and the 16-bit ΔΣ type A/D converter

The A/D conversion accuracy may deteriorate when the 10-bit successive approximation type A/D converter and the 16-bit ΔΣ type A/D converter are used at the same time.

Stop the 16-bit ΔΣ type A/D converter during 10-bit successive approximation type A/D converter operation, because the accuracy cannot be guaranteed. Also, stop the 10-bit successive approximation type A/D converter during 16-bit ΔΣ type A/D converter operation. (Do not operate them simultaneously.)

(e) Reception error

Three types of errors may occur during reception: a parity error, framing error, or overrun error. If the error flag of asynchronous serial interface reception error status register 0 (ASIS0) is set as a result of data reception, a reception error interrupt (INTSR0) is generated.

Which error has occurred during reception can be identified by reading the contents of ASIS0 in the reception error interrupt (INTSR0) servicing (see **Figure 14-3**).

The contents of ASIS0 are cleared to 0 when ASIS0 is read.

Table 14-3. Cause of Reception Error

Reception Error	Cause
Parity error	The parity specified for transmission does not match the parity of the receive data.
Framing error	Stop bit is not detected.
Overrun error	Reception of the next data is completed before data is read from receive buffer register 0 (RXB0).

(f) Noise filter of receive data

The RxD0 signal is sampled using the base clock output by the prescaler block.

If two sampled values are the same, the output of the match detector changes, and the data is sampled as input data.

Because the circuit is configured as shown in Figure 14-11, the internal processing of the reception operation is delayed by two clocks from the external signal status.

Figure 14-11. Noise Filter Circuit

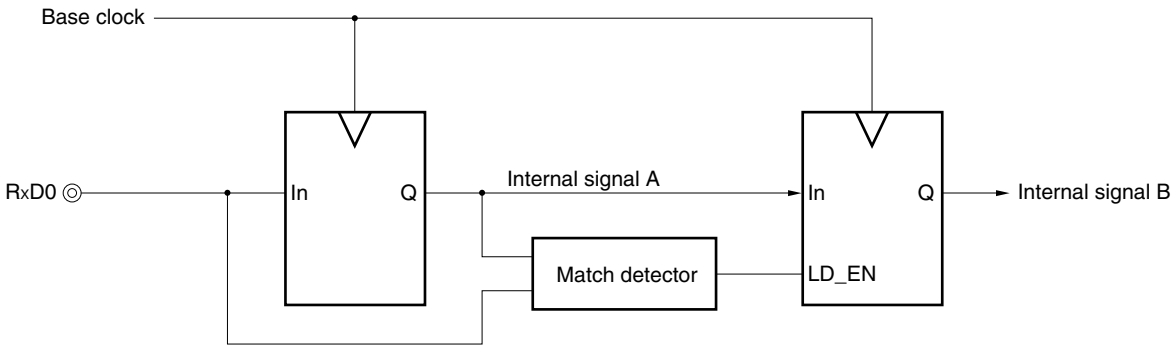
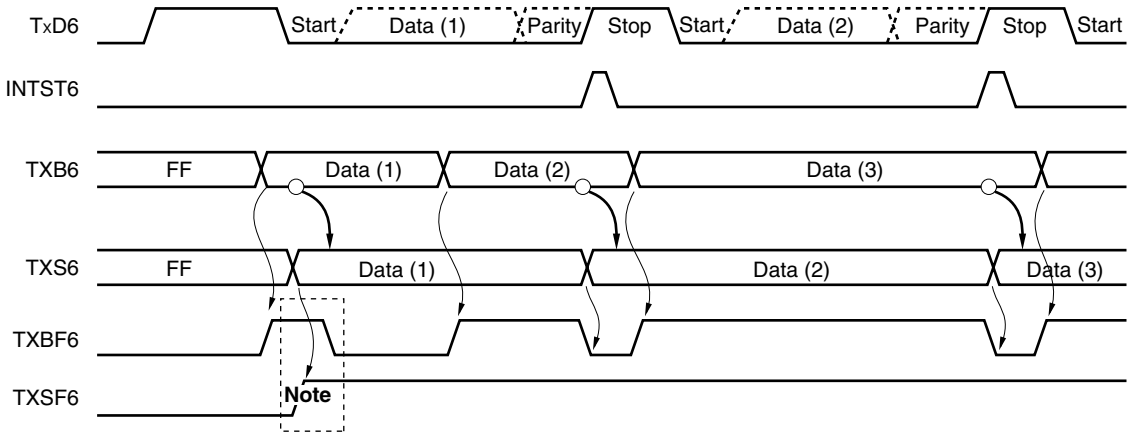


Figure 15-19 shows the timing of starting continuous transmission, and Figure 15-20 shows the timing of ending continuous transmission.

Figure 15-19. Timing of Starting Continuous Transmission



Note When ASIF6 is read, there is a period in which TXBF6 and TXSF6 = 1, 1. Therefore, judge whether writing is enabled using only the TXBF6 bit.

Remark TxD6: TxD6 pin (output)
INTST6: Interrupt request signal
TXB6: Transmit buffer register 6
TXS6: Transmit shift register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6
TXSF6: Bit 0 of ASIF6

The basic procedure of setting an operation in the 3-wire serial I/O mode is as follows.

<1> Set the CSIC10 register (see **Figures 16-3**).
<2> Set bits 4 and 6 (DIR10 and TRMD10) of the CSIM10 register (see **Figures 16-2**).
<3> Set bit 7 (CSIE10) of the CSIM10 register to 1. → Transmission/reception is enabled.
<4> Write data to transmit buffer register 10 (SOTB10). → Data transmission/reception is started.
Read data from serial I/O shift register 10 (SIO10). → Data reception is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

The relationship between the register settings and pins is shown below.

Table 16-2. Relationship Between Register Settings and Pins

CSIE10	TRMD10	PM12	P12	PM13	P13	PM11	P11	CSI10 Operation	Pin Function		
									SI10/RxD0/ P12	SO10/ TxD0/P13	$\overline{\text{SCK10}}$/ P11
0	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	Stop	RxD0/P12	TxD0/P13	P11Note 2
1	0	1	×	×Note 1	×Note 1	1	×	Slave receptionNote 3	SI10	TxD0/P13	$\overline{\text{SCK10}}$ (input)Note 3
1	1	×Note 1	×Note 1	0	0	1	×	Slave transmissionNote 3	RxD0/P12	SO10	$\overline{\text{SCK10}}$ (input)Note 3
1	1	1	×	0	0	1	×	Slave transmission/ receptionNote 3	SI10	SO10	$\overline{\text{SCK10}}$ (input)Note 3
1	0	1	×	×Note 1	×Note 1	0	1	Master reception	SI10	TxD0/P13	$\overline{\text{SCK10}}$ (output)
1	1	×Note 1	×Note 1	0	0	0	1	Master transmission	RxD0/P12	SO10	$\overline{\text{SCK10}}$ (output)
1	1	1	×	0	0	0	1	Master transmission/ reception	SI10	SO10	$\overline{\text{SCK10}}$ (output)

Notes 1. Can be set as port function.
2. To use P11/$\overline{\text{SCK10}}$ as port pins, clear CKP10 to 0.
3. To use the slave mode, set CKS102, CKS101, and CKS100 to 1, 1, 1.

Remark ×: don't care
CSIE10: Bit 7 of serial operation mode register 10 (CSIM10)
TRMD10: Bit 6 of CSIM10
CKP10: Bit 4 of serial clock selection register 10 (CSIC10)
CKS102, CKS101, CKS100: Bits 2 to 0 of CSIC10
PM1×: Port mode register
P1×: Port output latch

(2) 1-byte transmission/reception communication operation

(a) 1-byte transmission/reception

When bit 7 (CSIAE0) and bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) = 1, 0, respectively, if communication data is written to serial I/O shift register 0 (SIOA0), the data is output via the SOA0 pin in synchronization with the $\overline{\text{SCKA0}}$ falling edge, and stored in the SIOA0 register in synchronization with the rising edge 1 clock later.

Data transmission and data reception can be performed simultaneously.

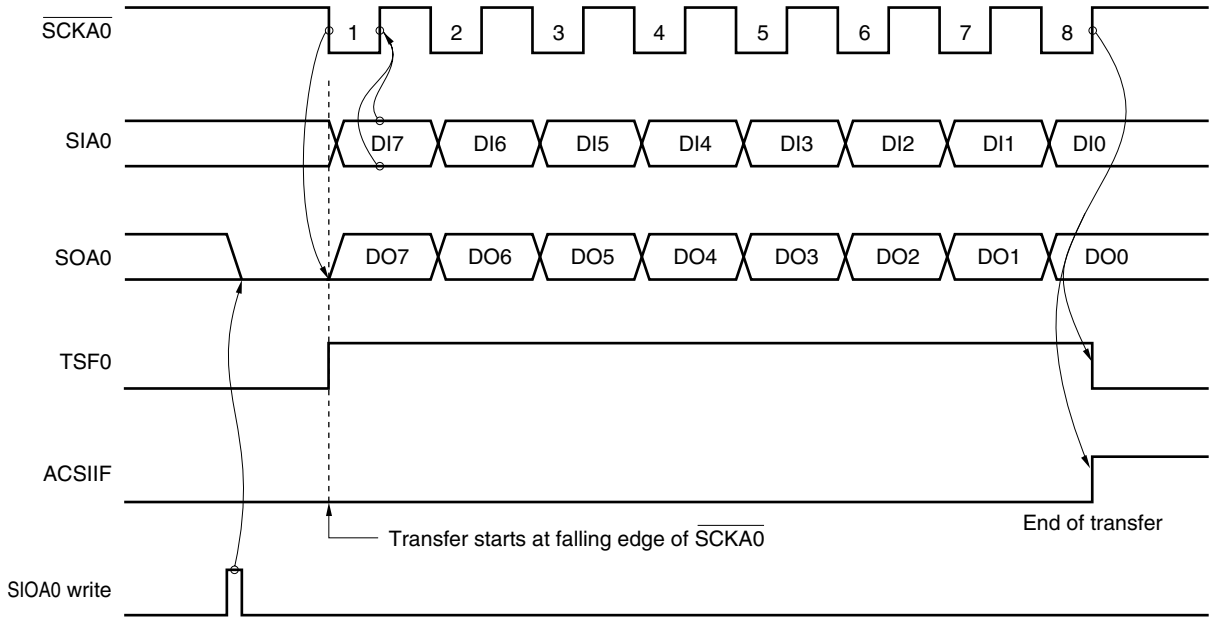
If only reception is to be performed, communication can only be started by writing a dummy value to the SIOA0 register.

When communication of 1 byte is complete, an interrupt request signal (INTACSI) is generated.

In 1-byte transmission/reception, the setting of bit 5 (ATM0) of CSIMA0 is invalid.

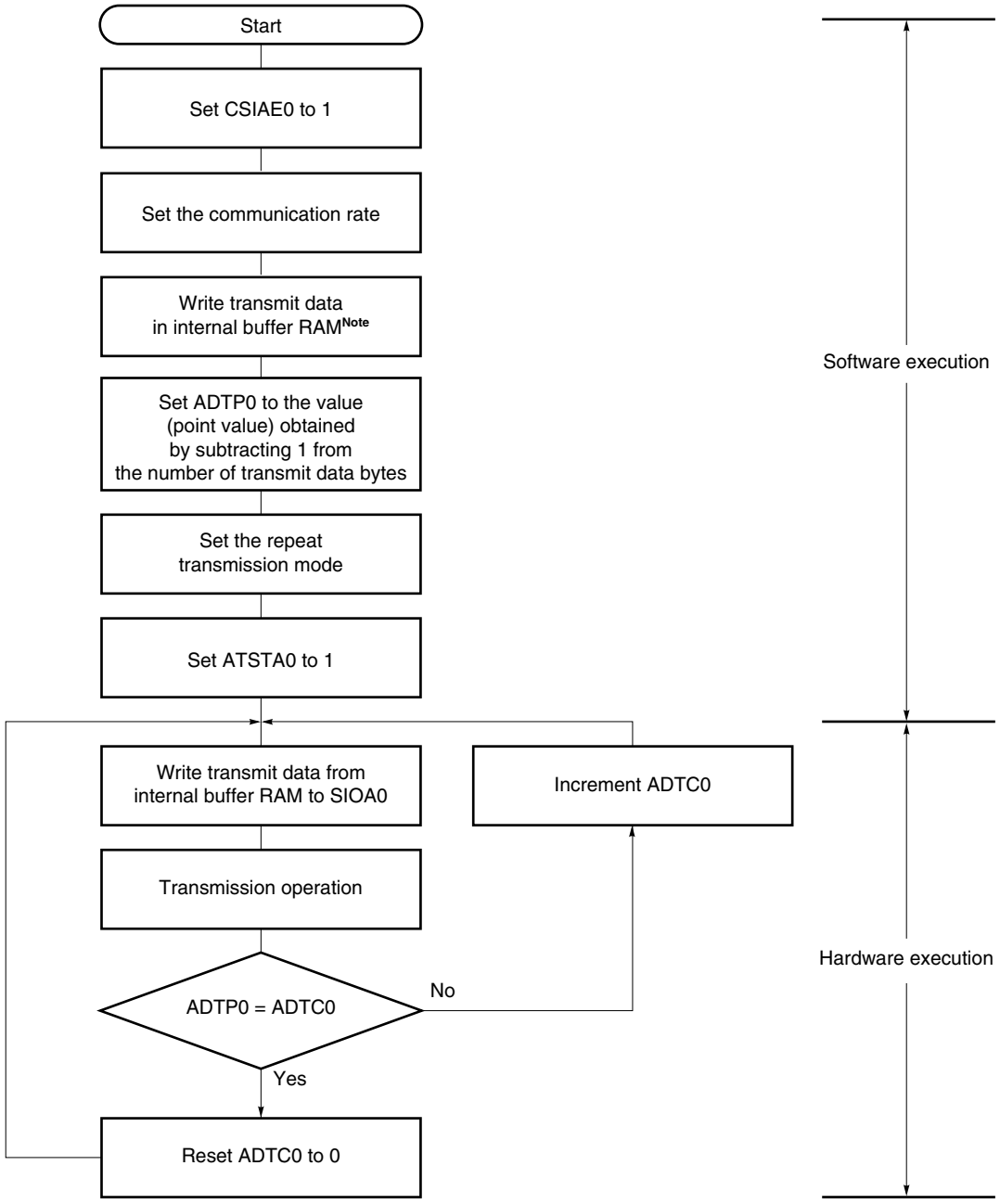
Be sure to read data after confirming that bit 0 (TSF0) of serial status register 0 (CSIS0) = 0.

Figure 17-11. 3-Wire Serial I/O Mode Timing



Caution The SOA0 pin becomes low level by an SIOA0 write.

Figure 17-21. Repeat Transmission Mode Flowchart



CSIAE0: Bit 7 of serial operation mode specification register 0 (CSIMA0)
ADTP0: Automatic data transfer address point specification register 0
ADTI0: Automatic data transfer interval specification register 0
ATSTA0: Bit 0 of serial trigger register 0 (CSIT0)
SIOA0: Serial I/O shift register 0
ADTC0: Automatic data transfer address count register 0

Note A wait state may be generated when data is written to the buffer RAM. For details, see **CHAPTER 34 CAUTIONS FOR WAIT**.

(3) LCD clock control register (LCDC0)

LCDC0 specifies the LCD source clock and LCD clock.

The frame frequency is determined according to the LCD clock and the number of time slices.

LCDC0 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets LCDC0 to 00H.

Figure 18-4. Format of LCD Clock Control Register

Address: FFB2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDC0	0	LCDC6	LCDC5	LCDC4	0	LCDC2	LCDC1	LCDC0

LCDC6	LCDC5	LCDC4	LCD source clock (f_{LCD}) selection
0	0	0	f_{XT} (32.768 kHz)
0	0	1	$f_{PRS}/2^6$
0	1	0	$f_{PRS}/2^7$
0	1	1	$f_{PRS}/2^8$
1	0	0	$f_{RL}/2^3$
Other than above			Setting prohibited

LCDC2	LCDC1	LCDC0	LCD clock (LCDCL) selection
0	0	0	$f_{LCD}/2^4$
0	0	1	$f_{LCD}/2^5$
0	1	0	$f_{LCD}/2^6$
0	1	1	$f_{LCD}/2^7$
1	0	0	$f_{LCD}/2^8$
1	0	1	$f_{LCD}/2^9$
Other than above			Setting prohibited

Caution Bits 3 and 7 must be set to 0.

Remarks 1. f_{XT}: XT1 clock oscillation frequency

2. f_{PRS}: Peripheral hardware clock frequency

3. f_{RL}: Internal low-speed oscillation clock frequency