Renesas Electronics America Inc - UPD78F0482GK-GAK-AX Datasheet

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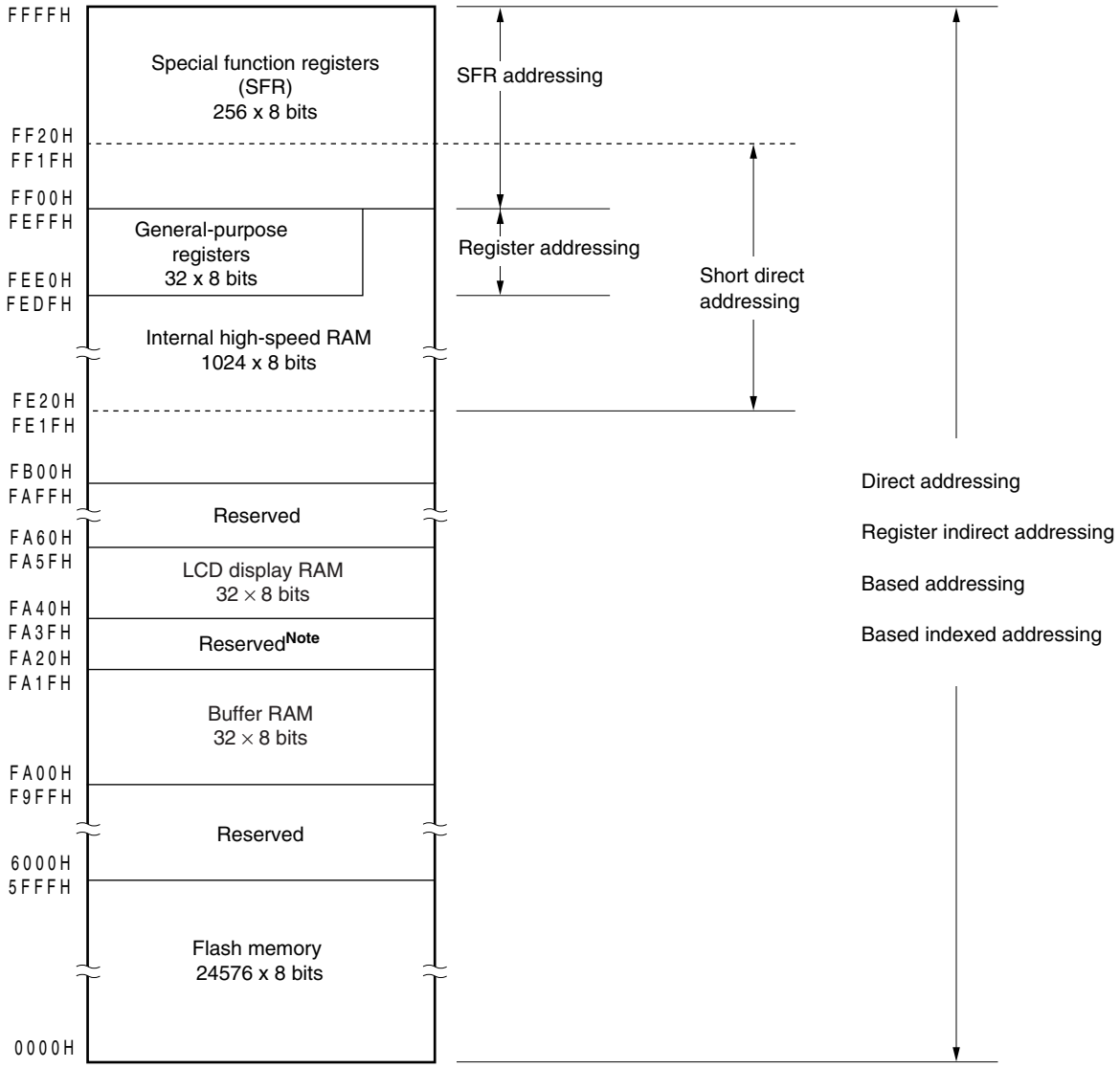
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0482gk-gak-ax

Figure 3-14. Correspondence Between Data Memory and Addressing (μPD78F0492)



<R> **Note** However, FA26H and FA27H can be used (See **13.3 Registers Used in 16-Bit ΔΣ Type A/D Converter**).

4.2 Port Configuration

Ports include the following hardware.

Table 4-3. Port Configuration

Item	Configuration
Control registers	Port mode register (PM1 to PM4, PM8 to PM15) Port register (P1 to P4, P8 to P15) Pull-up resistor option register (PU1, PU3, PU4, PU8 to PU15) Port function register 1 (PF1) Port function register 2 (PF2)[Note 1] Port function register ALL (PFALL) A/D port configuration register 0 (ADPC0)[Note 2]
Port	Total: 62
Pull-up resistor	Total: 50

Notes 1. μPD78F047x and 78F048x only

2. μPD78F048x and 78F049x only

CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00

6.1 Functions of 16-Bit Timer/Event Counter 00

16-bit timer/event counter 00 has the following functions.

(1) Interval timer

16-bit timer/event counter 00 generates an interrupt request at the preset time interval.

(2) Square-wave output

16-bit timer/event counter 00 can output a square wave with any selected frequency.

(3) External event counter

16-bit timer/event counter 00 can measure the number of pulses of an externally input signal.

(4) One-shot pulse output

16-bit timer event counter 00 can output a one-shot pulse whose output pulse width can be set freely.

(5) PPG output

16-bit timer/event counter 00 can output a rectangular wave whose frequency and output pulse width can be set freely.

(6) Pulse width measurement

16-bit timer/event counter 00 can measure the pulse width of an externally input signal.

(7) External 24-bit event counter

16-bit timer/event counter 00 can be operated to function as an external 24-bit event counter, by connecting 16-bit timer 00 and 8-bit timer/event counter 52 in cascade, and using the external event counter function of 8-bit timer/event counter 52.

When using it as an external 24-bit event counter, external event input gate enable can be controlled via 8-bit timer counter H2 output.

Figure 6-52. Example of Register Settings for Pulse Width Measurement (2/2)

(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

This register is used as a capture register. Either the TI000 or TI010 pin is selected as a capture trigger. When a specified edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

(g) 16-bit capture/compare register 010 (CR010)

This register is used as a capture register. The signal input to the TI000 pin is used as a capture trigger. When the capture trigger is detected, the count value of TM00 is stored in CR010.

(3) Input switch control register (ISC)

By setting ISC2 to 1, the TI52 input signal can be controlled via the TOH2 output signal.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 7-12. Format of Input Switch Control Register (ISC)

Address: FF4FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	ISC5	ISC4	ISC3	ISC2	ISC1	ISC0

ISC5	ISC4	TxD6, RxD6 input source selection
0	0	TxD6:P112, RxD6: P113
0	1	TxD6:P16, RxD6: P15
Other than above		Setting prohibited

ISC3	RxD6/P113 input enabled/disabled
0	RxD6/P113 input disabled
1	RxD6/P113 input enabled

ISC2	TI52 input source control
0	No enable control of TI52 input (P34)
1	Enable controlled of TI52 input (P34) Note 1

ISC1	TI000 input source selection
0	TI000 (P33)
1	RxD6 (P15 or P113 Note 2)

ISC0	INTP0 input source selection
0	INTP0 (P120)
1	RxD6 (P15 or P113 Note 2)

Notes 1. TI52 input is controlled by TOH2 output signal.

<R> **2.** This is selected by ISC5 and ISC4.

12.3 Registers Used in 10-Bit Successive Approximation Type A/D Converter

The A/D converter uses the following seven registers.

- A/D converter mode register (ADM)
- A/D port configuration register 0 (ADPC0)
- Analog input channel specification register (ADS)
- Port function register 2 (PF2) (μPD78F048x only)
- Port mode register 2 (PM2)
- 10-bit A/D conversion result register (ADCR)
- 8-bit A/D conversion result register (ADCRH)

(1) A/D converter mode register (ADM)

This register sets the conversion time for analog input to be A/D converted, and starts/stops conversion.

ADM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12-3. Format of A/D Converter Mode Register (ADM)

Address: FF8DH After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM	ADCS	FR3[Note 1]	FR2[Note 1]	FR1[Note 1]	FR0[Note 1]	LV1[Note 1]	LV0[Note 1]	ADCE

ADCS	A/D conversion operation control
0	Stops conversion operation
1	Enables conversion operation

ADCE	Comparator operation control[Note 2]
0	Stops comparator operation
1	Enables comparator operation

Notes 1. For details of FR3 to FR0, LV1, LV0, and A/D conversion, see **Table 12-2 A/D Conversion Time Selection**.

2. The operation of the comparator is controlled by ADCS and ADCE, and it takes 1 μs from operation start to operation stabilization. Therefore, when ADCS is set to 1 after 1 μs or more has elapsed from the time ADCE is set to 1, the conversion result at that time has priority over the first conversion result. Otherwise, ignore data of the first conversion.

Table 12-1. Settings of ADCS and ADCE

ADCS	ADCE	A/D Conversion Operation
0	0	Stop status (DC power consumption path does not exist)
0	1	Conversion waiting mode (comparator operation, only comparator consumes power)
1	0	Conversion mode (comparator operation stopped[Note])
1	1	Conversion mode (comparator operation)

Note Ignore data of the first conversion.

Figure 12-9. Format of A/D Port Configuration Register 0 (ADPC0)

Address: FF8FH After reset: 08H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPC03	ADPC02	ADPC01	ADPC00

<μPD78F048x>

<R>

ADPC03	ADPC02	ADPC01	ADPC00	Digital I/O (D)/analog input (A) switching							
				P27/ ANI7/ SEG32	P26/ ANI6/ SEG33	P25/ ANI5/ SEG34	P24/ ANI4/ SEG35	P23/ ANI3/ SEG36	P22/ ANI2/ SEG37	P21/ ANI1/ SEG38	P20/ ANI0/ SEG39
0	0	0	0	A	A	A	A	A	A	A	A
0	0	0	1	A	A	A	A	A	A	A	D
0	0	1	0	A	A	A	A	A	A	D	D
0	0	1	1	A	A	A	A	A	D	D	D
0	1	0	0	A	A	A	A	D	D	D	D
0	1	0	1	A	A	A	D	D	D	D	D
0	1	1	0	A	A	D	D	D	D	D	D
0	1	1	1	A	D	D	D	D	D	D	D
1	0	0	0	D	D	D	D	D	D	D	D
Other than above				Setting prohibited							

<μPD78F049x>

ADPC03	ADPC02	ADPC01	ADPC00	Digital I/O (D)/analog input (A: successive approximation type, Δ: ΔΣ type) switching							
				P27/ ANI7/ REF+	P26/ ANI6/ REF-	P25/ ANI5/ DS2+	P24/ ANI4/ DS2-	P23/ ANI3/ DS1+	P22/ ANI2/ DS1-	P21/ ANI1/ DS0+	P20/ ANI0/ DS0-
0	0	0	0	A/Δ	A/Δ	A/Δ	A/Δ	A/Δ	A/Δ	A/Δ	A/Δ
0	0	0	1	A/Δ	A/Δ	A/Δ	A/Δ	A/Δ	A/Δ	A	D
0	0	1	0	A/Δ	A/Δ	A/Δ	A/Δ	A/Δ	A/Δ	D	D
0	0	1	1	A/Δ	A/Δ	A/Δ	A/Δ	A	D	D	D
0	1	0	0	A/Δ	A/Δ	A/Δ	A/Δ	D	D	D	D
0	1	0	1	A	A	A	D	D	D	D	D
0	1	1	0	A	A	D	D	D	D	D	D
0	1	1	1	A	D	D	D	D	D	D	D
1	0	0	0	D	D	D	D	D	D	D	D
Other than above				Setting prohibited							

Cautions 1. Set the channel used for A/D conversion to the input mode by using port mode register 2 (PM2).

2. Do not set the pin set by ADPC0 as digital I/O by ADS, ADDS1, or ADDS0.

3. If data is written to ADPC0, a wait cycle is generated. Do not write data to ADPC0 when the CPU is operating on the subsystem clock and the peripheral hardware clock is stopped. For details, see CHAPTER 34 CAUTIONS FOR WAIT.

4. If pins ANI0/P20/SEG39 to ANI7/P27/SEG32 are set to segment output pins via the PF2 register, output is set to segment output, regardless of the ADPC0 setting (for μPD78F048x only).

(1) Receive buffer register 0 (RXB0)

This 8-bit register stores parallel data converted by receive shift register 0 (RXS0).

Each time 1 byte of data has been received, new receive data is transferred to this register from receive shift register 0 (RXS0).

If the data length is set to 7 bits the receive data is transferred to bits 0 to 6 of RXB0 and the MSB of RXB0 is always 0.

If an overrun error (OVE0) occurs, the receive data is not transferred to RXB0.

RXB0 can be read by an 8-bit memory manipulation instruction. No data can be written to this register.

Reset signal generation and POWER0 = 0 set this register to FFH.

(2) Receive shift register 0 (RXS0)

This register converts the serial data input to the RxD0 pin into parallel data.

RXS0 cannot be directly manipulated by a program.

(3) Transmit shift register 0 (TXS0)

This register is used to set transmit data. Transmission is started when data is written to TXS0, and serial data is transmitted from the TxD0 pins.

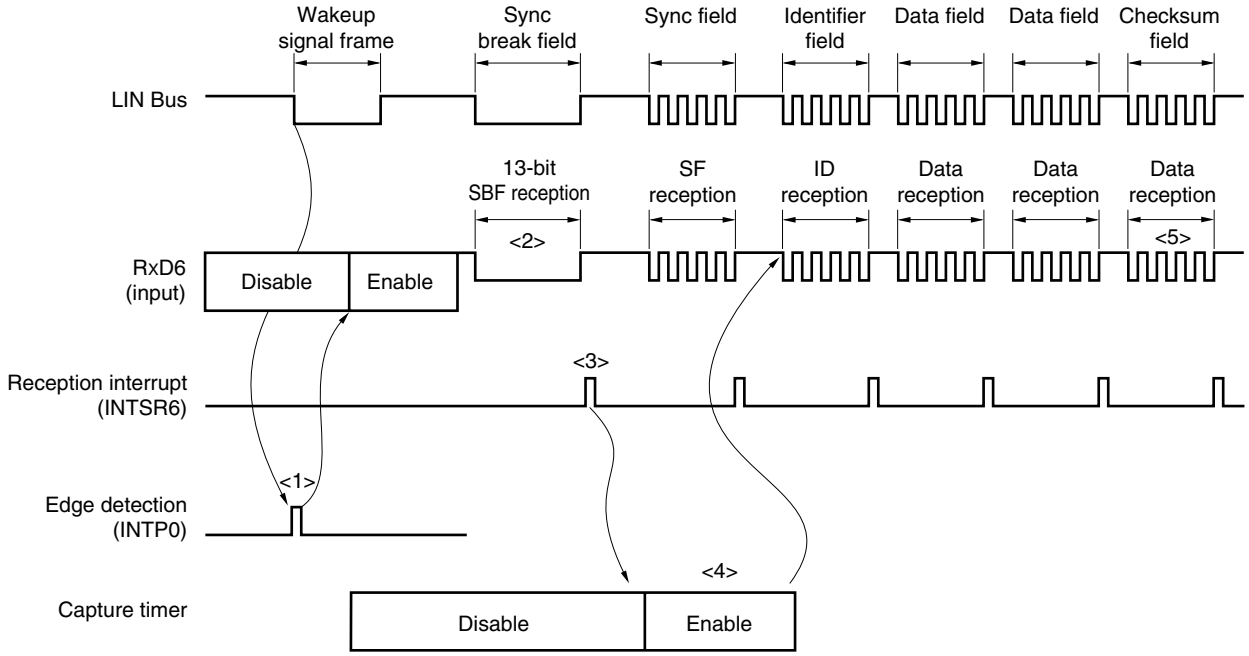
TXS0 can be written by an 8-bit memory manipulation instruction. This register cannot be read.

Reset signal generation, POWER0 = 0, and TXE0 = 0 set this register to FFH.

Cautions 1. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

2. Do not write the next transmit data to TXS0 before the transmission completion interrupt signal (INTST0) is generated.

Figure 15-2. LIN Reception Operation



Reception processing is as follows.

<1> The wakeup signal is detected at the edge of the pin, and enables UART6 and sets the SBF reception mode.

<2> Reception continues until the STOP bit is detected. When an SBF with low-level data of 11 bits or more has been detected, it is assumed that SBF reception has been completed correctly, and an interrupt signal is output. If an SBF with low-level data of less than 11 bits has been detected, it is assumed that an SBF reception error has occurred. The interrupt signal is not output and the SBF reception mode is restored.

<3> If SBF reception has been completed correctly, an interrupt signal is output. Start 16-bit timer/event counter 00 by the SBF reception end interrupt servicing and measure the bit interval (pulse width) of the sync field (see **6.4.8 Pulse width measurement operation**). Detection of errors OVE6, PE6, and FE6 is suppressed, and error detection processing of UART communication and data transfer of the shift register and RXB6 is not performed. The shift register holds the reset value FFH.

<4> Calculate the baud rate error from the bit interval of the sync field, disable UART6 after SF reception, and then re-set baud rate generator control register 6 (BRGC6).

<5> Distinguish the checksum field by software. Also perform processing by software to initialize UART6 after reception of the checksum field and to set the SBF reception mode again.

Figure 15-3 shows the port configuration for LIN reception operation.

The wakeup signal transmitted from the LIN master is received by detecting the edge of the external interrupt (INTP0). The length of the sync field transmitted from the LIN master can be measured using the external event capture operation of 16-bit timer/event counter 00, and the baud rate error can be calculated.

The input source of the reception port input (RxD6) can be input to the external interrupt (INTP0) and 16-bit timer/event counter 00 by port input switch control (ISC0/ISC1), without connecting RxD6 and INTP0/TI000 externally.

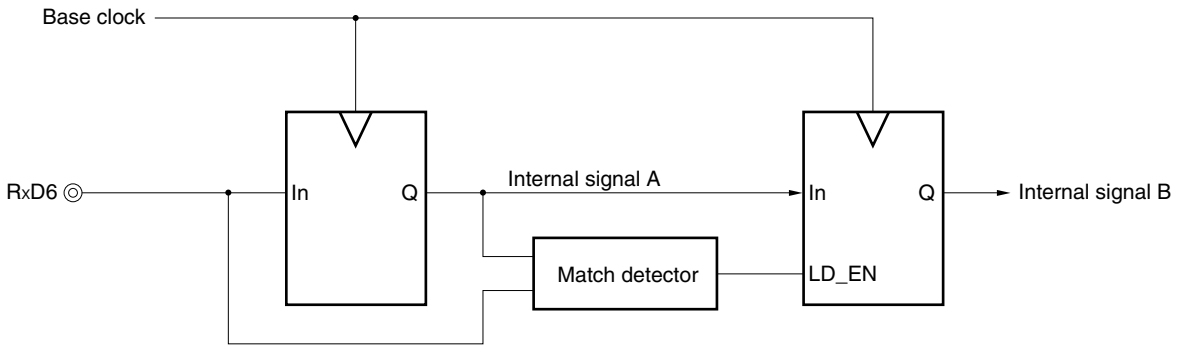
(g) Noise filter of receive data

The RxD6 signal is sampled with the base clock output by the prescaler block.

If two sampled values are the same, the output of the match detector changes, and the data is sampled as input data.

Because the circuit is configured as shown in Figure 15-23, the internal processing of the reception operation is delayed by two clocks from the external signal status.

Figure 15-23. Noise Filter Circuit



(h) SBF transmission

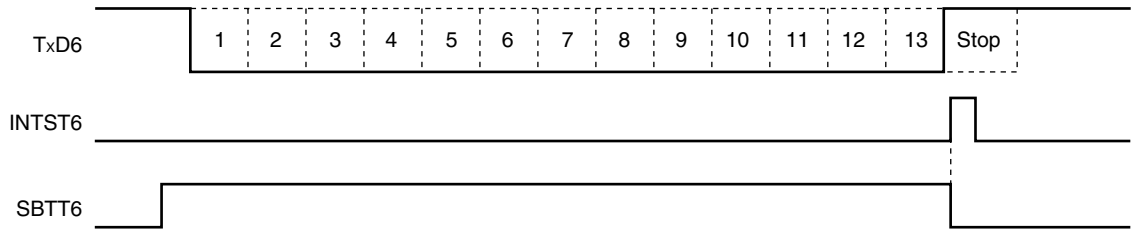
When the device is use in LIN communication operation, the SBF (Synchronous Break Field) transmission control function is used for transmission. For the transmission operation of LIN, see **Figure 15-1 LIN Transmission Operation**.

When bit 7 (POWER6) of asynchronous serial interface mode register 6 (ASIM6) is set to 1, the TxD6 pin outputs high level. Next, when bit 6 (TXE6) of ASIM6 is set to 1, the transmission enabled status is entered, and SBF transmission is started by setting bit 5 (SBTT6) of asynchronous serial interface control register 6 (ASICL6) to 1.

Thereafter, a low level of bits 13 to 20 (set by bits 4 to 2 (SBL62 to SBL60) of ASICL6) is output. Following the end of SBF transmission, the transmission completion interrupt request (INTST6) is generated and SBTT6 is automatically cleared. Thereafter, the normal transmission mode is restored.

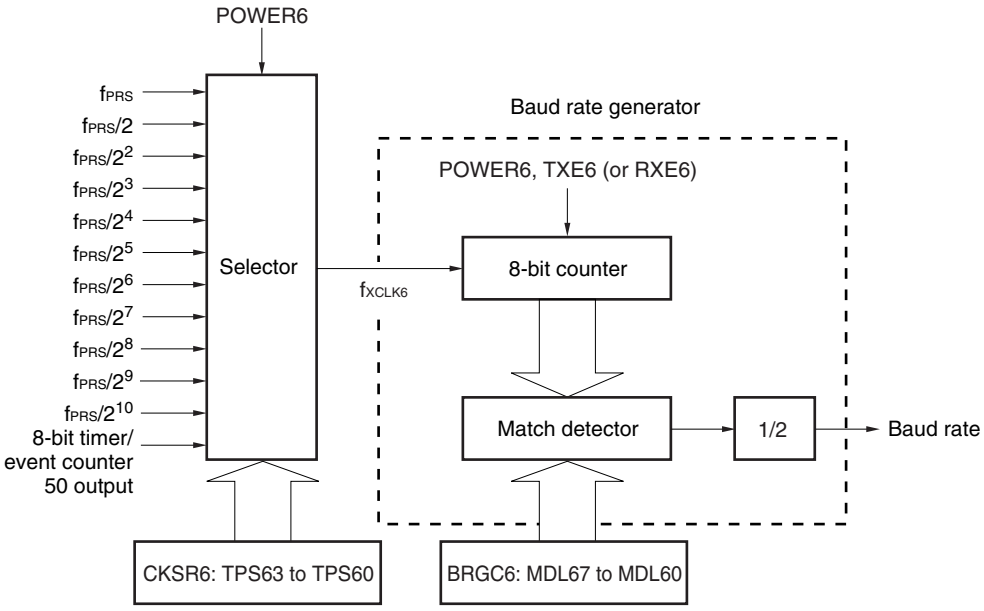
Transmission is suspended until the data to be transmitted next is written to transmit buffer register 6 (TXB6), or until SBTT6 is set to 1.

Figure 15-24. SBF Transmission



Remark TxD6: TxD6 pin (output)
INTST6: Transmission completion interrupt request
SBTT6: Bit 5 of asynchronous serial interface control register 6 (ASICL6)

Figure 15-26. Configuration of Baud Rate Generator



Remark POWER6: Bit 7 of asynchronous serial interface operation mode register 6 (ASIM6)
TXE6: Bit 6 of ASIM6
RXE6: Bit 5 of ASIM6
CKSR6: Clock selection register 6
BRGC6: Baud rate generator control register 6

(2) Generation of serial clock

A serial clock to be generated can be specified by using clock selection register 6 (CKSR6) and baud rate generator control register 6 (BRGC6).

The clock to be input to the 8-bit counter can be set by bits 3 to 0 (TPS63 to TPS60) of CKSR6 and the division value ($f_{XCLK6}/4$ to $f_{XCLK6}/255$) of the 8-bit counter can be set by bits 7 to 0 (MDL67 to MDL60) of BRGC6.

Remarks 1. Use the following procedure to set to the display-off state and disconnect the internal resistors when using the internal resistance division method.

<1> Clear LCDON (bit 7 of LCDM) (LCDON = 0).
Deselect signals are output from all segment pins and common pins, and a non-display state is entered.

<2> Clear SCOC (bit 6 of the LCD display mode register (LCDM)) (SCOC = 0).
Ground levels are output from all segment pins and common pins.

<3> Assume MDSET0, MDSET1 (bits 4 and 5 of the LCD mode register (LCDMD)) = (0, 0) and set the resistance division method to the external resistance division method.

2. m = 0 to 7, n = 08 to 11, 13 to 15

Caution When displaying in a mode with a large number of COMs, such as 8 COM, V_{LC0} may not be able to obtain sufficient contrast under the low-voltage conditions, depending on the panel characteristics. Use the LCD controller/driver after having performed thorough LCD display evaluation and confirmed that there are no problems regarding the display quality.

18.7.2 Two-time-slice display example

Figure 18-21 shows how the 6-digit LCD panel having the display pattern shown in Figure 18-20 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 and COM1) of the 78K0/LF3 chip. This example displays data "12345.6" in the LCD panel. The contents of the display data memory (FA40H to FA57H) correspond to this display.

The following description focuses on numeral "3" (∃) displayed in the fourth digit. To display "3" in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 to SEG15 pins according to Table 18-7 at the timing of the common signals COM0 and COM1; see Figure 18-20 for the relationship between the segment signals and LCD segments.

Table 18-7. Select and Deselect Voltages (COM0 and COM1)

Segment / Common	SEG12	SEG13	SEG14	SEG15
COM0	Select	Select	Deselect	Deselect
COM1	Deselect	Select	Select	Select

According to Table 18-7, it is determined that the display data memory location (FA4FH) that corresponds to SEG15 must contain xx10.

Figure 18-22 shows examples of LCD drive waveforms between the SEG15 signal and each common signal. When the select voltage is applied to SEG15 at the timing of COM1, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 18-20. Two-Time-Slice LCD Display Pattern and Electrode Connections

Remark n = 0 to 5

(b) MCG control register 1 (MC0CTL1)

This register is used to set the base clock of the Manchester code generator.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Address: FF4DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MC0CTL1	0	0	0	0	0	MC0CKS2	MC0CKS1	MC0CKS0

MC0CKS2	MC0CKS1	MC0CKS0	Base clock (f_{XCLK}) selection[Note 1]
0	0	0	f_{PRS}[Note 2] (10 MHz)
0	0	1	$f_{PRS}/2$ (5 MHz)
0	1	0	$f_{PRS}/2^2$ (2.5 MHz)
0	1	1	$f_{PRS}/2^3$ (1.25 MHz)
1	0	0	$f_{PRS}/2^4$ (625 kHz)
1	0	1	$f_{PRS}/2^5$ (312.5 kHz)
1	1	0	
1	1	1	

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of MC0CKS2 = MC0CKS1 = MC0CKS0 = 0 (base clock: f_{PRS}) is prohibited.

Caution Clear bit 7 (MC0PWR) of the MC0CTL0 register to 0 before rewriting the MC0CKS2 to MC0CKS0 bits.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. Figures in parentheses are for operation with f_{PRS} = 10 MHz.

(c) MCG control register 2 (MC0CTL2)

This register is used to set the transmit baud rate.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 1FH.

Address: FF4EH After reset: 1FH R/W

Symbol	7	6	5	4	3	2	1	0
MC0CTL2	0	0	0	MC0BRS4	MC0BRS3	MC0BRS2	MC0BRS1	MC0BRS0

MC0BRS4	MC0BRS3	MC0BRS2	MC0BRS1	MC0BRS0	k	Output clock selection of 5-bit counter
0	0	0	×	×	4	$f_{XCLK}/4$
0	0	1	0	0	4	$f_{XCLK}/4$
0	0	1	0	1	5	$f_{XCLK}/5$
0	0	1	1	0	6	$f_{XCLK}/6$
0	0	1	1	1	7	$f_{XCLK}/7$
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	1	1	0	0	28	$f_{XCLK}/28$
1	1	1	0	1	29	$f_{XCLK}/29$
1	1	1	1	0	30	$f_{XCLK}/30$
1	1	1	1	1	31	$f_{XCLK}/31$

Cautions 1. Clear bit 7 (MC0PWR) of the MC0CTL0 register to 0 before rewriting the MC0BRS4 to MC0BRS0 bits.

2. The value from further dividing the output clock of the 5-bit counter by 2 is the baud rate value.

Remarks 1. f_{XCLK}: Frequency of the base clock selected by the MC0CKS2 to MC0CKS0 bits of the MC0CTL1 register

2. k: Value set by the MC0BRS4 to MC0BRS0 bits (k = 4, 5, 6, 7, …., 31)

3. ×: Don't care

<1> Baud rate

The baud rate can be calculated by the following expression.

- Baud rate = $\frac{f_{XCLK}}{2 \times k}$ [bps]

f_{XCLK}: Frequency of base clock selected by the MC0CKS2 to MC0CKS0 bits of the MC0CTL1 register

k: Value set by the MC0BRS4 to MC0BRS0 bits of the MC0CTL2 register (k = 4, 5, 6, ..., 31)

21.4 Interrupt Servicing Operations

21.4.1 Maskable interrupt acknowledgment

A maskable interrupt becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request (when the ISP flag is reset to 0).

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 21-4 below.

For the interrupt request acknowledgment timing, see **Figures 21-8** and **21-9**.

Table 21-4. Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
When ××PR = 0	7 clocks	32 clocks
When ××PR = 1	8 clocks	33 clocks

Note If an interrupt request is generated just before a divide instruction, the wait time becomes longer.

Remark 1 clock: $1/f_{CPU}$ (f_{CPU}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 21-7 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP flag. The vector table data determined for each interrupt request is the loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

Table 28-14. Interrupt Response Time (Library for Normal Model) (1/2)

Function Name	Interrupt Response Time (Unit: μs)					
	When entry RAM is allocated outside short direct addressing range			When entry RAM is allocated within short direct addressing range		
	RSTOP = 0 and RSTS = 1 (during stable operation of internal high-speed oscillator)		RSTOP = 1 (internal high-speed oscillator stopped)Note	RSTOP = 0 and RSTS = 1 (during stable operation of internal high-speed oscillator)		RSTOP = 1 (internal high-speed oscillator stopped)Note
	MCS = 0 (CPU operates with internal high-speed oscillation clock)	MCS = 1 (CPU operates with high-speed system clock)	MCS = 1 (CPU operates with high-speed system clock)	MCS = 0 (CPU operates with internal high-speed oscillation clock)	MCS = 1 (CPU operates with high-speed system clock)	MCS = 1 (CPU operates with high-speed system clock)
Block erase function	179/fCPU+1269	179/fCPU+1269	179/fCPU+1912	179/fCPU+703	179/fCPU+703	179/fCPU+713
Word write function	333/fCPU+1098	333/fCPU+1098	333/fCPU+1742	333/fCPU+533	333/fCPU+533	333/fCPU+543
Block verify function	179/fCPU+1013	179/fCPU+1013	179/fCPU+1656	179/fCPU+448	179/fCPU+448	179/fCPU+456
Block blank check function	179/fCPU+993	179/fCPU+993	179/fCPU+1637	179/fCPU+428	179/fCPU+428	179/fCPU+438
Set information function	80/fCPU+833	80/fCPU+833	80/fCPU+1477	80/fCPU+346	80/fCPU+346	80/fCPU+346
EEPROM write function	333/fCPU+1107	333/fCPU+1107	333/fCPU+1751	333/fCPU+542	333/fCPU+542	333/fCPU+552

Note This is the function processing time when the function is executed immediately after the self programming start function has been executed. The processing time after a function other than the self programming start function has been executed is the same as that of RSTOP = 0.

Remark RSTOP: Bit 0 of the internal oscillation mode register (RCM)
RSTS: Bit 7 of RCM
MCS: Bit 1 of main clock mode register (MCM)
f_{CPU}: CPU clock frequency
W: Number of words to be written (1 word = 4 bytes)

28.10.1 Boot swap function

If rewriting the boot area has failed during self-programming due to a power failure or some other cause, the data in the boot area may be lost and the program may not be restarted by resetting.

The boot swap function is used to avoid this problem.

Before erasing boot cluster 0[Note], which is a boot program area, by self-programming, write a new boot program to boot cluster 1 in advance. When the program has been correctly written to boot cluster 1, swap this boot cluster 1 and boot cluster 0 by using the set information function of the firmware of the 78K0/LF3, so that boot cluster 1 is used as a boot area. After that, erase or write the original boot program area, boot cluster 0.

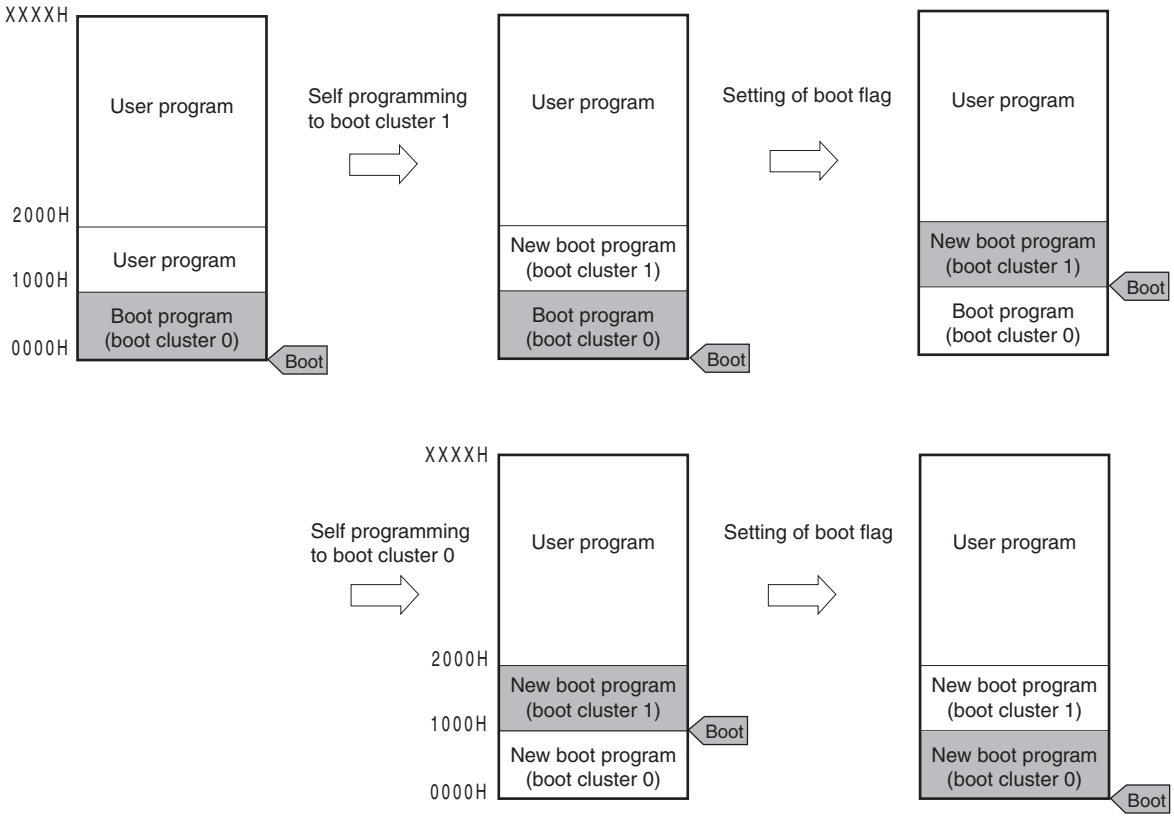
As a result, even if a power failure occurs while the boot programming area is being rewritten, the program is executed correctly because it is booted from boot cluster 1 to be swapped when the program is reset and started next.

If the program has been correctly written to boot cluster 0, restore the original boot area by using the set information function of the firmware of the 78K0/LF3.

Note A boot cluster is a 4 KB area and boot clusters 0 and 1 are swapped by the boot swap function.

Boot cluster 0 (0000H to 0FFFH): Original boot program area
Boot cluster 1 (1000H to 1FFFH): Area subject to boot swap function

Figure 28-17. Boot Swap Function



Remark Boot cluster 1 becomes 0000H to 0FFFH when a reset is generated after the boot flag has been set.

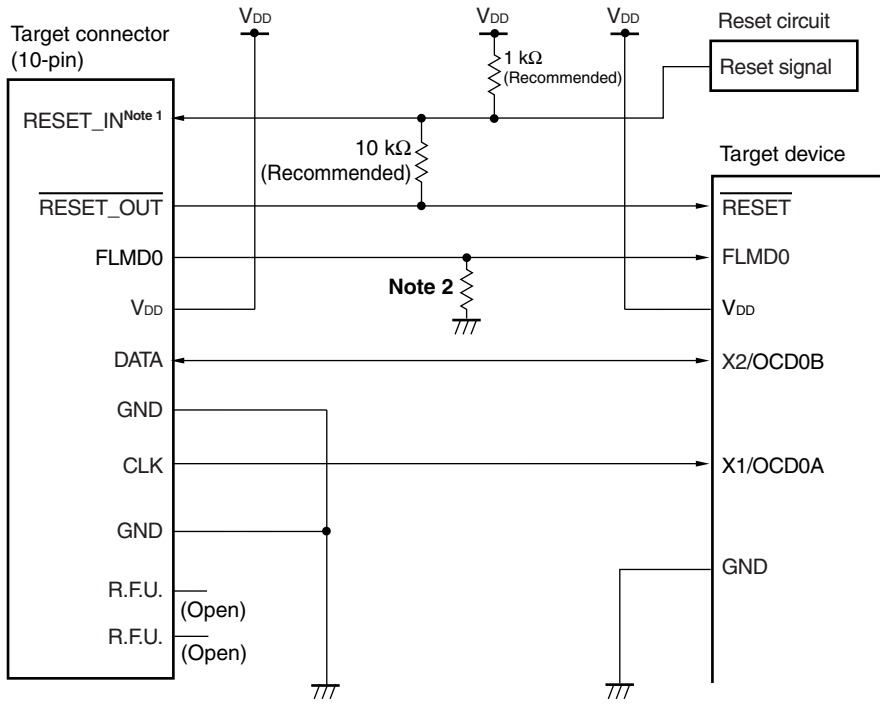
<R>

29.1 Connecting QB-MINI2 to 78K0/LF3

The 78K0/LF3 uses the V_{DD}, FLMD0, $\overline{\text{RESET}}$, OCD0A/X1, OCD0B/X2, and V_{SS} pins to communicate with the host machine via an on-chip debug emulator (QB-MINI2).

Caution The 78K0/LF3 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. NEC Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 29-1. Connection Example of QB-MINI2 and 78K0/LF3



Notes 1. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less). For details, refer to **QB-MINI2 User's Manual (U18371E)**.

2. Make pull-down resistor 470 Ω or more (10 kΩ: recommended).

Caution Input the clock from the OCD0A/X1 pin during on-chip debugging.

30.3 Instructions Listed by Addressing Type

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

First Operand \ Second Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except “r = A”