Renesas Electronics America Inc - UPD78F0483GC-GAD-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0483gc-gad-ax

Table 4-5. Settings of PFALL, PF2, PF1, ISC, Port Mode Register, and Output Latch When Using Alternate Function (1/2)

Pin Name	Alternate Function		PFALL, PF2[Note 4]	PF1	ISC	PM××	P××
	Function Name	I/O					
P10	PCL	Output	–			0	0
P11	$\overline{SCK10}$	Input	–			1	×
		Output	–			0	1
P12	SI10	Input	–			1	×
	RxD0	Input	–			1	×
P13[Note 10]	SO10	Output	–	PF13 = 0		0	0
	TxD0	Output	–	PF13 = 1		0	×
P14	$\overline{SCKA0}$	Input	–			1	×
		Output	–			0	1
	INTP4	Input	–			1	×
P15	SIA0	Input	–			1	×
	<RxD6>	Input	–		ISC4 = 1[Note 5, 7], ISC5 = 0	1	×
P16[Note 11]	SOA0	Output	–	PF16 = 0		0	0
	<TxD6>	Output	–	PF16 = 1	ISC4 = 1, ISC5 = 0	0	×
P20 to P27[Note 2]	SEG39 to SEG32[Note 12]	Output	1			×	×
	ANI0 to ANI7[Note 1]	Input	0			1	×
	DS0± to DS2±[Note 8]	Input	0			1	×
	REF±[Note 8]	Input	0			1	×
P30	INTP5	Input	–			1	×
P31	TOH1	Output	–			0	0
	INTP3	Input	–			1	×
P32	TOH0	Output	–			0	0
	MCGO	Output	–			0	0
P33	TI000	Input	–		ISC1 = 0	1	×
	RTCDIV	Output	–			0	0
	RTCCL	Output	–			0	0
	BUZ	Output	–			0	0
	INTP2	Input	–			1	×
P34	TI52	Input	–		**Note 6**	1	×
	TI010	Input	–			1	×
	TO00	Output	–			0	0
	RTC1HZ	Output	–			0	0
	INTP1	Input	–			1	×

(Note and Remark are listed on the page after next.)

Figure 5-2. Format of Clock Operation Mode Select Register (OSCCTL)

Address: FF9FH After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	3	2	1	0
OSCCTL	EXCLK	OSCSEL	0	OSCSELS	0	0	0	0

EXCLK	OSCSEL	High-speed system clock pin operation mode	P121/X1 pin	P122/X2/EXCLK pin
0	0	Input port mode	Input port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Caution To change the value of EXCLK and OSCSEL, be sure to confirm that bit 7 (MSTOP) of the main OSC control register (MOC) is 1 (the X1 oscillator stops or the external clock from the EXCLK pin is disabled).
Be sure to clear bits 0 to 3, and 5 to "0".

Remark f_{XH}: High-speed system clock oscillation frequency

(9) Internal high-speed oscillation trimming register (HIOTRM)

This register corrects the accuracy of the internal high-speed oscillator. The accuracy can be corrected by self-measuring the frequency of the internal high-speed oscillator, using a subsystem clock using a crystal resonator or using a timer with high-accuracy external clock input, such as a real-time counter.

HIOTRM can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets HIOTRM to 10H.

Caution If the temperature or V_{DD} pin voltage is changed after accuracy correction, the frequency will fluctuate. Also, if a value other than the initial value (10H) is set to the HIOTRM register, the oscillation accuracy of the internal high-speed oscillation clock may exceed the MIN. and MAX. values described in CHAPTER 31 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) due to the subsequent fluctuation in the temperature or V_{DD} voltage, or HIOTRM register setting value. If the temperature or V_{DD} voltage fluctuates, accuracy correction must be executed either before frequency accuracy will be required or regularly.

(2) Capture/compare control register 00 (CRC00)

CRC00 is the register that controls the operation of CR000 and CR010.

Changing the value of CRC00 is prohibited during operation (when TMC003 and TMC002 = other than 00).

CRC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CRC00 to 00H.

Figure 6-6. Format of Capture/Compare Control Register 00 (CRC00)

Address: FFBCH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRC00	0	0	0	0	0	CRC002	CRC001	CRC000

CRC002	CR010 operating mode selection
0	Operates as compare register
1	Operates as capture register

CRC001	CR000 capture trigger selection
0	Captures on valid edge of TI010 pin
1	Captures on valid edge of TI000 pin by reverse phase[Note]
The valid edge of the TI010 and TI000 pin is set by PRM00. If ES001 and ES000 are set to 11 (both edges) when CRC001 is 1, the valid edge of the TI000 pin cannot be detected.	

CRC000	CR000 operating mode selection
0	Operates as compare register
1	Operates as capture register
If TMC003 and TMC002 are set to 11 (clear & start mode entered upon a match between TM00 and CR000), be sure to set CRC000 to 0.	

Note When the valid edge is detected from the TI010 pin, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal.

Caution To ensure that the capture operation is performed properly, the capture trigger requires a pulse two cycles longer than the count clock selected by prescaler mode register 00 (PRM00).

Figure 6-8. Format of 16-Bit Timer Output Control Register 00 (TOC00)

Address: FFBDH After reset: 00H R/W

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

OSPT00	One-shot pulse output trigger via software
0	–
1	One-shot pulse output
The value of this bit is always “0” when it is read. Do not set this bit to 1 in a mode other than the one-shot pulse output mode. If it is set to 1, TM00 is cleared and started.	

OSPE00	One-shot pulse output operation control
0	Successive pulse output
1	One-shot pulse output
One-shot pulse output operates correctly in the free-running timer mode or clear & start mode entered by TI000 pin valid edge input. The one-shot pulse cannot be output in the clear & start mode entered upon a match between TM00 and CR000.	

TOC004	TO00 output control on match between CR010 and TM00
0	Disables inversion operation
1	Enables inversion operation
The interrupt signal (INTTM010) is generated even when TOC004 = 0.	

LVS00	LVR00	Setting of TO00 pin output status
0	0	No change
0	1	Initial value of TO00 output is low level (TO00 output is cleared to 0).
1	0	Initial value of TO00 output is high level (TO00 output is set to 1).
1	1	Setting prohibited

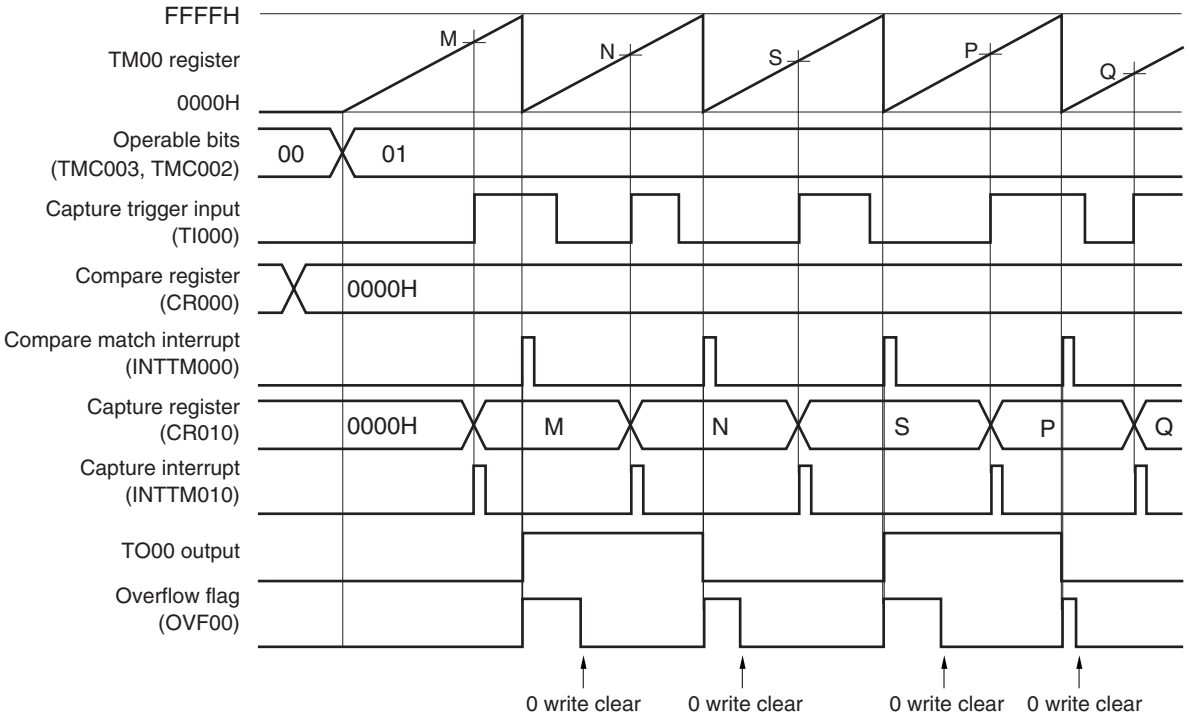
- LVS00 and LVR00 can be used to set the initial value of the TO00 output level. If the initial value does not have to be set, leave LVS00 and LVR00 as 00.
- Be sure to set LVS00 and LVR00 when TOE00 = 1.
  LVS00, LVR00, and TOE00 being simultaneously set to 1 is prohibited.
- LVS00 and LVR00 are trigger bits. By setting these bits to 1, the initial value of the TO00 output level can be set. Even if these bits are cleared to 0, TO00 output is not affected.
- The values of LVS00 and LVR00 are always 0 when they are read.
- For how to set LVS00 and LVR00, see **6.5.2 Setting LVS00 and LVR00**.
- The actual TO00/TI010/P34/TI52/RTC1HZ/INTP1 pin output is determined depending on PM34 and P34, besides TO00 output.

TOC001	TO00 output control on match between CR000 and TM00
0	Disables inversion operation
1	Enables inversion operation
The interrupt signal (INTTM000) is generated even when TOC001 = 0.	

TOE00	TO00 output control
0	Disables output (TO00 output fixed to low level)
1	Enables output

Figure 6-36. Timing Example of Free-Running Timer Mode (CR000: Compare Register, CR010: Capture Register)

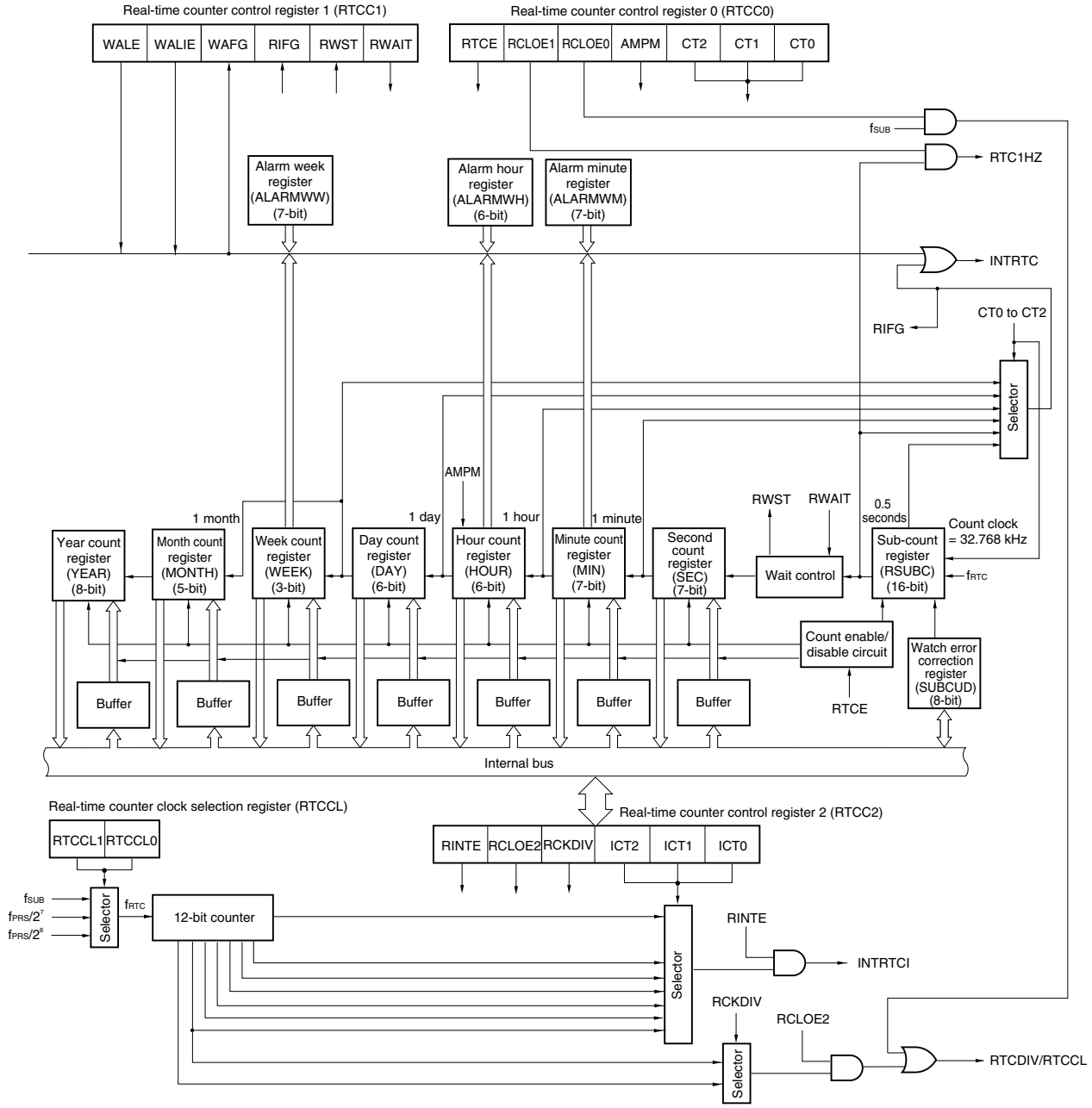
• TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 04H



This is an application example where a compare register and a capture register are used at the same time in the free-running timer mode.

In this example, the INTTM000 signal is generated and the TO00 output is reversed each time the count value of TM00 matches the set value of CR000 (compare register). In addition, the INTTM010 signal is generated and the count value of TM00 is captured to CR010 each time the valid edge of the TI000 pin is detected.

Figure 9-1. Block Diagram of Real-Time Counter



12.4.2 Input voltage and conversion results

The relationship between the analog input voltage input to the analog input pins (ANI0 to ANI7) and the theoretical A/D conversion result (stored in the 10-bit A/D conversion result register (ADCR)) is shown by the following expression.

$$SAR = INT\left(\frac{V_{AIN}}{AV_{REF}} \times 1024 + 0.5\right)$$

$$ADCR = SAR \times 64$$

or

$$\left(\frac{ADCR}{64} - 0.5\right) \times \frac{AV_{REF}}{1024} \leq V_{AIN} < \left(\frac{ADCR}{64} + 0.5\right) \times \frac{AV_{REF}}{1024}$$

where, INT( ): Function which returns integer part of value in parentheses

V_{AIN}: Analog input voltage

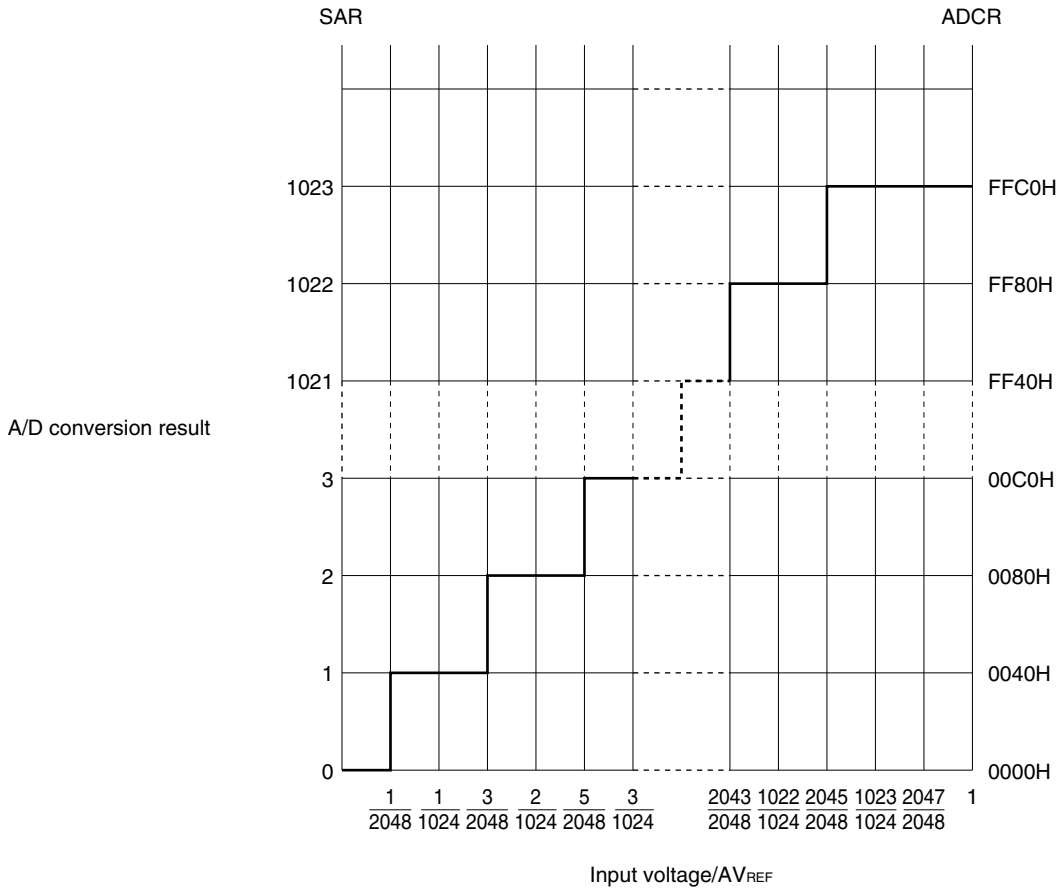
AV_{REF}: AV_{REF} pin voltage

ADCR: A/D conversion result register (ADCR) value

SAR: Successive approximation register

Figure 12-12 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 12-12. Relationship Between Analog Input Voltage and A/D Conversion Result



CHAPTER 14 SERIAL INTERFACE UART0

14.1 Functions of Serial Interface UART0

Serial interface UART0 has the following two modes.

(1) Operation stop mode

This mode is used when serial communication is not executed and can enable a reduction in the power consumption.

For details, see **14.4.1 Operation stop mode**.

(2) Asynchronous serial interface (UART) mode

The functions of this mode are outlined below.

For details, see **14.4.2 Asynchronous serial interface (UART) mode** and **14.4.3 Dedicated baud rate generator**.

- Maximum transfer rate: 625 kbps
- Two-pin configuration TxD0: Transmit data output pin
  RxD0: Receive data input pin
- Length of communication data can be selected from 7 or 8 bits.
- Dedicated on-chip 5-bit baud rate generator allowing any baud rate to be set
- Transmission and reception can be performed independently (full-duplex operation).
- Fixed to LSB-first communication

Cautions 1. If clock supply to serial interface UART0 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART0 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD0 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER0 = 0, RXE0 = 0, and TXE0 = 0.

2. Set POWER0 = 1 and then set TXE0 = 1 (transmission) or RXE0 = 1 (reception) to start communication.

3. TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.

4. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

The relationship between the register settings and pins is shown below.

Table 17-3. Relationship Between Register Settings and Pins

CSIAE0	ATE0	MASTER0	PM15	P15	PM16	P16	PM14	P14	Serial I/O Shift Register 0 Operation	Serial Clock Counter Operation Control	Pin Function		
											SIA0/P15	SOA0/P16	$\overline{\text{SCKA0}}$/P14 /INTP4
0	×	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	Operation stopped	Clear	P15	P16	P14/INTP4
1	0	0	1Note 2	×Note 2	0Note 3	0Note 3	1	×	Operation enabled	Count operation	SIA0Note 2	SOA0Note 3	$\overline{\text{SCKA0}}$ (input)
		1					0	1					$\overline{\text{SCKA0}}$ (output)

Notes 1. Can be set as port function.

2. Can be used as P15 when only transmission is performed. Clear bit 2 (RXEA0) of CSIMA0 to 0.

3. Can be used as P16 when only reception is performed. Clear bit 3 (TXEA0) of CSIMA0 to 0.

Remark ×: don't care
CSIAE0: Bit 7 of serial operation mode specification register 0 (CSIMA0)
ATE0: Bit 6 of CSIMA0
MASTER0: Bit 4 of CSIMA0
PM1×: Port mode register
P1×: Port output latch

(2) Automatic transmit/receive data setting

Here is an example of the procedure for successively transmitting/receiving data as the master.

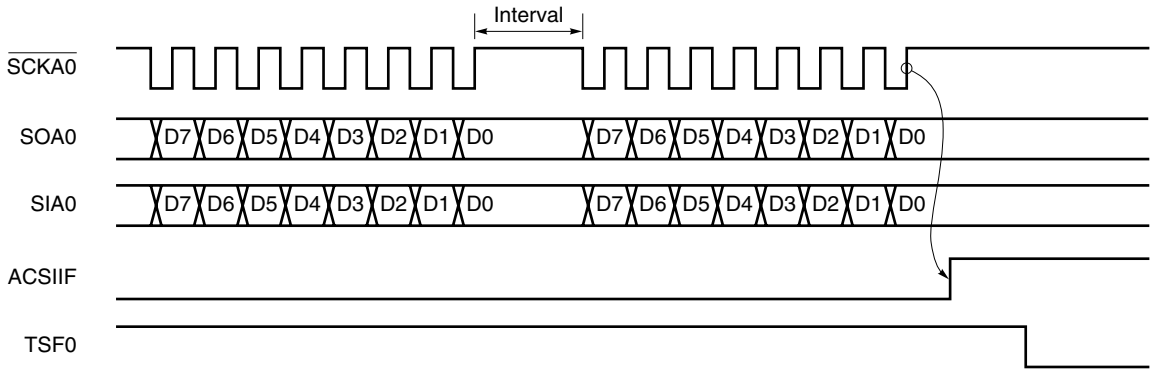
<1> Enable CSIA0 to operate by setting bit 7 (CSIAE0) of serial operation mode specification register 0 (CSIMA0) to 1 (the buffer RAM can now be accessed).
<2> Select a serial clock by using serial status register 0 (CSIS0).
<3> Set the division ratio of the serial clock by using division value selection register 0 (BRGCA0), and specify a communication rate.
<4> Sequentially write data to be transmitted to the buffer RAM, starting from the least significant address FA00H, up to FA1FH. Data is transmitted from the lowest address, continuing on to higher addresses.
<5> Set "number of data items to be transmitted − 1" to automatic data transfer address point specification register 0 (ADTP0).
<6> Set bits 6 (ATE0) and 4 (MASTER0) of CSIMA0 to select a master operation in the automatic communication mode.
<7> Set bits 3 (TXEA0) and 2 (RXEA0) of CSIMA0 to 1 to enable transmission/reception.
<8> Set the transmission interval of data to the automatic data transfer interval specification register (ADTI0).
<9> Automatic transmit/receive processing is started when bit 0 (ATSTA0) of serial trigger register 0 (CSIT0) is set to 1.

Caution Take the relationship with the other communicating party into consideration when setting the port mode register and port register.

Operations <1> to <9> execute the following operation.

- After the buffer RAM data indicated by automatic data transfer address count register 0 (ADTC0) is transferred to SIOA0, transmission is carried out (start of automatic transmission/reception).
- The received data is written to the buffer RAM address indicated by ADTC0.
- ADTC0 is incremented and the next data transmission/reception is carried out. Data transmission/reception continues until the ADTC0 incremental output matches the set value of automatic data transfer address point specification register 0 (ADTP0) (end of automatic transmission/reception). However, if bit 5 (ATM0) of CSIMA0 is set to 1 (repeat mode), ADTC0 is cleared after a match between ADTP0 and ADTC0, and then repeated transmission/reception is started.
- When automatic transmission/reception is terminated, an interrupt request (INTACSI) is generated and bit 0 (TSF0) of CSIS0 is cleared.
- To continue transmitting the next data, set the new data to the buffer RAM, and set "number of data to be transmitted − 1" to ADTP0. After setting the number of data, set ATSTA0 to 1.

Figure 17-14. Example of Automatic Transmission/Reception Mode Operation Timings

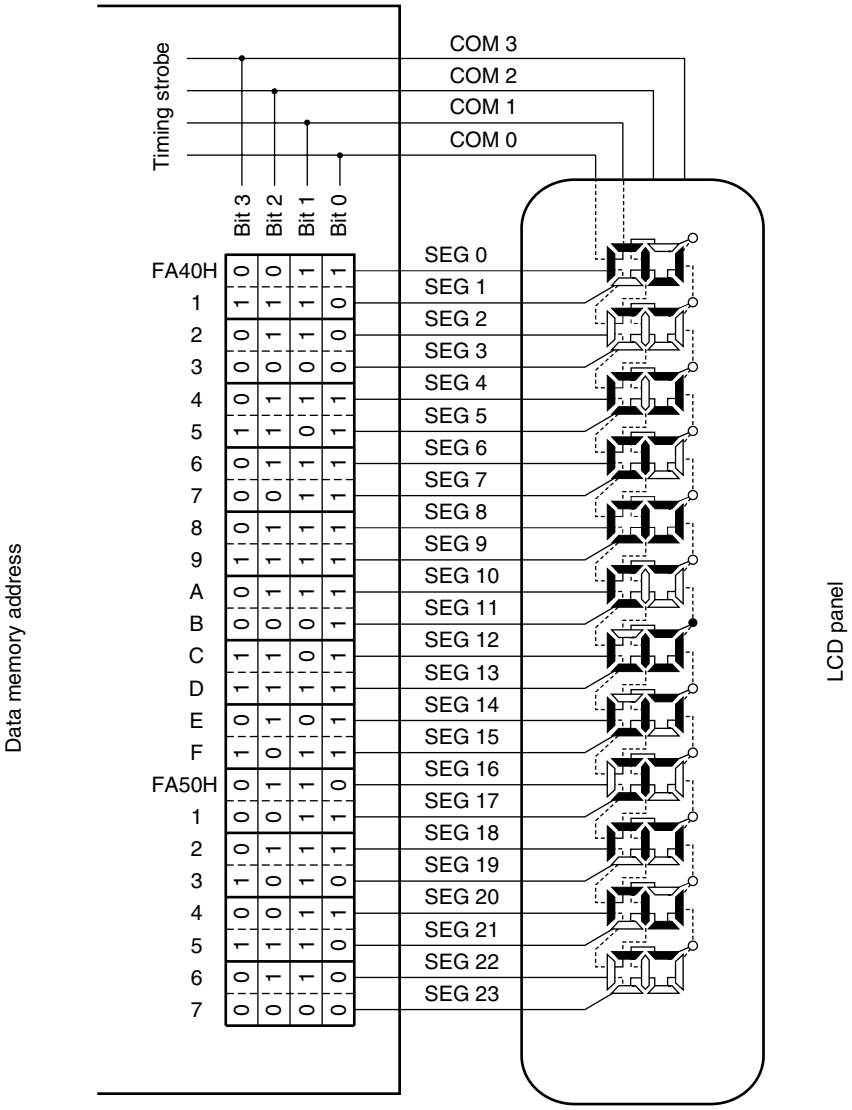


Cautions 1. Because, in the automatic transmission/reception mode, the automatic transmit/receive function writes/reads data to/from the internal buffer RAM after 1-byte transmission/reception, an interval is inserted until the next transmission/reception. As the buffer RAM write/read is performed at the same time as CPU processing, the interval is dependent upon the set value of automatic data transfer interval specification register 0 (ADTI0).

2. If an access to the buffer RAM by the CPU conflicts with an access to the buffer RAM by serial interface CSIA0 during the interval period, the interval time specified by automatic data transfer interval specification register 0 (ADTI0) may be extended.

Remark ACSIIF: Interrupt request flag
TSF0: Bit 0 of serial status register 0 (CSIS0)

Figure 18-28. Example of Connecting Four-Time-Slice LCD Panel



<2> Error of baud rate

The baud rate error can be calculated by the following expression.

- $\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1 \right) \times 100 \text{ [\%]}$

Caution Keep the baud rate error during transmission to within the permissible error range at the reception destination.

Example: Frequency of base clock = 2.5 MHz = 2,500,000 Hz
Set value of MC0BRS4 to MC0BRS0 bits of MC0CTL2 register = 10000B (k = 16)
Target baud rate = 76,800 bps

Baud rate = 2.5 M/(2 × 16)
= 2,500,000/(2 × 16) = 78125 [bps]

Error = (78,125/76,800 − 1) × 100
= 1.725 [%]

<3> Example of setting baud rate

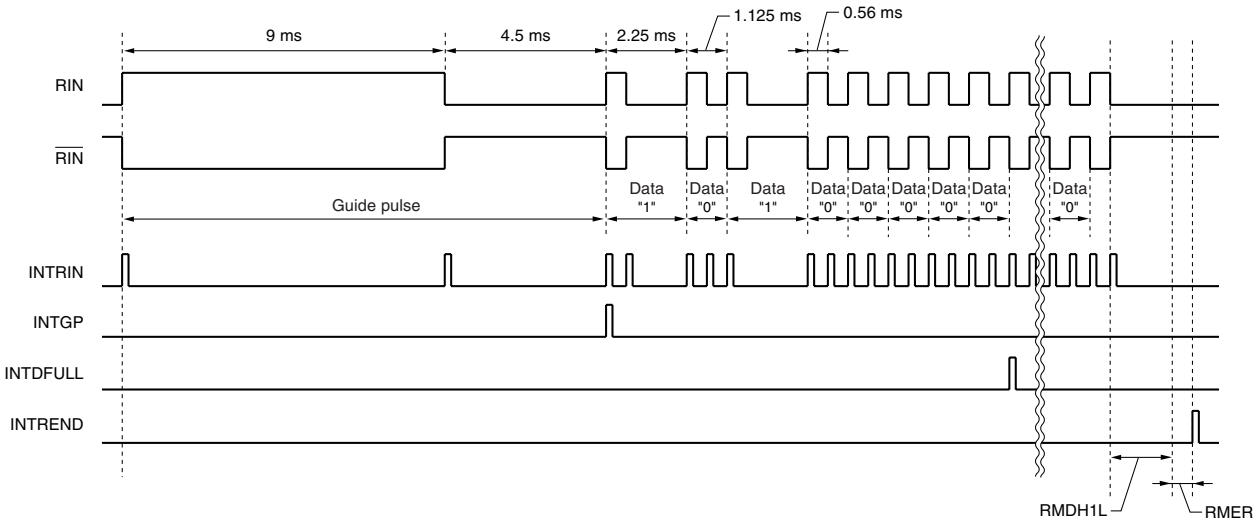
Baud Rate [bps]	f_{PRS} = 10.0 MHz				f_{PRS} = 8.38 MHz				f_{PRS} = 8.0 MHz				f_{PRS} = 6.0 MHz			
	MC0CKS2 to MC0CKS0	k	Calculated Value	ERR [%]	MC0CKS2 to MC0CKS0	k	Calculated Value	ERR [%]	MC0CKS2 to MC0CKS0	k	Calculated Value	ERR [%]	MC0CKS2 to MC0CKS0	k	Calculated Value	ERR [%]
4800	–	–	–	–	5, 6, or 7	27	4850	1.03	5, 6, or 7	26	4808	0.16	5, 6, or 7	20	4688	–2.34
9600	5, 6, or 7	16	9766	1.73	4	27	9699	1.03	5, 6, or 7	13	9615	0.16	4	20	9375	–2.34
19200	5	8	19531	1.73	3	27	19398	1.03	4	13	19231	0.16	4	10	18750	–2.34
31250	4	10	31250	0	2	17	30809	–1.41	4	8	31250	0	2	24	31250	0
38400	4	8	39063	1.73	2	27	38796	1.03	3	13	38462	0.16	2	20	37500	–2.34
56000	3	11	56818	1.46	2	19	55132	–1.55	3	9	55556	–0.79	1	27	55556	–0.79
62500	2	20	62500	0	2	17	61618	–1.41	3	8	62500	0	2	12	62500	0
76800	2	16	78125	1.73	1	27	77592	1.03	2	13	76923	0.16	2	10	75000	–2.34
115200	1	22	113636	–1.36	2	9	116389	1.03	1	17	117647	2.12	1	13	115385	0.16
125000	1	20	125000	0	1	17	123235	–1.41	1	16	125000	0	1	12	125000	0
153600	1	16	156250	1.73	2	7	149643	–2.58	1	13	153846	0.16	1	10	150000	–2.34
250000	1	10	250000	0	1	8	261875	4.75	1	8	250000	0	1	6	250000	0
					0	17	246471	–1.41								

Remark MC0CKS2 to MC0CKS0: Bits 2 to 0 of MCG control register 1 (MC0CTL1) (setting of base clock (f_{XCLK}))
k: Value set by bits 4 to 0 (MC0BRS4 to MC0BRS0) of MCG control register 2 (MC0CTL2) (k = 4, 5, 6, …, 31)
f_{PRS}: Peripheral hardware clock frequency
ERR: Baud rate error

20.4.3 Format of type B reception mode

Figure 20-8 shows the data format for type B.

Figure 20-8. Example of Type B Data Format



Remark $\overline{\text{RIN}}$ is the internally inverted signal of RIN.

20.4.4 Operation flow of type B reception mode

Figure 20-9 shows the operation flow.

Cautions 1. When INTRERR is generated, RMSR and RMSCR are automatically cleared immediately.

2. When data has been set to all the bits of RMSR, the following processing is automatically performed.

- **The value of RMSR is transferred to RMDR.**
- **INTDFULL is generated.**
- **RMSR is cleared.**

RMDR must then be read before the next data is set to all the bits of RMSR.

3. When INTREND has been generated, read RMSCR first followed by RMSR.
When RMSR has been read, RMSCR and RMSR are automatically cleared.
If INTREND is generated, the next data cannot be received until RMSR is read.

4. RMSR, RMSCR, and RMDR are cleared simultaneously to operation termination (RMEN = 0).

(3) Type C reception mode

The INTRERR signal is generated under any of the following conditions.

- Counter < RMDLS at the rising edge of $\overline{\text{RIN}}$
- Register changes so that RMDLL ≤ counter while $\overline{\text{RIN}}$ is at low level
- Counter < RMDH0S at the falling edge of $\overline{\text{RIN}}$
- RMDH0L ≤ counter < RMDH1S at the falling edge of $\overline{\text{RIN}}$
- RMDH1L ≤ counter and counter after RMDH1L < RMER at the falling edge of $\overline{\text{RIN}}$

However, before the first INTDFULL interrupt is generated, INTRERR signal will not be generated.

The generation timing of the INTRERR signal is shown in Figure 20-15.

(1) Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

IF0L, IF0H, IF1L, and IF1H are set by a 1-bit or 8-bit memory manipulation instruction. When IF0L and IF0H, and IF1L and IF1H are combined to form 16-bit registers IF0 and IF1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 21-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	CSIIF10 STIF0	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
<R> IF1L	TMIF52	DSADIF Note 2	RTCIIF	KRIF	TMIF51	RTCIF	SRIF0	ADIF Note 1

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
IF1H	0	0	0	ACSIIF	RERRIF GPIF RENIF DFULLIF	RINIF	MCGIF	TMHIF2

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Notes 1. μPD78F048x and 78F049x only.

2. μPD78F049x only.

Cautions 1. Be sure to clear bits 5 to 7 of IF1H to 0.

2. When operating a timer, serial interface, or A/D converter after standby release, operate it once after clearing the interrupt request flag. An interrupt request flag may be set by noise.

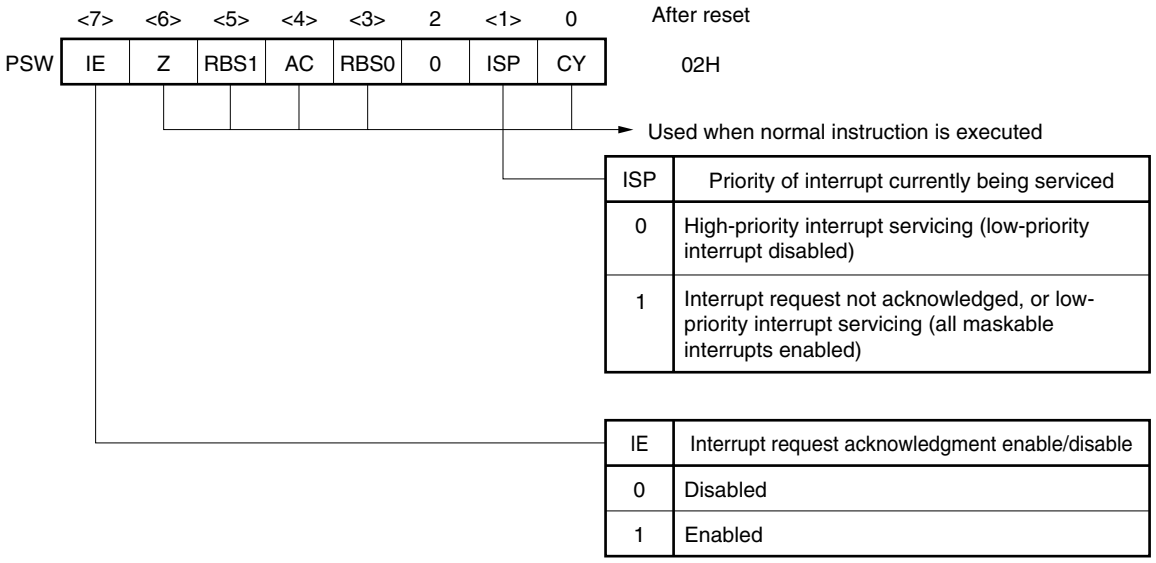
(5) Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP flag that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. If a maskable interrupt request is acknowledged, the contents of the priority specification flag of the acknowledged interrupt are transferred to the ISP flag. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets PSW to 02H.

Figure 21-6. Format of Program Status Word

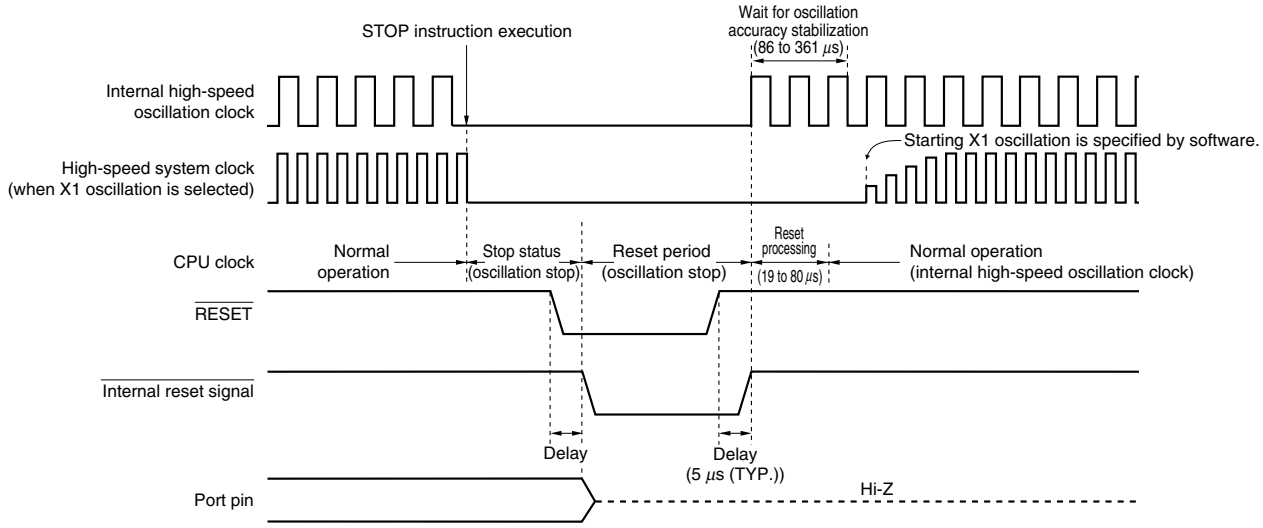


ISP	Priority of interrupt currently being serviced
0	High-priority interrupt servicing (low-priority interrupt disabled)
1	Interrupt request not acknowledged, or low-priority interrupt servicing (all maskable interrupts enabled)

IE	Interrupt request acknowledgment enable/disable
0	Disabled
1	Enabled

<R>

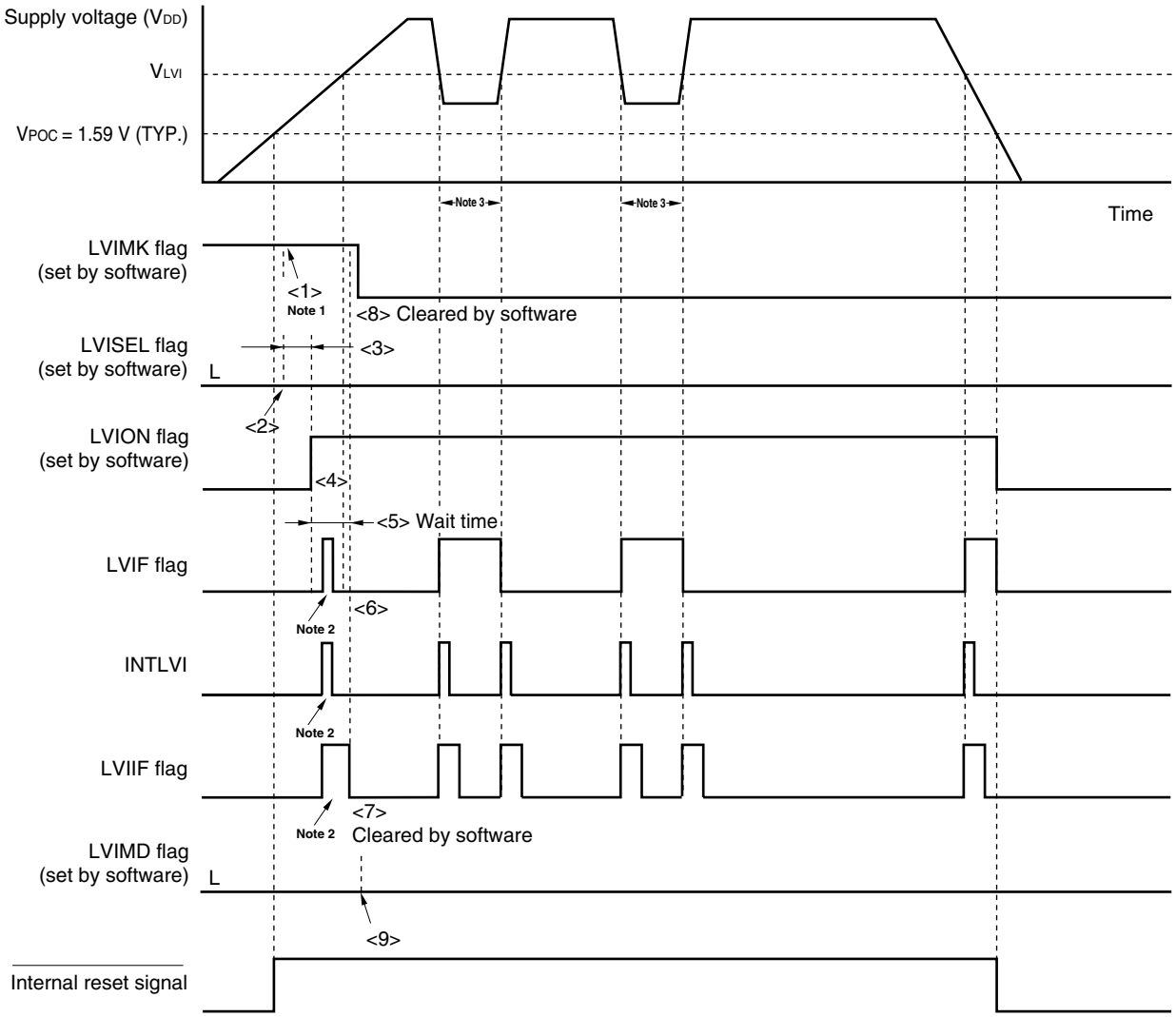
Figure 24-4. Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input



Remark For the reset timing of the power-on-clear circuit and low-voltage detector, see **CHAPTER 25 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 26 LOW-VOLTAGE DETECTOR**.

Figure 26-7. Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Supply Voltage (V_{DD})) (1/2)

(1) In 1.59 V POC mode (option byte: POCMODE = 0)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVION is cleared (0) in a state below the LVI detection voltage, an INTLVI signal is generated and LVIIF becomes 1.

Remark <1> to <9> in Figure 26-7 above correspond to <1> to <9> in the description of "When starting operation" in **26.4.2 (1) When detecting level of supply voltage (V_{DD})**.